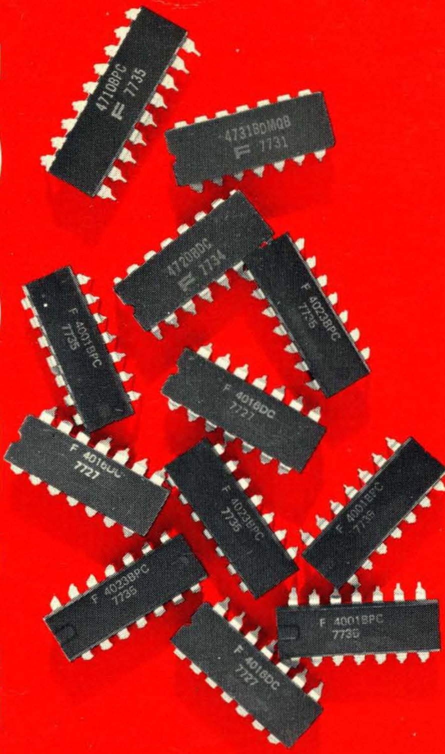
CMOS DATA BOOK



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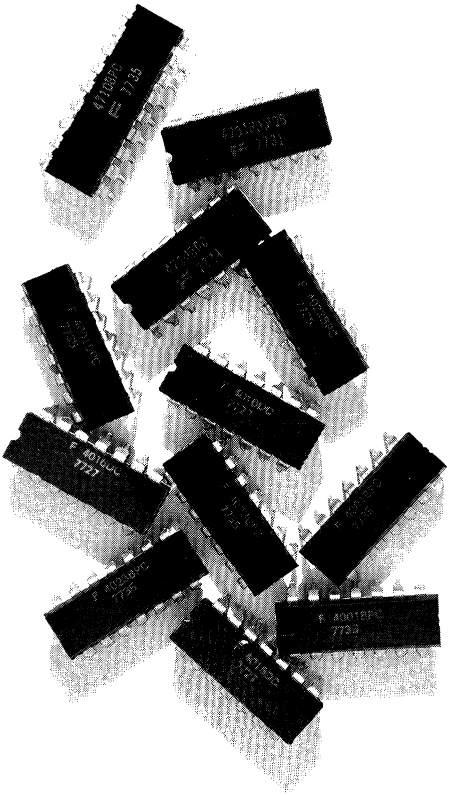
CMOS DATA BOOK



464 Ellis Street, Mountain View, California 94042

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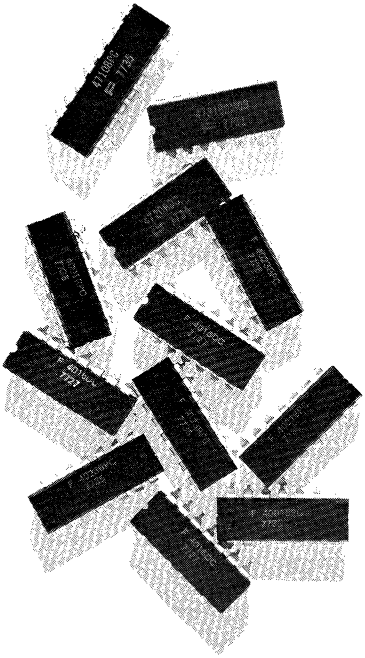


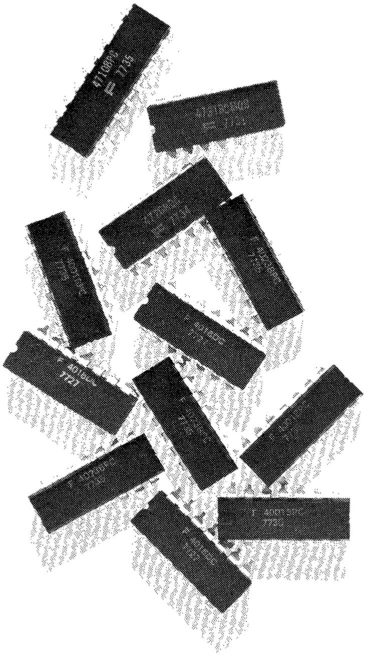
INTRODUCTION

This data book provides complete technical information on Fairchild's 4000B Series Isoplanar CMOS family. The family encompasses a wide range of SSI, MSI and LSI devices offering the designer a complete spectrum of various circuit complexities all at highest performance. For easy reference to this broad range of devices, a number if indices, selection guides and cross references can be found in Sections 2 and 3.

Since the first introduction of CMOS in the early 1970s, and as each new generation of designs was developed, a large variety of functional and performance parameters were generated by the industry creating a great deal of customer confusion.

In late 1976, under the auspices of EIA/JEDEC, the CMOS vendor community accepted the formidable task of clearing this confusion via industry-wide standardization. The result, as found in Section 6 of this book, is the new "Jedec Industry Standard 'B' Series CMOS Specification." Fairchild lauds EIA/JEDEC and the industry in total for such a cooperative and valuable effort and encourages continuation of this trend.

It should be noted that all Fairchild CMOS products have always, since first introduction in early 1974, complied with today's JEDEC CMOS specifications. Furthermore, it should be noted that Fairchild offers the only CMOS family which meets or exceeds all functional and performance parameters of all CMOS devices and generations of devices introduced to date. Fairchild continues to provide leadership in technology.



NUMERICAL INDEX OF DEVICES

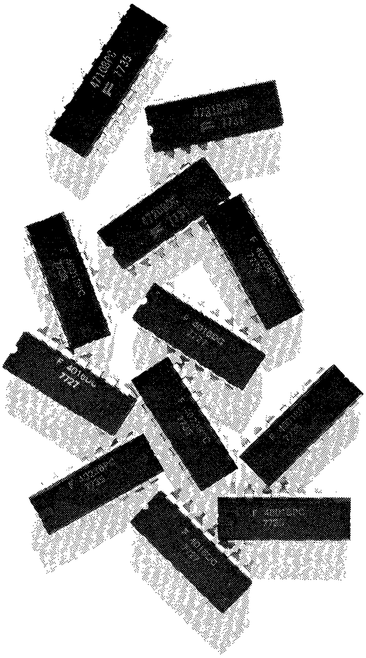
LOGIC DEVICES

NUMERICAL INDEX OF DEVICES

LOGIC DEVICES

NUMERICAL INDEX OF DEVICES

LOGIC DEVICES



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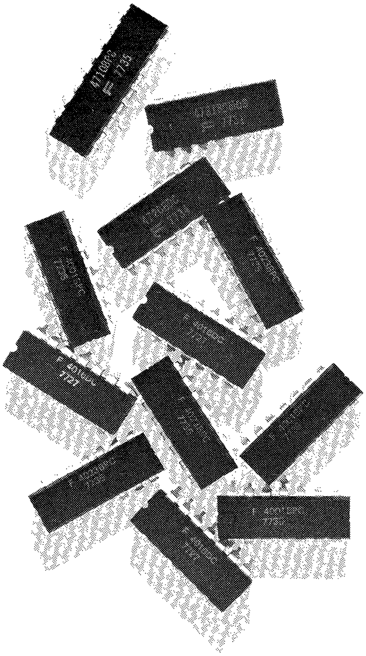


FAIRCHILD 4000

SERIES CMOS

GENERAL DESCRIPTION – Fairchild CMOS logic combines popular 4000 series functions with the advanced Isoplanar C process. The result is a logic family with a superior combination of noise immunity and standardized drive characteristics. Under static conditions, these devices dissipate very low power, typically 10 nW per gate. The low power combined with the wide (3 to 15 V) recommended operating supply voltage requirement greatly minimizes power supply costs. The CMOS family is designed with standardized output drive characteristics which, combined with relative insensitivity to output capacitance loading, simplify system design.

- **LOW POWER – TYPICALLY 10 nW PER GATE STATIC**
- **WIDE OPERATING SUPPLY VOLTAGE RANGE –**
  3 TO 15 V RECOMMENDED
  18 V ABSOLUTE MAXIMUM
- **HIGH NOISE IMMUNITY**
- **BUFFERED OUTPUTS STANDARDIZE OUTPUT DRIVE AND REDUCE VARIATION OF PROPAGATION DELAY WITH OUTPUT CAPACITANCE**
- **WIDE OPERATING TEMPERATURE RANGE**
  COMMERCIAL -40°C TO +85°C
  MILITARY -55°C TO +125°C
- **HIGH DC FAN OUT – GREATER THAN 50**

ISOPLANAR C

The Fairchild CMOS logic family uses Isoplanar C for high performance. This technology combines local oxidation isolation techniques with silicon gate technology to achieve an approximate 35% to 100% savings in area as shown in Figure 4-1a. Operating speeds are increased due to the self-alignment of the silicon gate and reduced sidewall capacitance.

Conventional CMOS circuits are fabricated on an n-type substrate as shown in Figure 4-1b. The p-type substrate required for complementary n-channel MOS is obtained by diffusing a lightly doped p-region into the n-type substrate. Conventional CMOS fabrication requires more chip area and has slower circuit speeds than Isoplanar C CMOS. This is a result of the n+ or p+ channel stop which surrounds the p- or n-channels respectively in conventional metal gate CMOS. Silicon gate CMOS (Figure 4-1c) has a negligible reduction in area, though transient performance is improved.

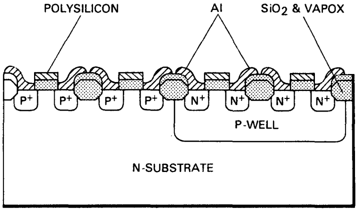


Fig. 4-1a. ISOPLANAR C CMOS STRUCTURE REDUCES AREA 35%

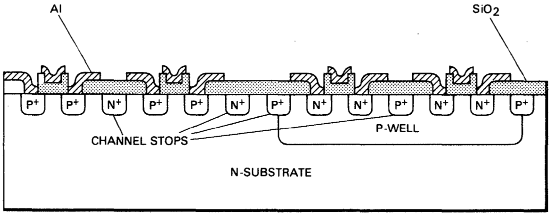


Fig. 4-1b. CONVENTIONAL METAL GATE CMOS STRUCTURE

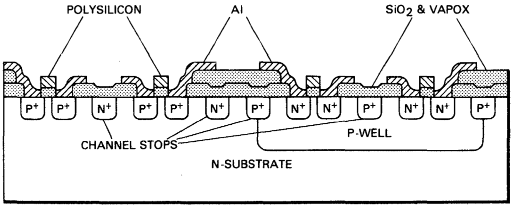


Fig. 4-1c. CONVENTIONAL SILICON GATE CMOS STRUCTURE REDUCES AREA 8%

FULLY BUFFERED CONFIGURATION DESCRIPTION

Fairchild CMOS logic is designed with the system user in mind. Output buffering is used on all devices to achieve high performance, standardized output drive, highest noise immunity and decreased ac sensitivity to output loading. Figure 4-2 illustrates a conventional unbuffered 2-Input NOR Gate. Either n-channel transistor connected to V_{SS} (ground) conducts when either input is HIGH, causing the output to go LOW through the ON resistance of the device. If both inputs are HIGH, both n-channel devices are on; effectively halving the ON resistance, thereby making the output impedance (and hence fall time) a function of input variables. Similarly the p-channel devices are switched on by LOW signals; i.e., when both inputs are LOW, conduction from V_{DD} to the output will occur.

Since the p-channel devices are in series, their ON resistance must be decreased (larger chip area) to hold output HIGH impedance within specification. As the number of gate inputs increases, even larger p-channel devices are required, and the output impedance to V_{SS} becomes even more pattern sensitive.

A conventional unbuffered CMOS 2-Input NAND Gate interchanges the parallel and serial transistor gating to achieve the NAND function (Figure 4-3). The changes in output resistance then move to the p-channel transistors connected to V_{DD}, while the n-channel devices must be increased in size due to their serial connection.

Fairchild CMOS uses small geometry logic transistors to generate the required function which drive standard low impedance output buffers (Figures 4-4 and 5). This technique reduces chip size, since only two large output transistors are required and rise and fall times are independent of input pattern. Buffered outputs also increase system speeds and make propagation delay less sensitive to output capacitance. Figure 4-6 illustrates typical propagation delay vs. output capacitance for conventional and buffered CMOS Gates.

Another advantage of the Fairchild approach is improved noise immunity. Because of the increased voltage gain, nearly ideal transfer characteristics are realized as shown in Figure 4-7. The high gain (greater than 10,000) also provides significant pulse shaping; the waveforms of Figures 4-8 and 9 compare the output waveforms of conventional and buffered CMOS gates. For input transition times of 100 ns or less, the outputs of both gate types are similar. When the input transitions are stretched to one microsecond, the conventional gate exhibits increased transition times while the buffered gate has unchanged output transition times. This feature eliminates progressive deterioration of pulse characteristics in a system. The combination of Isoplanar C and buffered outputs results in new standards of CMOS logic performance.

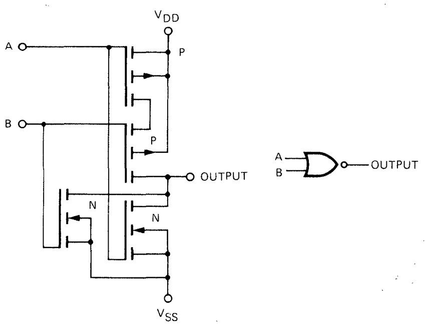


Fig. 4-2. CONVENTIONAL NON-BUFFERED 2-INPUT NOR GATE

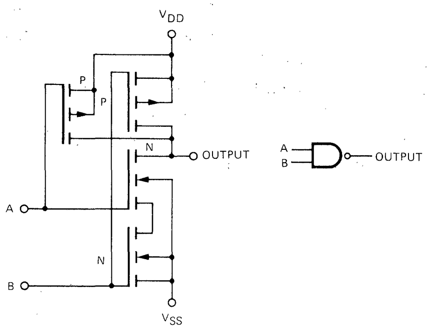


Fig. 4-3. CONVENTIONAL NON-BUFFERED 2-INPUT NAND GATE

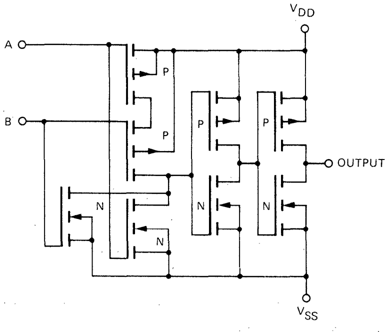


Fig. 4-4. FAIRCHILD 4001B FULLY BUFFERED NOR GATE

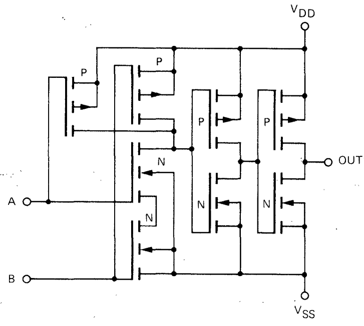


Fig. 4-5. FAIRCHILD 4011B FULLY BUFFERED NAND GATE

Fig. 4-6
COMPARISON OF PROPAGATION DELAY VS LOAD CAPACITANCE FOR CONVENTIONAL AND FULLY BUFFERED NAND GATES

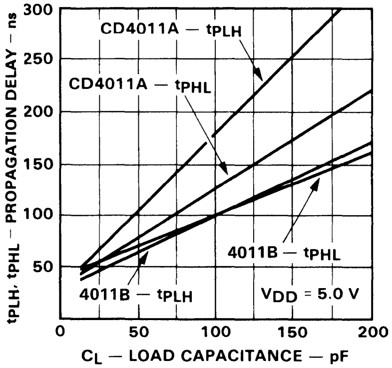


Fig. 4-7
TYPICAL VOLTAGE TRANSFER CHARACTERISTICS FOR CONVENTIONAL AND FULLY BUFFERED DEVICES

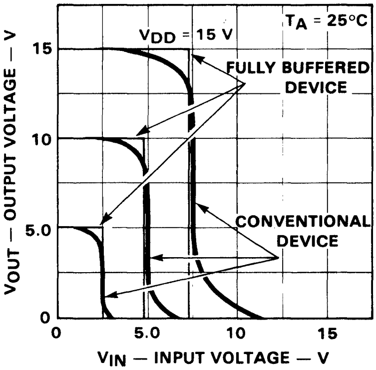


Fig. 4-8
POSITIVE-GOING INPUT RAMPS OF 0.1 μs AND 1.0 μs APPLIED TO CONVENTIONAL AND FULLY BUFFERED GATES

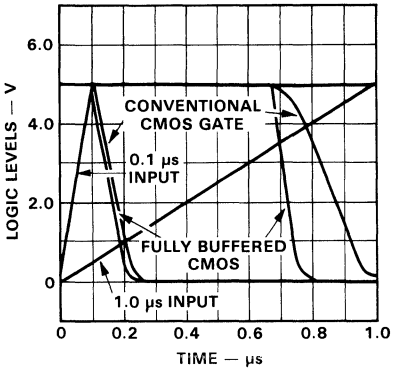
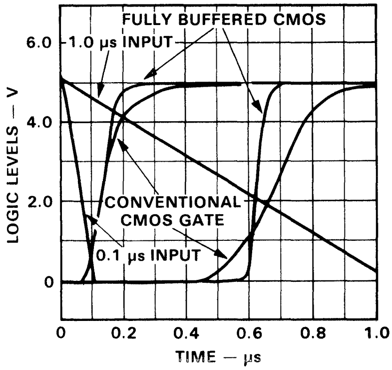
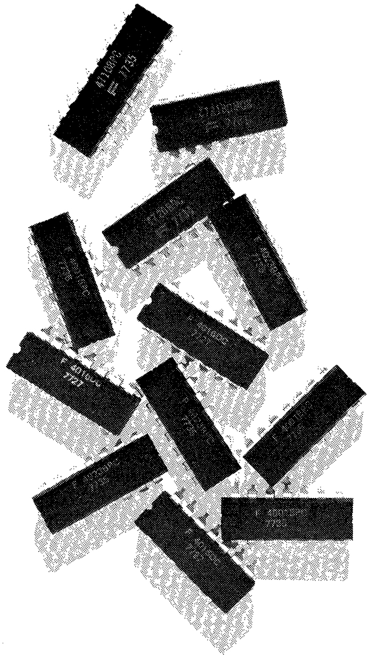


Fig. 4-9
NEGATIVE-GOING INPUT RAMPS OF 0.1 μs AND 1.0 μs APPLIED TO CONVENTIONAL AND FULLY BUFFERED GATES





DESIGN CONSIDERATIONS
WITH FAIRCHILD 4000B SERIES CMOS

INTRODUCTION

Complementary MOS digital logic building blocks of SSI and MSI complexity have been hailed as the ideal logic family. They are rapidly gaining popularity as more and more manufacturers introduce increasing numbers of parts at reasonable prices.

Originally designed for aerospace applications, CMOS now finds its way into portable instruments, industrial and medical electronics, automotive applications and computer peripherals, besides dominating the electronic watch market.

In late 1973, Fairchild introduced the Fairchild 4000B CMOS family, using Isoplanar technology to achieve superior electrical performance. Most of these devices are functional equivalents and pin-for-pin replacements of the well-known 4000 series; some are equivalent to TTL circuits and some are proprietary logic designs.

A few CMOS devices, such as bidirectional analog switches, exploit the unique features of CMOS technology; some take advantage of the smaller device size and higher potential packing density to achieve true LSI complexity; but most of the available CMOS elements today are of SSI and MSI complexity and perform logic functions that have been available in DTL or TTL for many years. Therefore, it is both helpful and practical to compare the performance of CMOS with that of the more familiar DTL/TTL *(Figure 5-1)*. The TTL to CMOS Comparison Guide in Section 3 lists numerous CMOS circuits that are pinout identical to their TTL counterparts, others that are functionally identical only, still others that are similar and, in most cases, offer added features.

CMOS speed is comparable to 74L-TTL and DTL, and about three to six times slower than TTL or Low Power Schottky (LS-TTL). Voltage noise immunity and fan out are almost ideal, supply voltage is noncritical, and the quiescent power consumption is close to zero-several orders of magnitude lower than for any competing technology.

POWER CONSUMPTION

Under static conditions, the p-channel (top) and the n-channel (bottom) transistors are not conducting simultaneously, thus only leakage current flows from the positive (V_{DD}) to the negative (V_{SS}) supply connection. This leakage current is typically 0.5 nA per gate, resulting in very attractive low power consumption of 2.5 nW per gate (at 5 V).

Whenever a CMOS circuit is exercised, when data or clock inputs change, additional power is consumed to charge and discharge capacitances (on-chip parasitic capacitances as well as load capacitances). Moreover, there is a short time during the transition when both the top and the bottom transistors are partially conducting. This dynamic power consumption is

PARAMETER	STANDARD TTL	74L	DTL	LOW POWER SCHOTTKY	FAIRCHILD 4000B CMOS 5 V SUPPLY	FAIRCHILD 4000B CMOS 10 V SUPPLY
PROPAGATION DELAY (GATE)	10 ns	33 ns	30 ns	5 ns	40 ns	20 ns
FLIP-FLOP TOGGLE FREQUENCY	35 MHz	3 MHz	5 MHz	45 MHz	8 MHz	16 MHz
QUIESCENT POWER (GATE)	10 mW	1 mW	8.5 mW	2 mW	10 nW	10 nW
NOISE IMMUNITY	1 V	1 V	1 V	0.8 V	2 V	4 V
FAN OUT	10	10	8	20	50*	50*

*OR AS DETERMINED BY ALLOWABLE PROPAGATION DELAY

Fig. 5-1 CMOS COMPARED TO OTHER LOGIC FAMILIES

obviously proportional to the frequency at which the circuit is exercised, to the load capacitance and to the square of the supply voltage. As shown in *Figure 5-2,* the power consumption of a CMOS gate exceeds that of a Low Power Schottky gate somewhere between 500 kHz and 2 MHz of actual output frequency.

At 100 transitions per second, the dynamic power consumption is far greater than the static dissipation; at one million transitions per second, it exceeds the power consumption of LS-TTL. Comparing the power consumption of more complex devices (MSI) in various technologies may show a different result. In any complex design, only a small fraction of the gates actually switch at the full clock frequency, most gates operate at a much lower average rate and consume, therefore, much less power.

A realistic comparison of power consumption between different technologies involves a thorough analysis of the average switching speed of each gate in the circuit. The small static supply current, I_{DD} is specified on individual data sheets for 5, 10 and 15 V. The dynamic power dissipation for 5, 10 and 15 V, 15 and 50 pF may be found in graph form for frequencies of 100 Hz to 10 MHz. The total power may be calculated, $P_T = (I_{DD} \times V_{DD})$ + dynamic power dissipation.

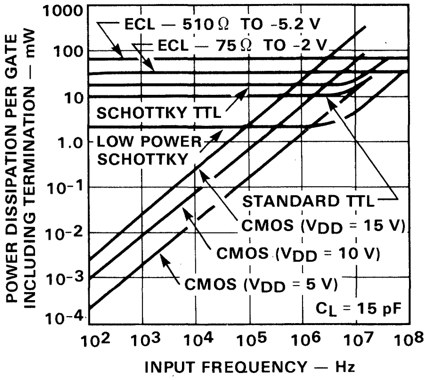
SUPPLY VOLTAGE RANGE

CMOS is guaranteed to function over the unprecedented range of 3 to 15 V supply voltage. Characteristics are guaranteed for 5, 10 and 15 V operation and can be extrapolated for any voltage in between. Operation below 4.5 V is not very meaningful because of the increase in delay (loss of speed), the increase in output impedance and the loss of noise immunity. Operation above 15 V is not recommended because of high dynamic power consumption and risk of noise spikes on the power supply exceeding the breakdown voltage (typ >20 V), causing SCR-latch-up and destroying the device unless the current is externally limited.

The lower limit of power supply voltage, including ripple, is determined by the required noise immunity, propagation delay or interface to TTL. The upper limit of supply voltage, including ripple and transients, is determined by power dissipation or direct interface to TTL. The 4049B, 4050B, 4104B, 40097B and 40098B provide level translation between TTL and CMOS when CMOS supply voltages over 5 V are used. While devices are usable to 18 V, operation above 12 V is discouraged for reasons of power dissipation.

Low static power consumption combined with wide supply voltage range make CMOS the ideal logic family for battery operated equipment.

Fig. 5-2
TYPICAL POWER DISSIPATION VERSUS INPUT FREQUENCY FOR SEVERAL POPULAR LOGIC FAMILIES



PROPAGATION DELAY

Compared to TTL and LS-TTL, all CMOS devices are slow and very sensitive to capacitive loading. See *Figure 5-3.* The Fairchild 4000B family uses both advanced processing (Isoplanar) and improved circuit design (buffered gates) to achieve propagation delays and output rise times that are superior to any other junction-isolated CMOS design. (Silicon-on-sapphire, SOS, can achieve similar performance but at a substantial cost penalty).

Isoplanar processing achieves lower parasitic capacitances which reduce the on-chip delay and increase the maximum toggle frequency of flip-flops, registers and counters. Buffering all outputs, even on gates, results in lower output impedance and thus reduces the effect of capacitive loading.

Propagation delay is affected by three parameters: capacitive loading, supply voltage, and temperature.

Capacitive Loading Effect

Historically, semiconductor manufacturers have always specified the propagation delay at an output load of 15 pF, not because anybody considers this a representative systems environment, but rather because it was the lowest practical test-jig capacitance. It also generated the most impressive specifications. TTL with an output impedance less than 100 Ω is little affected by an increase in capacitive loading; a 100 pF load increases the delay by only about 4 ns. CMOS, however, with an output impedance of 1 kΩ (worst case at 5 V) is 10 times more sensitive to capacitive loading. *Figure 5-4* shows the positive- and negative-going delays as a function of load capacitance. It should be noted that the older, unbuffered gates have an even higher output impedance, a larger dependence on output loading, and do not show the same symmetry.

Fig. 5-3
NORMALIZED PROPAGATION DELAY VERSUS LOAD CAPACITANCE FOR TTL AND CMOS

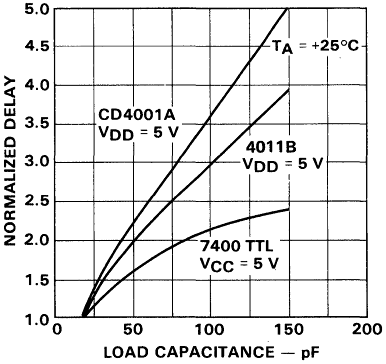


Fig. 5-4a
POSITIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE

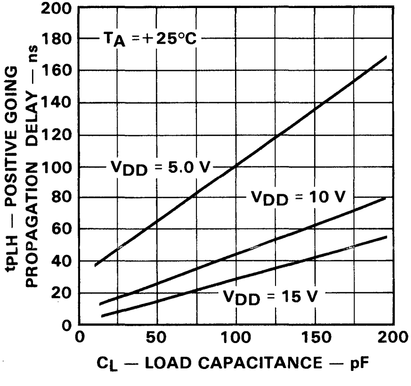
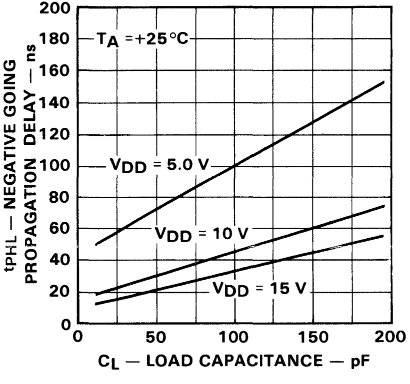


Fig. 5-4b
NEGATIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE



Supply Voltage Effect

Figure 5-5 shows propagation delay as a function of supply voltage and again indicates the symmetry of the positive- and negative-going delays. Increasing the supply voltage from 5 to 10 V more than doubles the speed of CMOS gates. Increasing the supply voltage to 15 V almost doubles the speed again, but, as mentioned before, results in a significant increase in dynamic power dissipation.

The best choice for slow applications is 5 V. For reasonably fast systems, choose 10 or 12 V. Any application requiring 15 V to achieve short delays and fast operation should be investigated for excessive power dissipation and should be weighed against an LS-TTL approach.

Fig. 5-5a
POSITIVE-GOING PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE

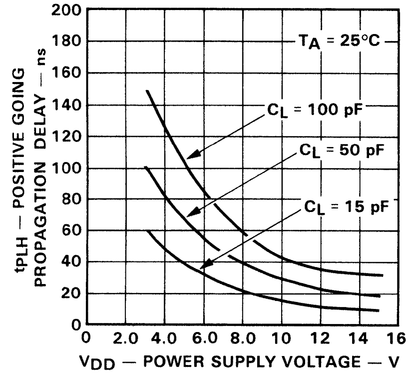
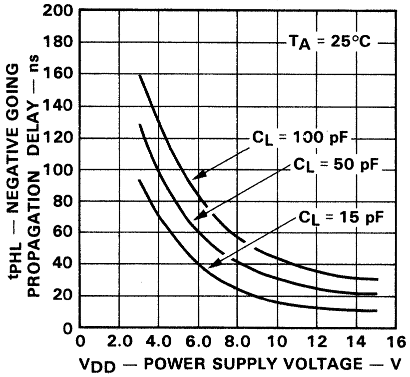


Fig. 5-5b
NEGATIVE-GOING PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



Temperature Effect

Figure 5-6 shows propagation delay as a function of ambient temperature. The temperature dependence of CMOS is much simpler than with TTL, where three factors contribute—increase of beta with temperature, increase of resistor value with temperature, and decrease of junction forward voltage drop with increasing temperature. In CMOS, essentially only the carrier mobility changes, thus increasing the impedance and hence the delay with temperature. For 4000B devices, this temperature dependence is less than 0.3% per °C, practically linear over the full temperature range. Note that the commercial temperature range is −40 to +85°C rather than the usual 0 to +75°C.

Fig. 5-6a
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE WITH V_{DD} = 5 V

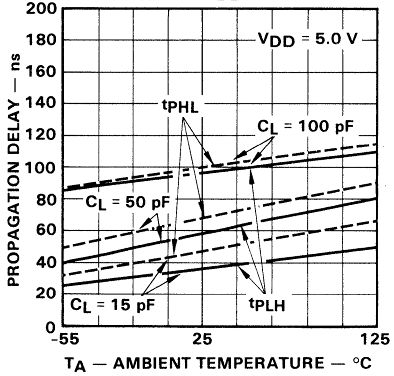
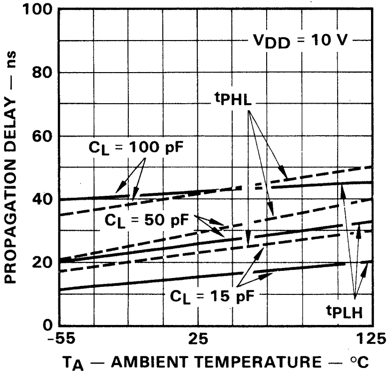


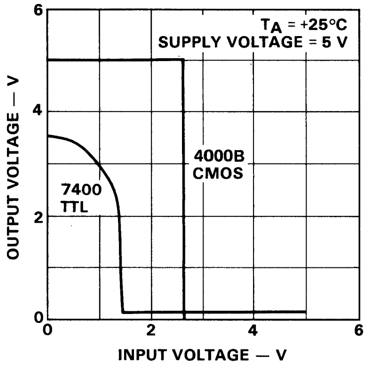
Fig. 5-6b
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE WITH V_{DD} = 10 V



CMOS delays increase with temperature. They are very sensitive to capacitive loading but can be reduced by increasing the supply voltage to 10 or even 15 V.

To determine propagation delays, the effects of capacitive loading, supply voltage, manufacturing tolerances and ambient temperature must be considered. Start with the values of t_{PLH} (propagation delay, a LOW-to-HIGH output transition) and t_{PHL} (propagation delay, a HIGH-to-LOW output transition) given in the individual data sheets. Delay values for V_{DD} at 5, 10 and 15 V and output capacity of 50 pF is provided. Manufacturing tolerances account for the differences between MIN, TYP and MAX. Starting with the nearest applicable delay value, correct for effects of capacitive loading, ambient temperature and supply voltage using the general family characteristics of Section 7.

Fig. 5-7
TYPICAL TRANSFER CHARACTERISTICS FOR TTL AND CMOS



NOISE IMMUNITY

One of the most advertised and also misunderstood CMOS features is noise immunity. The input threshold of a CMOS gate is approximately 50% of the supply voltage and the voltage transfer curve is almost ideal. As a result, CMOS can claim very good voltage noise immunity, typically 45% of the supply voltage, *i.e.,* 2.25 V in a 5 V system, 4.5 V in a 10 V system. Compare this with the TTL transfer curve in *Figure 5-5* and its resultant 1 V noise immunity in a lightly loaded system and only 0.4 V worst case.

Since CMOS output impedance, output voltage and input threshold are symmetrical with respect to the supply voltage, the LOW and HIGH level noise immunities are practically equal. Therefore, a CMOS system can tolerate ground or V_{DD} drops and noise on these supply lines of more than 1 V, even in a 5 V system. Moreover, the inherent CMOS delays act as a noise filter; 10 ns spikes tend to disappear in a chain of CMOS gates, but are amplified in a chain of TTL gates. Because of these features, CMOS is very popular with designers of industrial control equipment that must operate in an electrically and electromagnetically "polluted" environment.

Unfortunately these impressive noise margin specifications disregard one important fact: the output impedance of CMOS is 10 to 100 times higher than that of TTL. CMOS interconnections are therfore less "stiff" and much more susceptible to capacitively coupled noise. In terms of such current injected crosstalk from high noise voltages through small coupling capacitances, CMOS has about six times *less* noise margin than TTL. It takes more than 20 mA to pull a TTL output into the threshold region, but it takes only 3 mA to pull a CMOS output into the threshold of a 5 V system.

The nearly ideal transfer characteristic and the slow response of CMOS circuits make them insensitive to low voltage, magnetically coupled noise. The high output impedance, however, results in a poor rejection of capacitively coupled noise.

INTERFACE TO TTL

When CMOS is operated with a 5 V power supply, interface to TTL is straightforward. The input impedance of CMOS is very high, so that any form of TTL will drive CMOS without loss of fan out in the LOW state. Unfortunately, most TTL has insufficient HIGH state voltage (typically 3.5 V) to drive CMOS reliably. A pull up resistor (1 kΩ to 10 kΩ) from the output of the TTL device to the 5 V power supply will effectively pull the HIGH state level to 4.5 V or above. Alternately, DTL Hex inverters may be used between the TTL and CMOS. 9LS Low Power Schottky and 93L00 Low Power TTL/MSI utilize the unique output configuration shown in *Figure 5-8* to pull its output to $V_{CC}-V_{BC}$ or approximately 4.3 V when lightly loaded.

All Fairchild 4000B logic elements will drive a single 9LS Low Power Schottky input fan in directly. A 9LS Hex inverter such as the 9LS04 makes an excellent low cost TTL buffer with a fan out of 20 into 9LS or 5 into standard TTL. Alternately, the 4049B and 4050B Hex buffers may be used to drive a fan out of 8 into 9LS or 2 into standard TTL.

When operating CMOS at voltage higher than 5 V direct interface to TTL cannot be used. The 4104B Quad Level Translator converts TTL levels to high voltage CMOS up to 15 V. The 4049B and 4050B Hex Buffers will accept high voltage CMOS levels up to 15 V and drive 2 standard TTL loads.

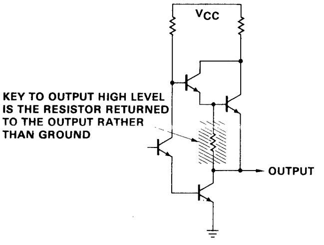


Fig. 5-8
THE 93L00 AND 9LS00 TTL FAMILIES WILL DRIVE CMOS DIRECTLY WITHOUT RESISTORS AS LONG AS THERE ARE ONLY CMOS DEVICES BEING DRIVEN FROM THE OUTPUT.

INPUT/OUTPUT CAPACITY

CMOS devices exhibit input capacities in the 1.5 to 5 pF range and output capacity in the 3 to 7 pF range.

OUTPUT IMPEDANCE

All Fairchild 4000B logic devices employ standardized output buffers. Section 7 details output characteristics. It should be noted that these impedances do not change with input pattern as do conventional CMOS gates. Buffers, analog switches and analog multiplexers employ special output configurations which are detailed in individual data sheets.

INPUT PROTECTION

The gate input to any MOS transistor appears like a small (<1 pF) very low leakage ($<10^{-12}$ A) capacitor. Without special precautions, these inputs could be electrostatically charged to a high voltage, causing a destructive breakdown of the dielectric and permanently damaging the device. Therefore, all CMOS inputs are protected by a combination of series resistor and shunt diodes. Various manufacturers have used different approaches; some use a single diode, others use two diodes, and some use a resistor with a parasitic substrate diode.

Each member of the Fairchild 4000B family utilizes a series resistor, nominally 200 Ω, and two diodes, one to V_{DD}, and the other to V_{SS} *(Figure 5-9).* The resistor is a poly-silicon "true resistor" without a parasitic substrate diode. This ensures that the input impedance is always at least 200 Ω under all biasing conditions, even when V_{DD} is short circuited to V_{SS}. A parasitic substrate diode would represent a poorly defined shunt to V_{SS} in this particular case.

The diodes exhibit typical forward voltage drops of 0.9 V at 1 mA and reverse breakdowns of 20 V for D1 and 20 V for D2. For certain special applications such as oscillators, the diodes actually conduct during normal operation. However, currents must be limited to 10 mA.

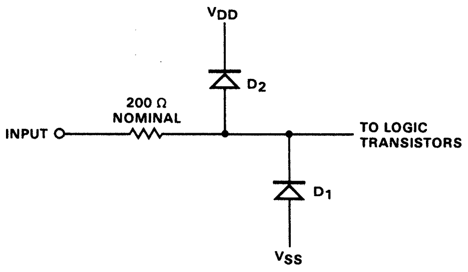


Fig. 5-9
4000B SERIES CMOS
INPUT PROTECTION CIRCUIT

HANDLING PRECAUTIONS

All MOS devices are subject to damage by large electrostatic charges. All Fairchild 4000B devices employ the input protection described in *Figure 5-9,* however, electrostatic damage can still occur. The following handling precautions should be observed.

1. All Fairchild 4000B devices are shipped in conducting foam or antistatic tubes. They should be removed for inspection or assembly using proper precautions.
2. Ionized air blowers are recommended when automatic incoming inspection is performed.
3. Fairchild 4000B devices, after removal from their shipping material, should be placed leads down on a grounded surface. Conventional cookie tins work well. Under no circumstances should they be placed in polystyrene foam or plastic trays used for shipment and handling of conventional ICs.
4. Individuals and tools should be grounded before coming in contact with 4000B devices.
5. Do not insert or remove devices in sockets with power applied. Ensure power supply transients, such as occur during power turn-on or off; do not exceed maximum ratings.
6. In the system, all unused inputs must be connected to either a logic HIGH or logic LOW level such as V_{SS}, V_{DD} or the output of a logic element.
7. After assembly on PC boards, ensure that static discharge cannot occur during storage or maintenance. Boards may be stored with their connectors surrounded with conductive foam. Board input/output pins may be protected with large value resistors (10 MΩ) to ground.
8. In extremely hostile environments, an additional series input resistor (10 to 100 kΩ) provides even better protection at a slight speed penalty.

A WORD TO THE TTL DESIGNER

Designing with CMOS is generally an easy transition and allows the designer to discard many of the old design inhibitions for new found freedoms. A few of these are:

Fan out—It is practically unlimited from a dc point of view and is restricted only by delay and rise time considerations.

Power Supply Regulation—Anything between 3 V and 15 V goes, as long as all communicating circuits are fed from the same voltage.

Ground and V_{CC} Line Drops—The currents are normally so small that there is no need for heavy supply line bussing.

V_{CC} Decoupling—It can be reduced to a few capacitors per board.

Heat Problems—They do not exist, unless an attempt is made to run CMOS very fast and from more than 10 V.

It should also be noted that there are a few warnings called for when designing with CMOS and that many of the hard-earned good engineering basics cannot be forgotten. A few of the new design challenges include:

Unused Inputs—They must be connected to V_{SS} or V_{DD} (V_{CC} or ground) lest they generate a logical "maybe". The bad TTL habit of leaving unused inputs open is definitely out.

Oscillations—Slowly rising or falling input signals can lead to oscillations and multiple triggering. A poorly regulated and decoupled power supply magnifies this problem since the CMOS input threshold varies with the supply voltage.

Timing Details—Even slow systems require a careful analysis of worst case timing delays, derated for maximum temperature, minimum supply voltage and maximum capacitive loading. Many CMOS flip-flops, registers and latches have a real hold time requirement, *i.e.,* inputs must remain stable even after the active clock edge; some require a minimum clock rise time. This hasn't been a problem with TTL. CMOS systems, even slow ones, are prone to unsuspected clock skew problems, especially since a heavily loaded clock generator can have a poor rise time.

Compatibility—The TTL designer knows that devices sold by different manufacturers under the same generic part number are electrically almost identical. Many semiconductor houses manufacture 4000-type devices with wide variations in output drive capability and speed. Sometimes even the functions are different and incompatible; two cases in point are the 1-of-10 decoder (CD4028A and MC14028) and the magnitude comparator (MC14585 and MM74C85).

Data Sheet Format—The original CMOS data sheets may appear confusing to the TTL user because a range of input voltage requirements is not specified. Rather, this information is contained in a "noise immunity" specification and is not immediately obvious.

Both TTL and CMOS tolerate deviations from the ideal LOW and HIGH input voltages. TTL is therefore specified as follows:

	MIN	MAX	
V_{IH}	2.0		V
V_{IL}		0.8	V

Any voltage below 0.8 V is considered LOW; any voltage above +2.0 V is considered HIGH. The actual threshold is somewhere in between these values, depending on manufacturing tolerances, supply voltage, and temperature.

Fairchild's 4000B CMOS is specified in a similar way. For $V_{DD} = 5$ V;

	MIN	MAX	
V_{IH}	3.5		V
V_{IL}		1.5	V

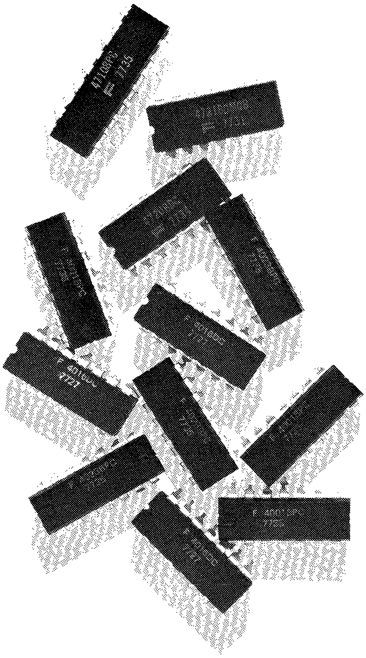
The CD4000 data sheets, on the other hand, do not call out V_{IH} and V_{IL} but specify a "noise immunity" which is somewhat arbitrarily defined relative to the appropriate supply voltage.

$$V_{NL} = V_{IL}$$

$$V_{NH} = V_{DD} - V_{IH}$$

For $V_{DD} = 5$ V, therefore
$V_{NL} = 1.5$ V min is equivalent to $V_{IL} = 1.5$ V max
$V_{NH} = 1.4$ V min is equivalent to $V_{IH} = 3.6$ V min, etc.

Systems Oriented MSI—Available CMOS circuits, especially the original 4000 series, are not as well suited for synchronous systems as are the 9300/7400 TTL families. Control polarities are inconsistent; many circuits cannot be cascaded or extended synchronously without additional gates, etc. This will improve as more good synchronous building blocks, like the 40160B are introduced.



JEDEC Industry Standard "B" Series
CMOS

Throughout first half of 1976 the CMOS vendor industry, in total, was invited to participate in the generation of a new JEDEC Industry Standard CMOS "B" Series specification. Unanimous agreement was reached and confirmed by industrywide ballot in late 1976.

This section is meant to extend knowledge of the new Industry Standard "B" Series CMOS specification to the customer and ensure that all Fairchild CMOS products meet or exceed all specifications of the new JEDEC standard.

In fact, since first introduction of the Isoplanar CMOS Family in 1973, all Fairchild CMOS products have been designed and tested to meet or exceed the more recently announced JEDEC specifications. The following is a compilation of the definitions and parametric specifications as listed in the JEDEC "Standard Specifications for description of 'B' Series CMOS devices".

(Formulated under the cognizance of th JEDEC JC-40.2 Committee on CMOS Standardization)

1. PURPOSE AND SCOPE

1. Purpose

To develop a standard of "B" Series CMOS Specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and system design by users.

1.2 Scope

This Tentative Standard covers standard specifications for description of "B" Series CMOS devices.

2. DEFINITIONS

2.1 "B" Series

"B" Series CMOS includes both buffered and unbuffered devices.

2.2 "Buffered"

A buffered output is one that has the characteristic that the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

3. STANDARD SPECIFICATIONS

3.1 Listing of Standard DC Specifications. Table 6-2 lists the standard dc specifications for "B" Series CMOS devices.

3.2 Absolute Maximum Ratings. In the maximum ratings listed below voltages are referenced to V_{SS}.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	V_{DD}	–0.5 to +18	Vdc
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.5	Vdc
DC Input Current (any one input)	I_{IN}	±10	mAdc
Storage Temperature Range	T_S	–65 to +150	°C

3.3 Recommended Operating Conditions. Recommended operating conditions are listed below.

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	V_{DD}	+3 to +15	Vdc
Operating Temperature Range	T_A		
Military-Range Devices		–55 to +125	°C
Commercial-Range Devices		–40 to +85	°C

3.4 Designation of "B" Series CMOS Devices

Those parts which have analog inputs and/or outputs shall be included in the "B" Series providing those parts' maximum ratings and logical input and output parameters conform to the "B" Series, such as (including, but not limited to):

Schmitt Triggers
Analog Switches and Multiplexers
One Shot Multivibrators and Oscillators
4511B BCD to 7-Segment Latch/Decoder/Driver
4046B Micropower Phase Lock Loop

Products that meet "B" Series specifications except that the logical outputs are not buffered and the V_{IL} and V_{IH} specifications differ from "B" series as shown in Table 6-1 shall be marked with the UB designation, such as (including, but not limited to):

4007UB
4069UB

Table 6-1. INPUT VOLTAGE LEVELS FOR "UB" PRODUCTS

PARAMETER		TEMP RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS			UNITS
					T_{LOW}	25°C	T_{HIGH}	
				V_O =				
V_{IL}	Input LOW	All	5	0.5 V or 4.5 V	1	1	1	V
(max)	Voltage		10	1.0 V or 9.0 V	2	2	2	
			15	1.5 V or 13.5 V	2.5	2.5	2.5	
				$\|I_O\| \leqslant 1\ \mu A$				
				V_O =				
V_{IH}	Input HIGH	All	5	0.5 V or 4.5 V	4	4	4	V
(min)	Voltage		10	1.0 V or 9.0 V	8	8	8	
			15	1.5 V or 13.5 V	12.5	12.5	12.5	
				$\|I_O\| \leqslant 1\ \mu A$				

Table 6-2. STANDARDIZED "B" SERIES CMOS SPECIFICATIONS

SYMBOL	PARAMETER	TEMP. RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS						UNITS
					T_{LOW}*		+25°C		T_{HIGH}**		
					MIN	MAX	MIN	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current GATES	Mil	5	$V_{IN} = V_{SS}$ or V_{DD}		0.25		0.25		7.5	µAdc
			10			0.5		0.5		15	
			15			1		1		30	
		Comm	5	All valid input combinations		1		1		7.5	µAdc
			10			2		2		15	
			15			4		4		30	
	BUFFERS, FLIP-FLOPS	Mil	5	$V_{IN} = V_{SS}$ or V_{DD}		1		1		30	µAdc
			10			2		2		60	
			15			4		4		120	
		Comm	5	All valid input combinations		4		4		30	µAdc
			10			8		8		60	
			15			16		16		120	
	MSI	Mil	5	$V_{IN} = V_{SS}$ or V_{DD}		5		5		150	µAdc
			10			10		10		300	
			15			20		20		600	
		Comm	5	All valid input combinations		20		20		150	µAdc
			10			40		40		300	
			15			80		80		600	
V_{OL}	LOW-Level Output Voltage	All	5	$V_{IN} = V_{SS}$ or V_{DD} $\lvert I_O \rvert < 1\ \mu A$		0.05		0.05		0.05	Vdc
			10			0.05		0.05		0.05	
			15			0.05		0.05		0.05	
V_{OH}	HIGH-Level Output Voltage	All	5	$V_{IN} = V_{SS}$ or V_{DD} $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95		4.95		Vdc
			10		9.95		9.95		9.95		
			15		14.95		14.95		14.95		
V_{IL}***	Input LOW Voltage	All	5	V_O = 0.5 V or 4.5 V		1.5		1.5		1.5	Vdc
			10	V_O = 1 V or 9 V		3		3		3	
			15	V_O = 1.5 V or 13.5 V $\lvert I_O \rvert < 1\ \mu A$		4		4		4	
V_{IH}***	Input HIGH Voltage	All	5	V_O = 0.5 V or 4.5 V	3.5		3.5		3.5		Vdc
			10	V_O = 1 V or 9 V	7		7		7		
			15	V_O = 1.5 V or 13.5 V $\lvert I_O \rvert < 1\ \mu A$	11		11		11		
I_{OL}	Output LOW (Sink) Current	Mil	5	V_O = 0.4 V, V_{IN} = 0 or 5 V	0.64		0.51		0.36		mAdc
			10	V_O = 0.5 V, V_{IN} = 0 or 10 V	1.6		1.3		0.9		
			15	V_O = 1.5 V, V_{IN} = 0 or 15 V	4.2		3.4		2.4		
		Comm	5	V_O = 0.4 V, V_{IN} = 0 or 5 V	0.52		0.44		0.36		mAdc
			10	V_O = 0.5 V, V_{IN} = 0 or 10 V	1.3		1.1		0.9		
			15	V_O = 1.5 V, V_{IN} = 0 or 15 V	3.6		3		2.4		
I_{OH}	Output HIGH (Source) Current	Mil	5	V_O = 4.6 V, V_{IN} = 0 or 5 V	-0.25		-0.2		-0.14		mAdc
			10	V_O = 9.5 V, V_{IN} = 0 or 10 V	-0.62		-0.5		-0.35		
			15	V_O = 13.5 V, V_{IN} = 0 or 15 V	-1.8		-1.5		-1.1		
		Comm	5	V_O = 4.6 V, V_{IN} = 0 or 5 V	-0.2		-0.16		-0.12		mAdc
			10	V_O = 9.5 V, V_{IN} = 0 or 10 V	-0.5		-0.4		-0.3		
			15	V_O = 13.5 V, V_{IN} = 0 or 15 V	-1.4		-1.2		-1		
I_{IN}	Input Current	Mil	15	V_{IN} = 0 or 15 V		±0.1		±0.1		±1	µAdc
		Comm	15	V_{IN} = 0 or 15 V		±0.3		±0.3		±1	
I_{OZ}	3-State Output Leakage Current	Mil	15	V_O = 0 V or 15 V		±0.4		±0.4		±12	µAdc
		Comm	15	V_O = 0 V or 15 V		±1.6		±1.6		±12	
C_{IN}	Input Capacitance per Unit Load	All	—	Any input				7.5			pF

*T_{LOW} = -55°C for Military Temp. Range device, -40°C for Commercial Temp. Range device

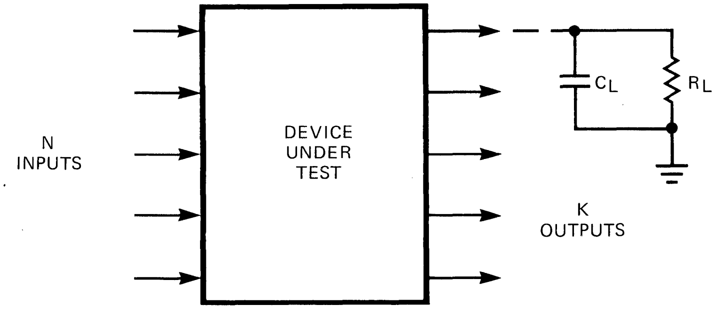
**T_{HIGH} = +125°C for Military Temp. Range device, +85°C for Commercial Temp. Range device

***V_{IL} and V_{IH} specifications apply to worst case input combinations.

3.5 Listing of Standard A C (Dynamic) Test Methods and Definitions.

Figure 6-1 shows the standard AC (Dynamic) test configuration and conditions. Dynamic electrical symbols and parametric definitions are listed in *Table 6-3. Figures 6-2* through *6-5* show standard AC characteristic test waveforms.

Fig. 6-1 TEST CONFIGURATION AND CONDITIONS



C_L = 50 pF
R_L = 200 k Ω
T_A = 25°C
V_{DD} = 5, 10, 15 V
$t_r = t_f$ = 20 ns

Table 6-3. DYNAMIC ELECTRICAL SYMBOLS AND DEFINITIONS

CHARACTERISTIC	SYMBOL	LIMITS		NOTES
		MAX.	MIN.	
PROPAGATION DELAY:				
Outputs going HIGH-to-LOW	t_{PHL}	X		
Outputs going LOW-to-HIGH	t_{PLH}	X		
OUTPUT TRANSITION TIME:				
Outputs going HIGH-to-LOW	t_{THL}	X		
Outputs going LOW-to-HIGH	t_{TLH}	X		
PULSE WIDTH — Set, Reset, Preset, Enable, Disable, Strobe, Clock	t_{WL} or t_{WH}		X	1
CLOCK INPUT FREQUENCY	F_{CL}		X	1, 2
CLOCK INPUT RISE & FALL TIME	t_rCL, t_fCL	X		
SET-UP TIME	t_{SU}		X	1
HOLD-TIME	t_H		X	1
REMOVAL TIME — Set, Reset, Preset, Enable	t_{REM}		X	1
THREE STATE DELAY TIMES:				
HIGH level-to-high impedance	t_{PHZ}	X		
High impedance-to-LOW level	t_{PZL}	X		
LOW level-to-high impedance	t_{PLZ}	X		
High impedance-to-HIGH level	t_{PZH}	X		

NOTES:

1) By placing a defining min or max in front of definition, the limits can change from min to max, or vice versa.

2) Clock input waveform should have a 50% duty cycle and be such as to cause the outputs to be switching from 10% V_{DD} to 90% V_{DD} in accordance with the device truth table.

Fig. 6-2 TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATIONAL LOGIC

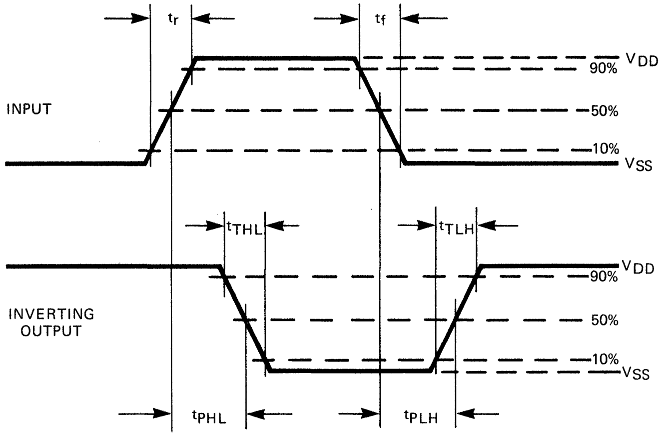
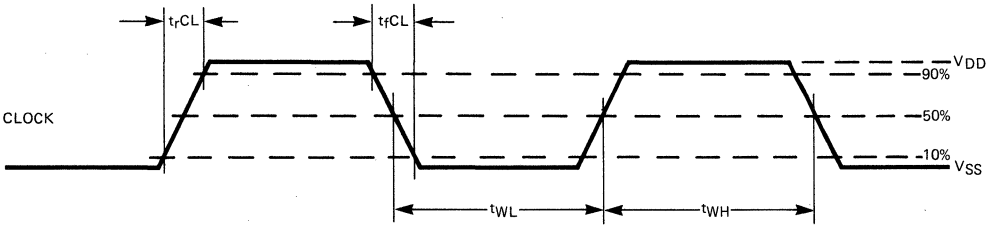


Fig. 6-3 CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH*



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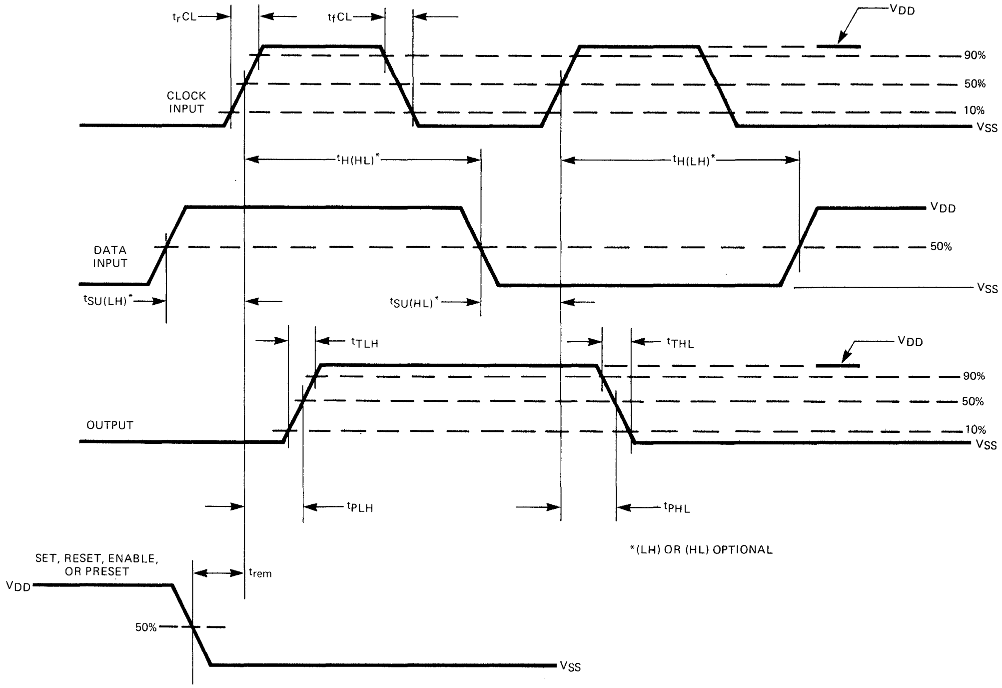
*Outputs should be switching from 10% V_{DD} to 90% V_{DD} in accordance with device truth table.

Fig. 6-4 SETUP TIMES, HOLD-TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR POSITIVE EDGE-TRIGGERED SEQUENTIAL LOGIC CIRCUITS.



*(LH) OR (HL) OPTIONAL

Fig. 6-5 3-STATE PROPAGATION DELAY WAVEFORMS

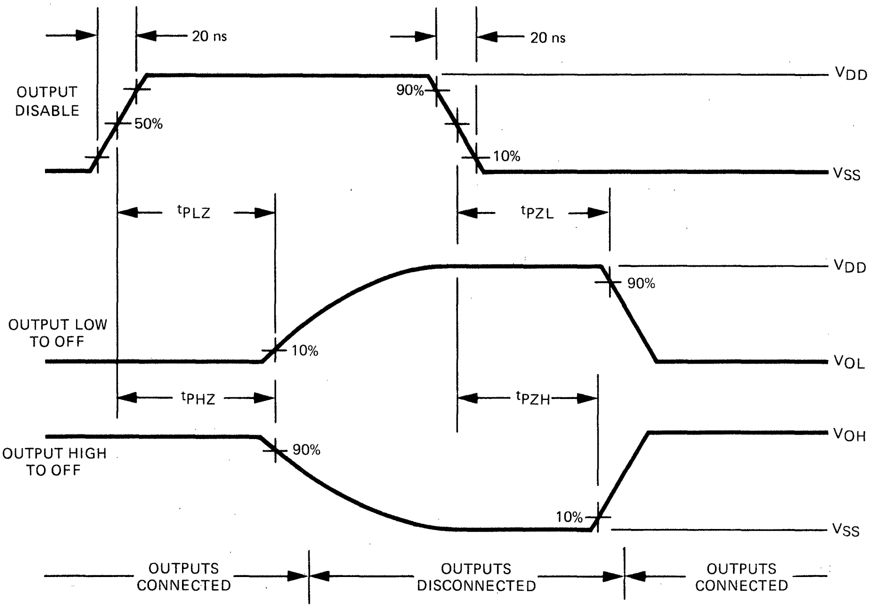
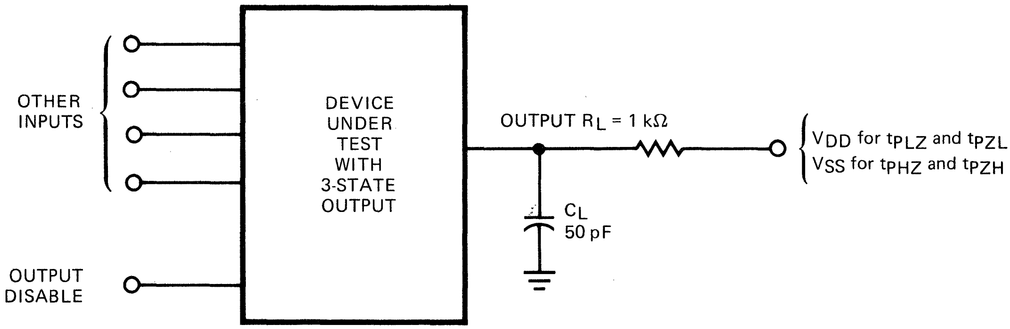


Fig. 6-6 THREE-STATE PROPAGATION DELAY TEST CIRCUIT



As defined by the above Industry Standard Specification, Fairchild offers the following devices:

4001B
4002B
4006B
4007UB
4008B
4011B
4012B
4013B
4014B
4015B
4016B
4017B
4019B
4020B
4021B
4022B
4023B
4024B
4025B
4027B
4028B
4029B
4030B
4031B
4034B
4035B
4040B
4042B
4044B
4045B
4046B
4047B
4049B
4050B
4051B
4052B
4053B
4066B
4067B
4069UB
4070B
4071B
4076B
4081B
4086B
4093B
4104B
4510B
4511B
4512B
4514B
4515B
4516B
4518B
4520B
4521B
4522B
4526B
4527B
4528B
4539B
4543B
4555B
4557B
4702B
4703B
4710B
4720B
4722B
4723B
4724B
4725B
4727B
4731B
4734B
4741B
40085B
40097B
40098B
40161B
40163B
40174B
40175B
40193B
6508B

To order Fairchild Industry Standard "B" Series CMOS . . .

ORDER AND PACKAGE INFORMATION

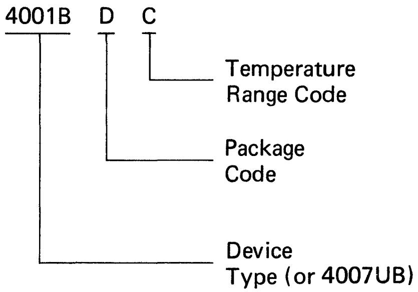
Fairchild integrated circuits may be ordered using a simplified purchasing code where the package style and temperature range are defined as follows:

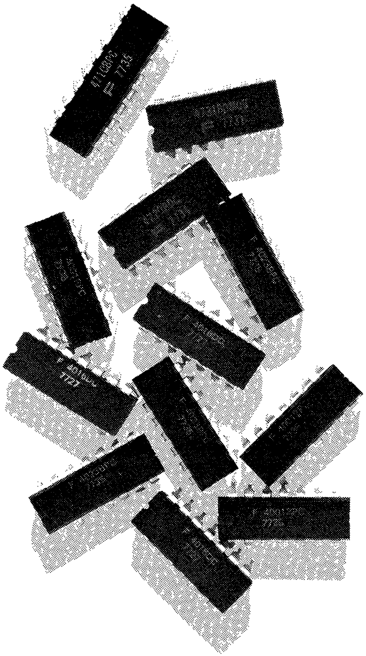
PACKAGE CODE

D = Dual In-line — Ceramic (hermetic)
P = Dual In-line — Plastic
F = Flatpak

TEMPERATURE RANGE CODE

C = Commercial
−40°C to +85°C
M = Military
−55°C to +125°C





FAIRCHILD 4000B SERIES
CMOS FAMILY CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Non-operating) above which useful life may be impaired. All voltages are referenced to V_{SS}.

Supply Voltage V_{DD}	−0.5 to 18 V
Voltage on any Input	−0.5 to V_{DD} +0.5 V
Current into any Input	±10 mA
Maximum Power Dissipation	400 mW
Storage Temperature	−65°C to 150°C
Lead Temperature (Soldering, 10 s)	300°C

RECOMMENDED OPERATING CONDITIONS

Fairchild CMOS will operate over a recommended V_{DD} power supply range of 3 to 15 V, as referenced to V_{SS} (usually ground). Parametric limits are guaranteed for V_{DD} equal to 5, 10 and 15 V. Where low power dissipation is required, the lowest power supply voltage, consistent with required speed, should be used. For larger noise immunity, higher power supply voltages should be specified. Because of its wide operating range, power supply regulation and filtering are less critical than with other types of logic. The lower limit of supply regulation is 3 V, or as determined by required system speed and/or noise immunity or interface to other logic. The recommended upper limit is 15 V or as determined by power dissipation constraints or interface to other logic.

Unused inputs must be connected to V_{DD}, V_{SS} or another input.

Care should be used in handling CMOS devices; large static charges may damage the device.

Operating temperature ranges are −40°C to +85°C for Commercial and −55°C to +125°C for Military.

PARAMETER	4000BXC			4000BXM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage, V_{DD}	3		15	3		15	V
Operating Free Air Temperature Range	−40	+25	+85	−55	+25	+125	°C

X = Package Type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Ordering Information section.

FAIRCHILD 4000B SERIES CMOS FAMILY CHARACTERISTICS

DC CHARACTERISTICS FOR THE 4000B SERIES CMOS FAMILY – Parametric Limits listed below are guaranteed for the entire Fairchild CMOS Family unless otherwise specified on the individual data sheets.

DC CHARACTERISTICS: V_{DD} = 5 V, V_{SS} = 0 V

SYMBOL	PARAMETER			LIMITS			UNITS	TEMP	TEST CONDITIONS
				MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage			3.5			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage					1.5	V	All	Guaranteed Input Low Voltage
V_{OH}	Output HIGH Voltage			4.95			V	Min, 25°C	$I_{OH} < 1$ µA, Inputs at 0 or 5 V per the Logic Function or Truth Table
				4.95				MAX	
				4.5			V	All	$I_{OH} < 1$ µA, Inputs at 1.5 or 3.5 V
V_{OL}	Output LOW Voltage					0.05	V	MIN, 25°C	$I_{OL} < 1$ µA, Inputs at 0 or 5 V per the Logic Function or Truth Table
						0.05		MAX	
						0.5	V	All	$I_{OL} < 1$ µA, Inputs at 1.5 or 3.5 V
I_{OH}	Output HIGH Current			-0.63			mA	MIN, 25°C	V_{OUT} = 4.6 V Inputs at 0 or 5 V per the Logic Function or Truth Table
				-0.36				MAX	
I_{OL}	Output LOW Current			1			mA	MIN,	V_{OUT} = 0.4 V
				0.8				25°C	
				0.4				MAX	
C_{IN}	Input Capacitance Per Unit Load					7.5	pF	25°C	Any Input
I_{DD}	Quiescent Power Supply Current	Gates	XC			1	µA	MIN, 25°C	All Inputs at 0 V or V_{DD} for all Valid Input Combinations
						7.5		MAX	
			XM			0.25	µA	MIN, 25°C	
						7.5		MAX	
		Buffers and Flip-Flops	XC			4	µA	MIN, 25°C	
						30		MAX	
			XM			1	µA	MIN, 25°C	
						30		MAX	
		MSI	XC			20	µA	MIN, 25°C	
						150		MAX	
			XM			5	µA	MIN, 25°C	
						150		MAX	

DC CHARACTERISTICS: $V_{DD} = 10$ V, $V_{SS} = 0$ V

SYMBOL	PARAMETER			LIMITS			UNITS	TEMP	TEST CONDITIONS
				MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage			7			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage					3	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage			9.95			V	MIN, 25°C	$I_{OH} < 1$ µA, Inputs at 0 V or 10 V per the Logic Function or Truth Table
				9.95				MAX	
				9			V	All	$I_{OH} < 1$ µA, Inputs at 3 or 7 V
V_{OL}	Output LOW Voltage					0.05	V	MIN, 25°C	$I_{OL} < 1$ µA, Inputs at 0 or 10 V per the Logic Function or Truth Table
						0.05		MAX	
						1	V	All	$I_{OL} < 1$ µ A, Inputs at 3 or 7 V
I_{OH}	Output HIGH Current			-1.4			mA	MIN, 25°C	$V_{OUT} = 9.5$ V Inputs at 0 or 10 V per the Logic Function or Truth Table
				-0.8				MAX	
I_{OL}	Output LOW Current			2.6			mA	MIN,	$V_{OUT} = 0.5$ V Inputs at 0 or 10 V per the Logic Function or Truth Table
				2				25°C	
				1.2				MAX	
C_{IN}	Input Capacitance Per Unit Load					7.5	pF	25°C	Any Input
I_{DD}	Quiescent Power Supply Current	Gates	XC			2	µA	MIN, 25°C	All Inputs at 0 V or V_{DD} for All Valid Input Combinations
						15		MAX	
			XM			0.5	µA	MIN, 25°C	
						15		MAX	
		Buffers, Flip-Flops	XC			8	µA	MIN, 25°C	
						60		MAX	
			XM			2	µA	MIN, 25°C	
						60		MAX	
		MSI	XC			40	µA	MIN, 25°C	
						300		MAX	
			XM			10	µA	MIN, 25°C	
						300		MAX	

FAIRCHILD 4000B SERIES CMOS FAMILY CHARACTERISTICS

DC CHARACTERISTICS: $V_{DD} = 15\ V$, $V_{SS} = 0\ V$

SYMBOL	PARAMETER			LIMITS			UNITS	TEMP	TEST CONDITIONS	
				MIN	TYP	MAX				
V_{IH}	Input HIGH Voltage			11			V	All	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage					4	V	All	Guaranteed Input LOW Voltage	
V_{OH}	Output HIGH Voltage			14.95			V	MIN, 25°C	$I_{OH} < 1\ \mu A$, Inputs at 0 or 15 V per the Logic Function or Truth Table	
				14.95				MAX		
				13.5			V	All	$I_{OH} < 1\ \mu A$, Inputs at 4 or 11 V	
V_{OL}	Output LOW Voltage					0.05	V	MIN, 25°C	$I_{OL} < 1\ \mu A$, Inputs at 0 or 15 V per the Logic Function or Truth Table	
						0.05		MAX		
						1.5	V	All	$I_{OL} < 1\ \mu A$, Inputs at 4 or 11 V	
I_{IN}	Input Current		XC			0.3	µA	MIN, 25°C	Lead under test at 0 or 15 V All other Inputs Simultaneously at 0 or 15 V	
						1		MAX		
			XM			0.1	µA	MIN, 25°C		
						1		MAX		
I_{OH}	Output HIGH Current			-4.5			mA	MIN, 25°C	V_{OUT} = 13.5 V	Inputs at 0 or 15 V per the Logic Function or Truth Table
				-2.7				MAX		
I_{OL}	Output LOW Current			7.5			mA	MIN, 25°C	V_{OUT} = 1.5 V	
				4.5				MAX		
C_{IN}	Input Capacitance Per Unit Load					7.5	pF	25°C	Any Input	
I_{DD}	Quiescent Power Supply Current	Gates	XC			4	µA	MIN, 25°C	All Inputs at 0 V or V_{DD} for all Valid Input Conditions	
						30		MAX		
			XM			1	µA	MIN, 25°C		
						30		MAX		
		Buffers, Flip-Flops	XC			16	µA	MIN, 25°C		
						120		MAX		
			XM			4	µA	MIN, 25°C		
						120		MAX		
		MSI	XC			80	µA	MIN, 25°C		
						600		MAX		
			XM			20	µA	MIN, 25°C		
						600		MAX		

TYPICAL FAIRCHILD 4000B SERIES CHARACTERISTICS

Fig. 7-1
POSITIVE-GOING PROPAGATION DELAY VERSUS SUPPLY VOLTAGE

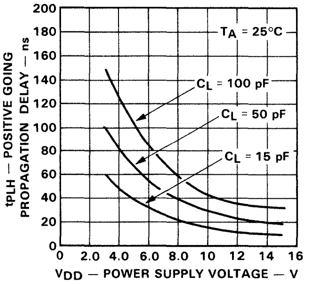


Fig. 7-2
NEGATIVE-GOING PROPAGATION DELAY VERSUS SUPPLY VOLTAGE

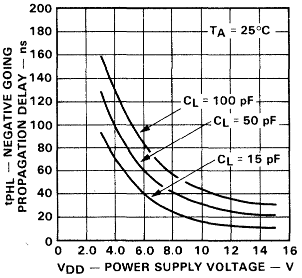


Fig. 7-3
POSITIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE

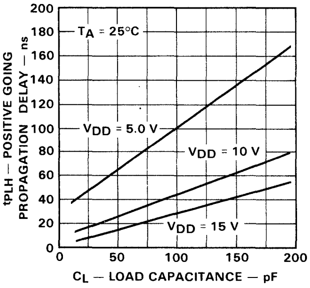


Fig. 7-4
NEGATIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE

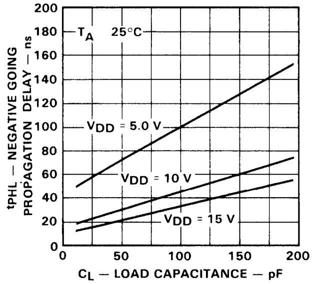


Fig. 7-5
VOLTAGE TRANSFER CHARACTERISTICS OVER −55°C TO +125°C RANGE

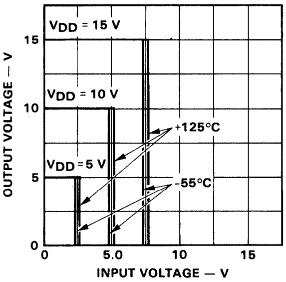


Fig. 7-6
GATE POWER DISSIPATION VERSUS FREQUENCY

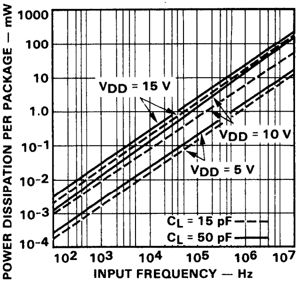


Fig. 7-7
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 5.0 V

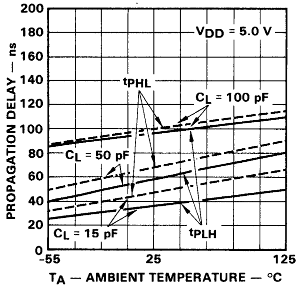


Fig. 7-8
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 10 V

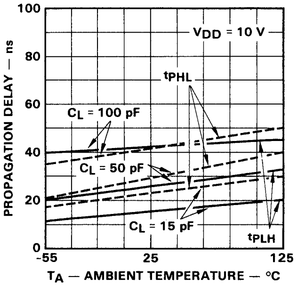


Fig. 7-9
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 15 V

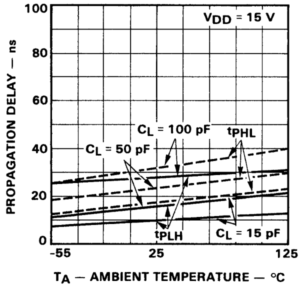


Fig. 7-10
p-CHANNEL DRAIN CHARACTERISTICS

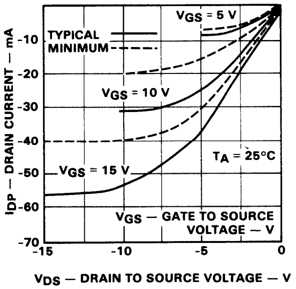


Fig. 7-11
n-CHANNEL DRAIN CHARACTERISTICS

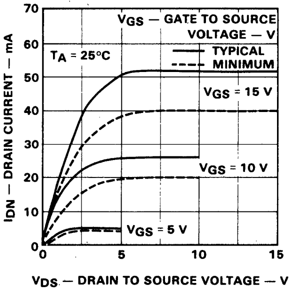


Fig. 7-12
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE

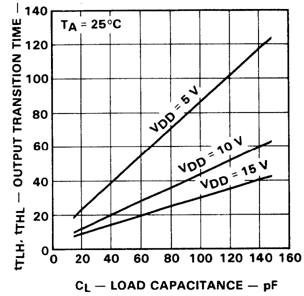
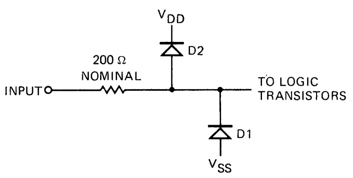


Fig. 7-13
INPUT PROTECTION CIRCUIT



INPUT CIRCUITRY

All inputs are protected by the network of Figure 7-13; a series input resistor plus diodes D1 and D2 clamp input voltages between V_{SS} and V_{DD}. Forward conduction of these diodes is typically 0.9 V at 1 mA. When V_{SS} or V_{DD} is not connected, avalanche breakdown of the diodes limit input voltage; D1 typically breaks down at 20 V, D2 at 20 V. In normal logic operation the diodes never conduct, but for certain special applications such as oscillators, circuit operation may actually depend on diode conduction. Operation in this mode is permissible so long as input currents do not exceed 10 mA.

Input capacitance is typically 5 pF across temperature for any input.

DEFINITION OF SYMBOLS AND TERMS

CURRENTS — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

I_{IN} — (Input Current) — The current flowing into a device at specified input voltage and V_{DD}.

I_{OH} — (Output HIGH Current) — The drive current flowing out of the device at specified HIGH output voltage and V_{DD}.

I_{OL} — (Output LOW Current) — The drive current flowing into the device at specified LOW output voltage and V_{DD}.

I_{DD} — (Quiescent Power Supply Current) — The current flowing into the V_{DD} lead at specified input and V_{DD} conditions.

I_{OZH} — (Output OFF Current HIGH) — The leakage current flowing into the output of a 3-state device in the "OFF" state at a specified HIGH output voltage and V_{DD}.

I_{OZL} — (Output OFF Current LOW) — The leakage current flowing out of a 3-state device in the "OFF" state at a specified HIGH output voltage and V_{DD}.

I_{IL} — (Input Current LOW) — The current flowing into a device at a specified LOW level input voltage and a specified V_{DD}.

I_{IH} — (Input Current HIGH) — The current flowing into a device at a specified HIGH level input voltage and a specified V_{DD}.

I_{DDL} — (Quiescent Power Supply Current LOW) — The current flowing into the V_{DD} lead with a specified LOW level input voltage on all inputs and specified V_{DD} conditions.

I_{DDH} — (Quiescent Power Supply Current HIGH) — The current flowing into the V_{DD} lead with a specified HIGH level input voltage on all inputs and specified V_{DD} conditions.

I_Z — (OFF State Leakage Current) — The leakage current flowing into the output of a 3-state device in the "OFF" state at a specified output voltage and V_{DD}.

VOLTAGES — All voltages are referenced to V_{SS} (or V_{EE}) which is the most negative potential applied to the device.

V_{DD} — (Drain Voltage) — The most positive potential on the device.

V_{IH} — (Input HIGH Voltage) — The range of input voltages that represents a logic HIGH level in the system.

V_{IL} — (Input LOW Voltage) — The range of input voltages that represents a logic LOW level in the system.

V_{IH} (min) — (Minimum Input HIGH Voltage) — The minimum allowed input HIGH level in a logic system.

V_{IL} (max) — (Maximum Input LOW Voltage) — The maximum allowed input LOW level in a system.

V_{OH} — (Output HIGH Voltage) — The range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} — (Output LOW Voltage) — The range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

V_{SS} — (Source Voltage) — For a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages. Typically ground.

V_{EE} — (Source Voltage) — One of two (V_{SS} and V_{EE}) negative power supplies. For a device with dual negative power supplies, the most negative power supply used as a reference level for other voltages.

ANALOG TERMS

R_{ON} — (ON Resistance) — The effective "ON" state resistance of an analog transmission gate, at specified input voltage, output load and V_{DD}.

ΔR_{ON} — ("Δ " ON Resistance) — The difference in effective "ON" resistance between any two transmission gates of an analog device at specified input voltage, output load and V_{DD}.

AC SWITCHING PARAMETERS

f_{MAX} — (Toggle Frequency/Operating Frequency) — The maximum rate at which clock pulses may be applied to a sequential circuit with the output of the circuit changing between 10% of V_{DD} and 90% of V_{DD}. Above this frequency the device may cease to function. See Figure 7-15.

t_{PLH} — (Propagation Delay Time) — The time between the specified reference points, normally 50% points on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level. See Figure 7-14.

t_{PHL} — (Propagation Delay Time) — The time between the specified reference points, normally 50% points on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level. See Figure 7-14.

t_{TLH} — (Transition Time, LOW to HIGH) — The time between two specified reference points on a waveform, normally 10% to 90% of V_{DD}, which is changing from LOW to HIGH. See Figure 7-14.

t_{THL} — (Transition Time, HIGH to LOW) — The time between two specified reference points on a waveform, normally 90% to 10% of V_{DD}, which is changing from HIGH to LOW. See Figure 7-14.

t_W — (Pulse Width) — The time between 50% amplitude points on the leading and trailing edges of pulse.

t_h — (Hold Time) — The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s — (Set-up Time) — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} — (3-State Output Disable Time, HIGH to Z) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing a 0.1 V_{DD} drop on the Output voltage waveform of a 3-state device, with the output changing from the defined HIGH level to a high impedance OFF state.

t_{PLZ} — (3-State Output Disable Time, LOW to Z) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing a 0.1 V_{DD} rise on the Output voltage waveform of a 3-state device, with the output changing from the defined LOW level to a high impedance OFF state.

t_{PZH} — (3-State Output Enable Time, Z to HIGH) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing 0.5 V_{DD} on the Output voltage waveform of a 3-state device, with the output changing from a high impedance OFF state to the defined HIGH level.

t_{PZL} — (3-State Output Enable Time, Z to LOW) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing 0.5 V_{DD} on the Output voltage waveform of a 3-state device, with the output changing from a high impedance OFF state to the defined LOW level.

t_{rec} — (Recovery Time) — The time between the end of an overriding asynchronous input, typically a Clear or Reset input, and the earliest allowable beginning of a synchronous control input, typically a Clock input, normally measured at 50% points on both input voltage waveforms.

t_{CW} — (Clock Period) – The time between 50% amplitude points on the leading edges of a clock pulse.

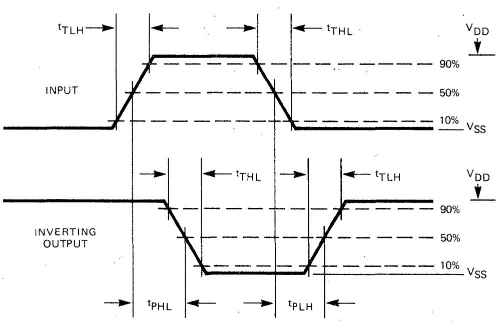


Fig. 7-14. Propagation Delay, Transition Time

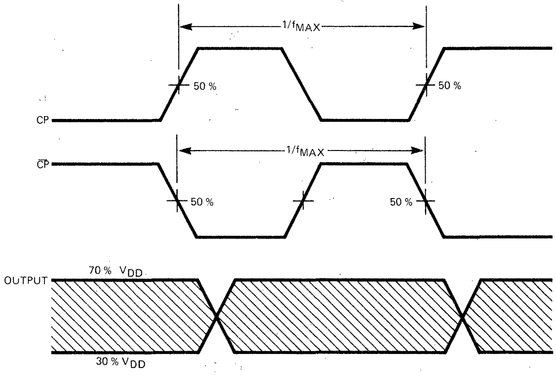


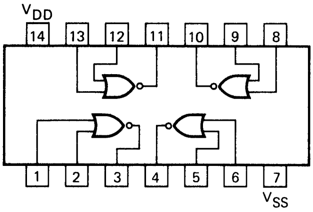
Fig. 7-15. Maximum Operating Frequency

4001B 4002B

QUAD 2-INPUT NOR GATE • DUAL 4-INPUT NOR GATE

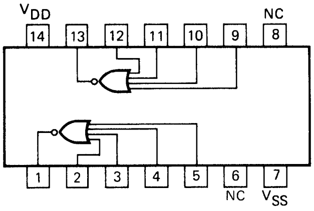
DESCRIPTION – These CMOS logic elements provide the positive input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

4001B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-line Package.

4002B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			See Note 1
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4001B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				See Note 2
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		60	110		25	60		20	48	ns	C_L = 50 pF,
t_{PHL}			60	110		25	60		20	48	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		60	135		30	70		20	45	ns	Input Transition
t_{THL}			60	135		30	70		20	45	ns	Times ⩽ 20 ns

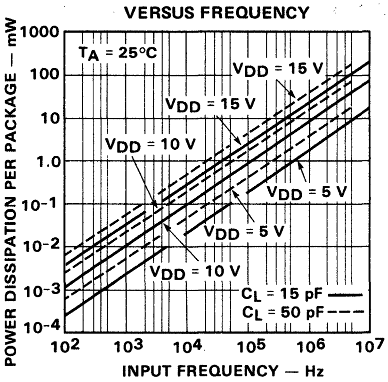
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4002B only

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				See Note 2
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		65	110		30	60		20	48	ns	C_L = 50 pF,
t_{PHL}			70	110		30	60		23	48	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		75	135		40	70		30	45	ns	Input Transition
t_{THL}			60	135		23	70		15	45	ns	Times ⩽ 20 ns

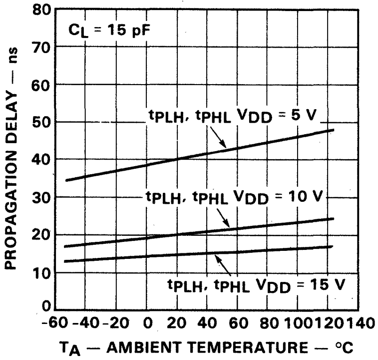
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

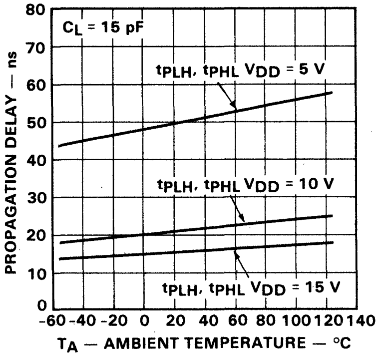
4001B AND 4002B POWER DISSIPATION VERSUS FREQUENCY



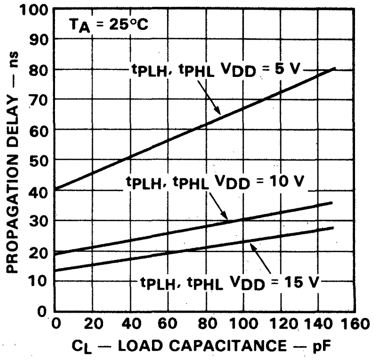
4001B PROPAGATION DELAY VERSUS TEMPERATURE



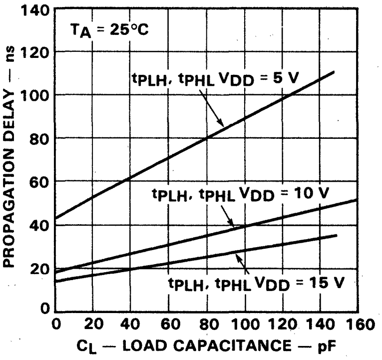
4002B PROPAGATION DELAY VERSUS TEMPERATURE



4001B PROPAGATION DELAY VERSUS LOAD CAPACITANCE



4002B PROPAGATION DELAY VERSUS LOAD CAPACITANCE



4006B

18-STAGE STATIC SHIFT REGISTER

DESCRIPTION — The 4006B is an 18-stage Shift Register arranged as two 4-stage and two 5-stage shift regsiters with a common Clock Input ($\overline{CP}$). The two 4-stage shift registers, each have a Data Input (D_a, D_b) and a Data Output (Q_{3a}, Q_{3b}); the two 5-stage shift registers each have a Data Input (D_c, D_d) and Data Outputs from the fourth and fifth stages (Q_{3c}, Q_{4c}, Q_{3d}, Q_{4d}).

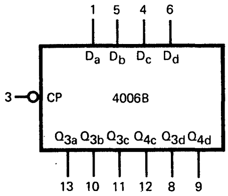
The registers can be operated in parallel or interconnected to form a single shift register of up to 18 bits. Data is shifted into the first register position of each register from the Data Inputs (D_a-D_d) and all the data in each register is shifted one position to the right on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$).

- **CLOCK EDGE-TRIGGERED ON A HIGH-TO-LOW TRANSITION**
- **CASCADABLE**
- **SERIAL-TO-SERIAL DATA TRANSFER**

PIN NAMES

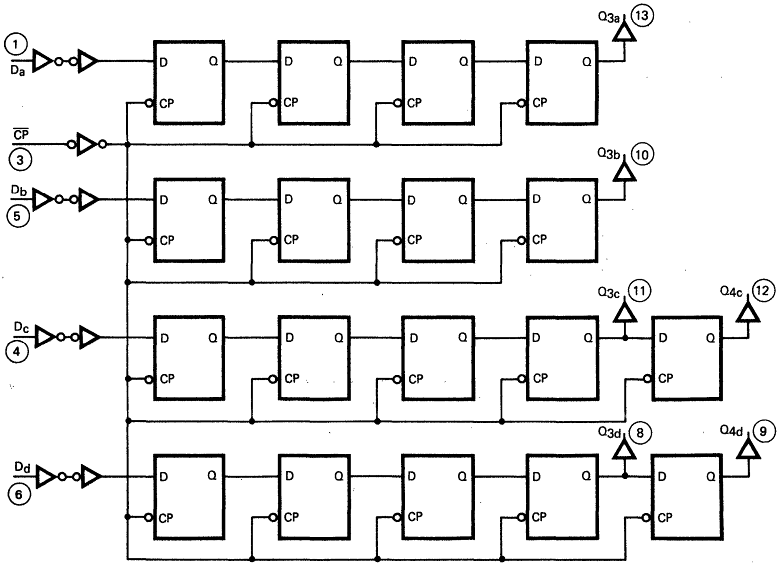
D_a-D_d	Data Inputs
$\overline{CP}$	Clock Input (H→L Edge-Triggered)
Q_{3a}-Q_{3d}, Q_{4c}, Q_{4d}	Data Outputs

LOGIC SYMBOL



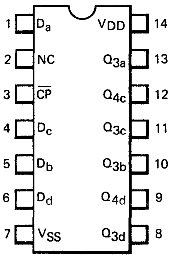
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pin 2

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pin 2
○ = Pin Number

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

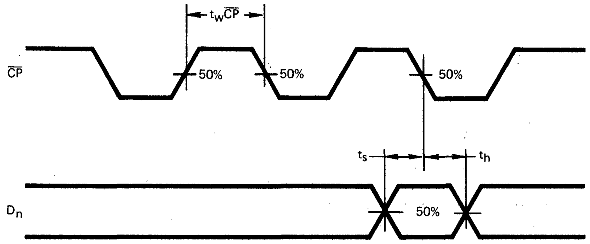
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to any Q_n		90	200		39	100		30	80	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			90	200		35	100		25	80		
t_{TLH}	Output Transition Time		60	135		30	75		20	45	ns	
t_{THL}			60	135		30	75		20	45		
$t_w\overline{CP}$	$\overline{CP}$ Minimum Pulse Width	100	50		50	20		40	13		ns	
t_s	Set-Up Time, D_n to $\overline{CP}$	30	12		15	5		15	5		ns	
t_h	Hold Time, D_n to $\overline{CP}$	30	1		15	4		10	4			
f_{MAX}	Maximum Input Clock Frequency (Note 3)	8	19		15	30		18	36		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, D_n TO $\overline{CP}$

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

4007UB

DUAL COMPLEMENTARY PAIR PLUS INVERTER

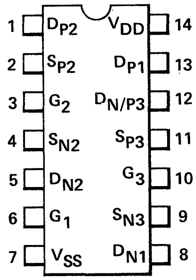
DESCRIPTION – The 4007UB is a Dual Complementary Pair and an Inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors. For proper operation $V_{SS} \leqslant V_1 \leqslant V_{DD}$.

- **INPUT DIODE PROTECTION ON ALL INPUTS**
- **DRAINS AND SOURCES TO N- AND P-CHANNEL TRANSISTORS AVAILABLE**

PIN NAMES

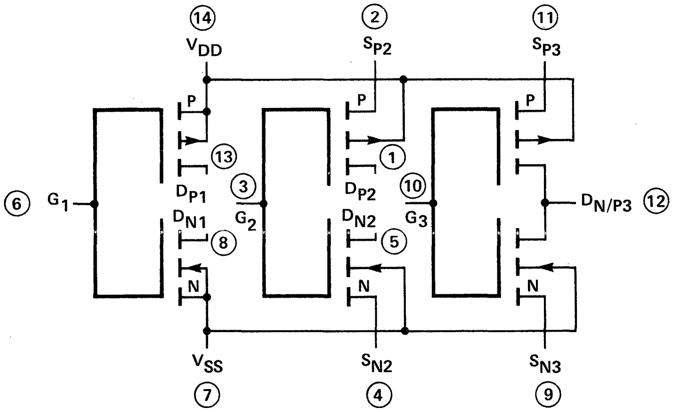
S_{P2}, S_{P3}	Source Connection to Second and Third p-channel Transistors
D_{P1}, D_{P2}	Drain Connection from the First and Second p-channel Transistors
D_{N1}, D_{N2}	Drain Connection from the First and Second n-channel Transistors
S_{N2}, S_{N3}	Source Connection to the Second and Third n-channel Transistors
$D_{N/P3}$	Common Connection to the Third p-channel and n-channel Transistor Drains
G_1-G_3	Gate Connection to n- and p-channel Transistors 1, 2 and 3

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package,

LOGIC SYMBOL



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	µA	MIN, 25°C	
					7.5			15			30		MAX	

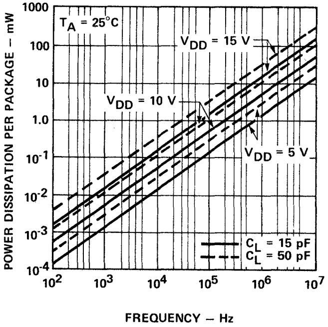
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		42	85		23	40		18	32	ns	C_L = 50 pF,
t_{PHL}			42	85		23	40		18	32	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		65	135		30	70		25	45	ns	Input Transition
t_{THL}			65	135		30	70		25	45	ns	Times ≤ 20 ns

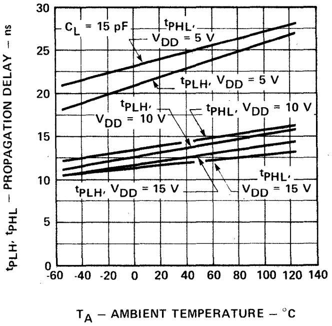
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

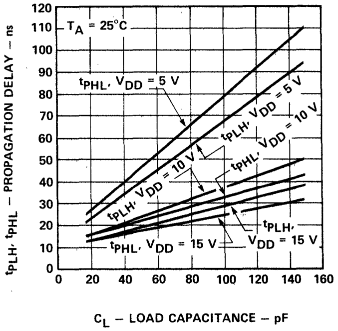
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



4008B

4-BIT BINARY FULL ADDER

DESCRIPTION – The 4008B is a 4-Bit Binary Full Adder with two 4-bit Data Inputs (A_0–A_3, B_0–B_3); a Carry Input (C_0), four Sum Outputs (S_0-S_3) and a Carry Output (C_4).

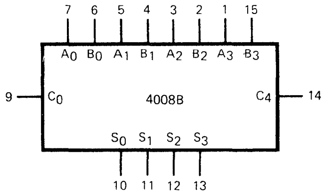
The 4008B uses full lookahead across 4-bits to generate the Carry Output (C_4). This minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

- **CARRY LOOKAHEAD BUFFERED OUTPUT**
- **EASILY CASCADED**

PIN NAMES

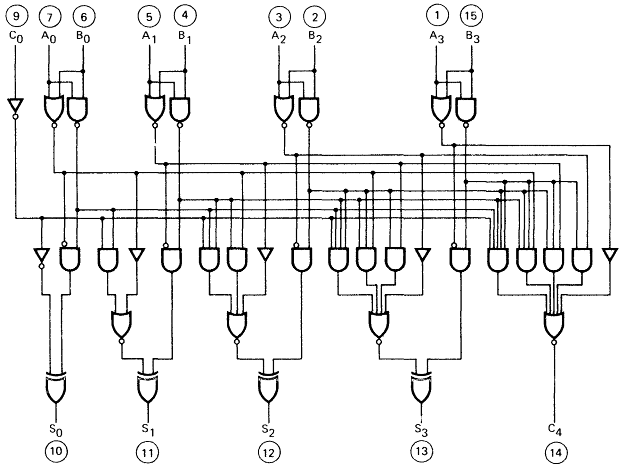
A_0-A_3, B_0-B_3	Data Inputs
C_0	Carry Input
S_0-S_3	Sum Outputs
C_4	Carry Output

LOGIC SYMBOL



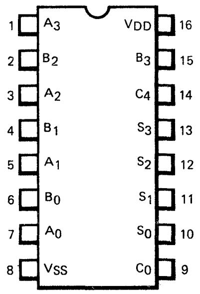
V_{DD} = Pin 16
V_{SS} = Pin 8

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

CONNECTION DIAGRAM
DIP(TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					100			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (see Note 2)

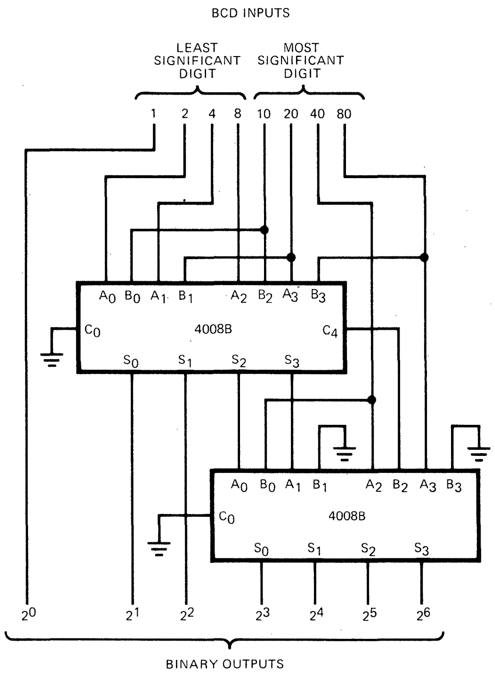
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, A_n, B_n to S_n		150	300		60	140		50	110	ns	C_L = 50 pF, R_L = 200 kΩ, Input Transition Times ≤ 20 ns
t_{PHL}			150	300		60	140		50	110	ns	
t_{PLH}	Propagation Delay, A_n, B_n to C_4		138	275		63	130		50	100	ns	
t_{PHL}			138	275		63	130		50	100	ns	
t_{PLH}	Propagation Delay, C_o to S_n		115	250		69	115		52	90	ns	
t_{PHL}			123	250		69	115		52	90	ns	
t_{PLH}	Propagation Delay, C_o to C_4		72	200		28	95		23	75	ns	
t_{PHL}			95	200		28	95		23	75	ns	
t_{TLH}	Output Transition Time		60	135		30	75		20	45	ns	
t_{THL}			60	135		30	75		20	45	ns	

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

APPLICATION

A 2-DIGIT BCD TO 7-BIT BINARY DECODER USING THE 4008B



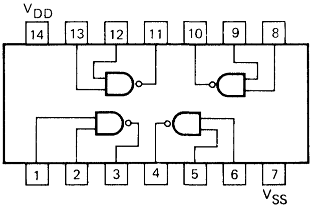
4011B • 4012B

4011B QUAD
2-INPUT NAND GATE

4012B DUAL
4-INPUT NAND GATE

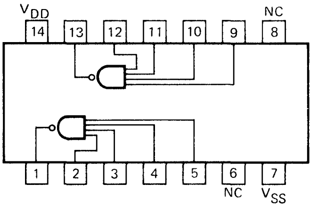
DESCRIPTION – These CMOS logic elements provide the positive input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

4011B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-line Package.

4012B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS See Note 1
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	µA	MIN, 25°C	
					7.5			15			30		MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4011B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS See Note 2
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		60	110		25	60		20	48	ns	C_L = 50 pF,
t_{PHL}			60	110		25	60		20	48	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		60	135		30	70		20	45	ns	Input Transition
t_{THL}			60	135		30	70		20	45	ns	Times ≤ 20 ns

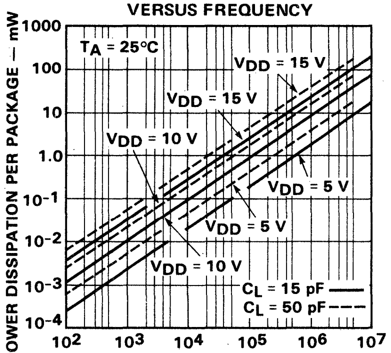
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4012B only

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS See Note 2
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		73	110		33	60		24	48	ns	C_L = 50 pF,
t_{PHL}			85	110		31	60		20	48	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		76	135		37	70		27	45	ns	Input Transition
t_{THL}			67	135		25	70		17	45	ns	Times ≤ 20 ns

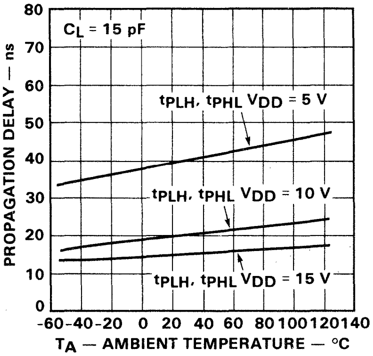
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

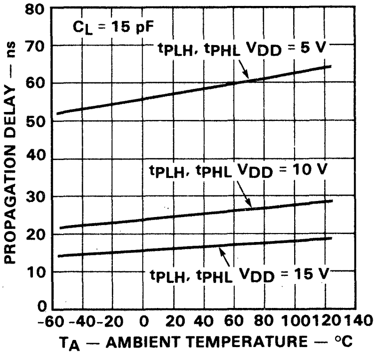
4011B AND 4012B
POWER DISSIPATION
VERSUS FREQUENCY



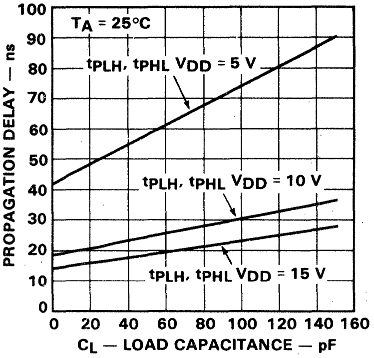
4011B
PROPAGATION DELAY
VERSUS TEMPERATURE



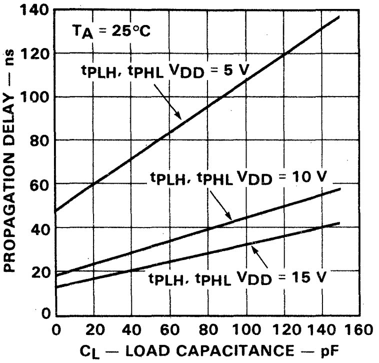
4012B
PROPAGATION DELAY
VERSUS TEMPERATURE



4011B
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



4012B
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



4013B
DUAL D FLIP-FLOP

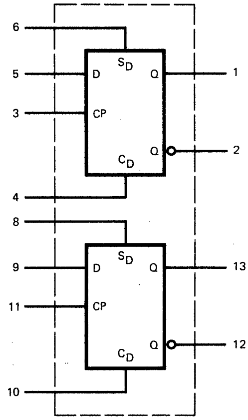
DESCRIPTION – The 4013B is a CMOS Dual D Flip-Flop which is edge-triggered and features independent Set Direct, Clear Direct, and Clock inputs. Data is accepted when the Clock is LOW and transferred to the output on the positive-going edge of the Clock. The active HIGH asynchronous Clear Direct (C_D) and Set Direct (S_D) are independent and override the D or Clock inputs. The outputs are buffered for best system performance.

PIN NAMES

D	Data Input
CP	Clock Input (L→H Edge-Triggered)
S_D	Asynchronous Set Direct Input (Active HIGH)
C_D	Asynchronous Clear Direct Input (Active HIGH)
Q	True Output
$\overline{Q}$	Complement Output

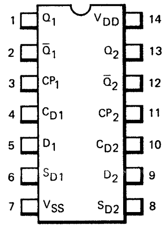
LOGIC SYMBOL

4013B



V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

4013B TRUTH TABLES

ASYNCHRONOUS INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
L	H	L	H
H	L	H	L
H	H	H	H

L = LOW Level
H = HIGH Level
↑ = Positive-Going Transition
Q_{n+1} = State After Clock Positive Transition

SYNCHRONOUS INPUTS		OUTPUTS	
CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
↑	L	L	H
↑	H	H	L

Conditions: $S_D = C_D$ = LOW

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			4			8			16	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					30			60			120		MAX	
		XM			1			2			4	µA	MIN, 25°C	
					30			60			120		MAX	

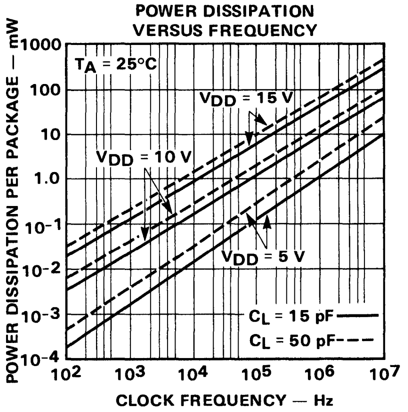
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

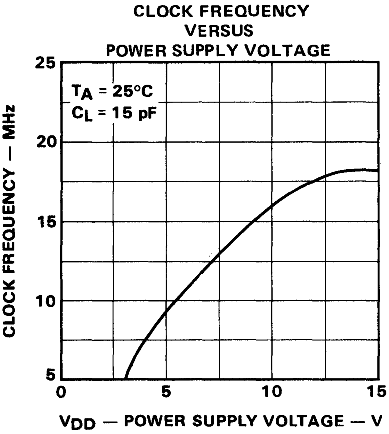
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP TO Q, $\overline{Q}$		95	200		38	90		29	72	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			95	200		38	90		29	72	ns	
t_{PLH}	Propagation Delay, S_D or C_D to $\overline{Q}$		130	225		45	110		32	88	ns	
t_{PHL}			75	225		35	110		20	88	ns	
t_{PLH}	Propagation Delay, S_D or C_D to Q		115	225		50	110		35	88	ns	
t_{PHL}			115	225		50	110		35	88	ns	
t_{TLH}	Output Transition Time		60	135		30	70		20	45	ns	
t_{THL}			60	135		30	70		20	45	ns	
t_s	Set-Up Time, Data to CP	60	30		30	15		24	8		ns	
t_h	Hold Time, Data to CP	0	-25		0	-12		0	-6		ns	
$t_wCP(L)$	Minimum Clock Pulse Width	100	55		55	30		44	18		ns	
$t_wS_D(H)$	Minimum S_D Pulse Width	60	30		30	15		24	10		ns	
$t_wC_D(H)$	Minimum C_D Pulse Width	60	30		30	15		24	10		ns	
$t_{rec}S_D$	Recovery Time for S_D	20	8		10	2		8	2		ns	
$t_{rec}C_D$	Recovery Time for C_D	30	15		15	7		12	6		ns	
f_{MAX}	Maximum CP Frequency (Note 2)	5	8		8	16		9	19		MHz	

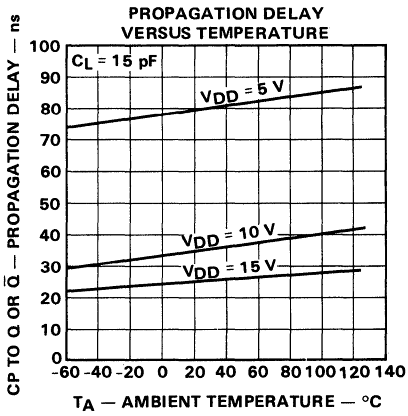
NOTES:

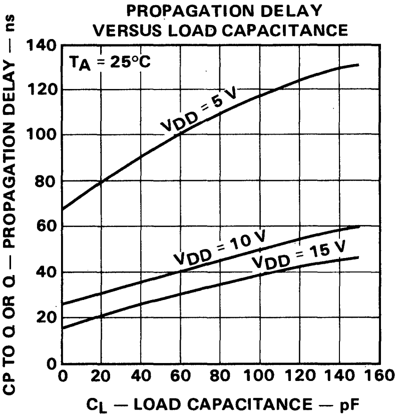
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

TYPICAL ELECTRICAL CHARACTERISTICS

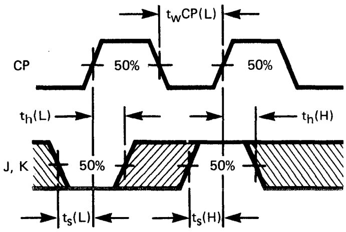

POWER DISSIPATION VERSUS FREQUENCY


CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE

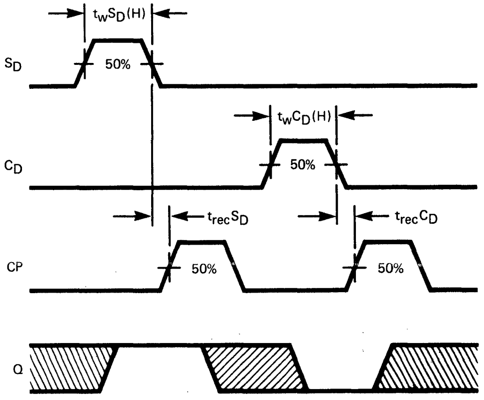

PROPAGATION DELAY VERSUS TEMPERATURE


PROPAGATION DELAY VERSUS LOAD CAPACITANCE

WAVEFORMS



SET-UP TIMES, HOLD TIMES, AND MINIMUM CLOCK PULSE WIDTH



RECOVERY TIME FOR S_D, RECOVERY TIME FOR C_D, MINIMUM S_D PULSE WIDTH, AND MINIMUM C_D PULSE WIDTH

NOTE: Set-up Times and Hold Times are shown as positive values but may be specified as negative values.

4014B
8-BIT SHIFT REGISTER

DESCRIPTION – The 4014B is a fully synchronous edge-triggered 8-Bit Shift Register with eight synchronous Parallel Inputs (P_0-P_7), a synchronous Serial Data Input (D_S), a synchronous Parallel Enable Input (PE), a LOW-to-HIGH edge-triggered Clock Input (CP) and Buffered Parallel Outputs from the last three stages (Q_5-Q_7).

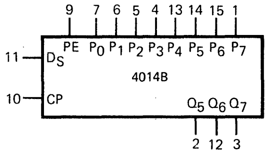
Operation is synchronous and the device is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is HIGH, data is loaded into the register from the Parallel Inputs (P_0–P_7) on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is LOW, data is shifted into the first register position from the Serial Data Input (D_S) and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

- **TYPICAL SHIFT FREQUENCY OF 14.7 MHz AT V_{DD} = 10 V**
- **PARALLEL OR SERIAL TO SERIAL DATA TRANSFER**
- **AVAILABLE OUTPUTS FROM THE LAST THREE STAGES**
- **FULLY SYNCHRONOUS**

PIN NAMES

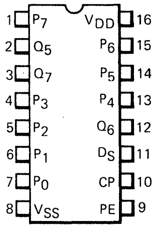
PE	Parallel Enable Input
P_0–P_7	Parallel Data Inputs
D_S	Serial Data Input
CP	Clock Input (L→H Edge-Triggered)
Q_5, Q_6, Q_7	Buffered Parallel Outputs from the Last Three Stages

LOGIC SYMBOL



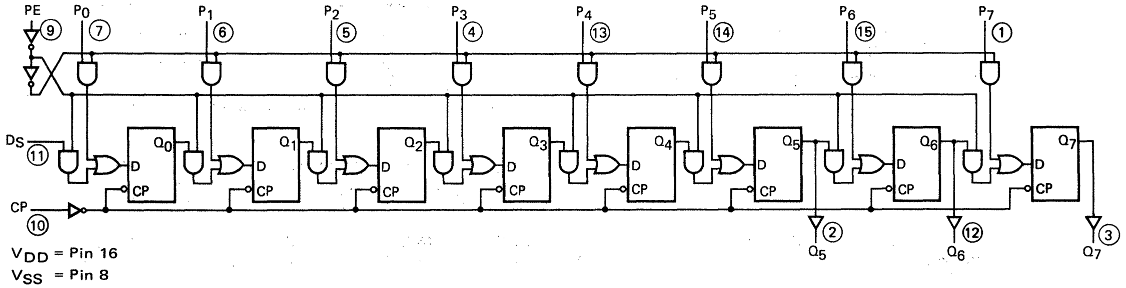
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

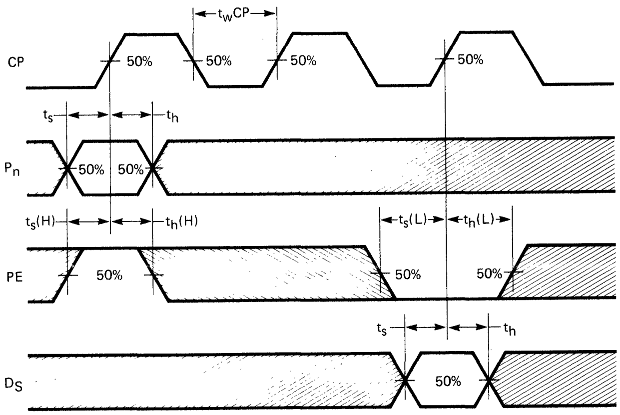
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to any Q		129	275		57	120		41	96	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			165	350		68	120		47	96	ns	
t_{TLH}	Output Transition Time		70	135		37	75		21	45	ns	
t_{THL}			77	135		34	75		21	45	ns	
t_wCP	CP Minimum Pulse Width	200	93		100	33		80	22		ns	
t_s	Set-Up Time PE to CP	300	118		80	44		64	29		ns	
t_h	Hold Time PE to CP	25	15		5	3		4	2		ns	
t_s	Set-Up Time D_S to CP	200	80		50	28		40	17		ns	
t_h	Hold Time D_S to CP	10	5		0	-1		0	-1		ns	
t_s	Set-Up Time P_n to CP	250	108		100	37		80	23		ns	
t_h	Hold Time P_n to CP	20	10		5	3		4	2		ns	
f_{MAX}	Max. Input Clock Frequency (Note 3)	2	5.8		5	14.7		6	17		MHz	

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

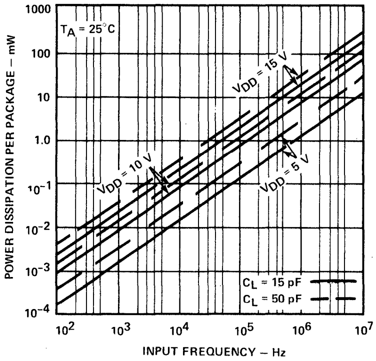
SWITCHING WAVEFORMS



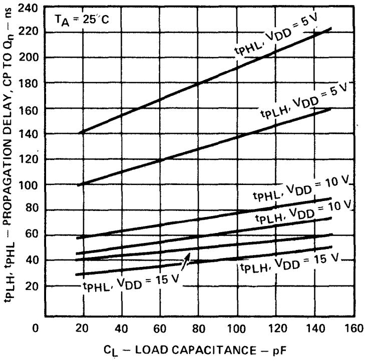
MINIMUM CLOCK PULSE WIDTH
AND SET-UP AND HOLD TIMES, PE TO CP, D_S TO CP, AND P_n TO CP

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

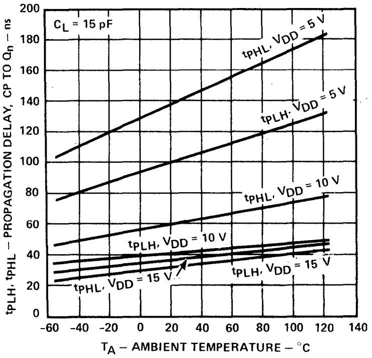
TYPICAL ELECTRICAL CHARACTERISTICS



POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY CP TO Q_n VERSUS LOAD CAPACITANCE



PROPAGATION DELAY, CP TO Q_n VERSUS TEMPERATURE

4015B

DUAL 4-BIT STATIC SHIFT REGISTER

DESCRIPTION – The 4015B is a Dual Edge-Triggered 4-Bit Static Shift Register (Serial-to-Parallel Converter). Each Shift Register has a Serial Data Input (D), a Clock Input (CP), four fully buffered parallel Outputs (Q_0–Q_3) and an overriding asynchronous Master Reset Input (MR).

Information present on the serial Data Input (D) is shifted into the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

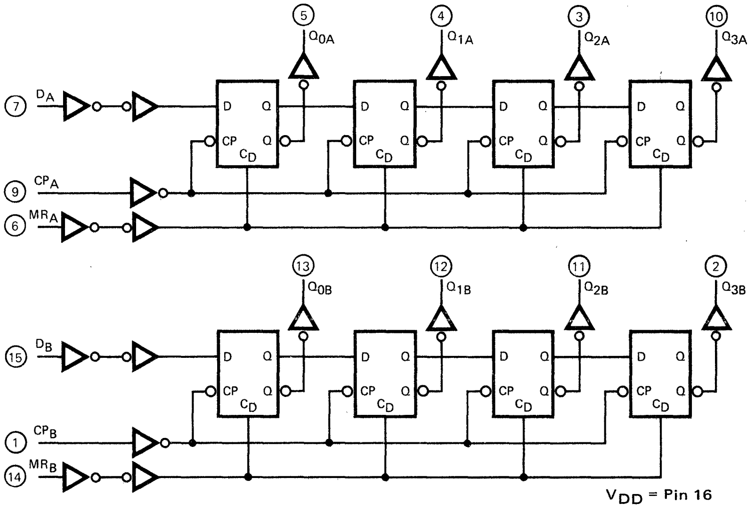
A HIGH on the Master Reset Input (MR) clears the register and forces the Outputs (Q_0 - Q_3) LOW, independent of the Clock and Data Inputs (CP and D).

- **TYPICAL SHIFT FREQUENCY OF 14 MHz AT V_{DD} = 10 V**
- **ASYNCHRONOUS MASTER RESET**
- **SERIAL-TO-PARALLEL DATA TRANSFER**
- **FULLY BUFFERED OUTPUTS FROM EACH STAGE**

PIN NAMES

D_A, D_B	Serial Data Input
MR_A, MR_B	Master Reset Input (Active HIGH)
CP_A, CP_B	Clock Input (L→H Edge-Triggered)
Q_{0A}, Q_{1A}, Q_{2A}, Q_{3A}	Parallel Outputs
Q_{0B}, Q_{1B}, Q_{2B}, Q_{3B}	Parallel Outputs

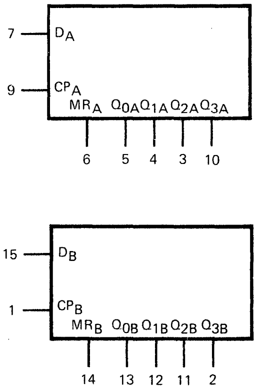
LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
O = Pin Number

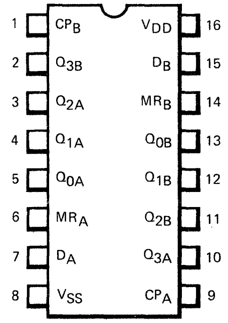
LOGIC SYMBOL

4015B



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

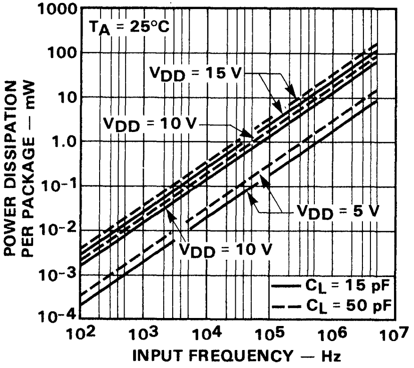
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q		165	300		85	150		50	120	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			165	300		85	150		50	120	ns	
t_{PHL}	Propagation Delay, MR to Q		180	325		90	160		60	128	ns	
t_{TLH}	Output Transition Time		85	150		45	85		30	50	ns	
t_{THL}			85	150		45	85		30	50	ns	
t_s	Set-Up Time, D to CP	150	70		50	30		40	25		ns	
t_h	Hold Time, D to CP	0	-5		0	-20		0	-10		ns	
t_wCP(L)	Minimum Clock Pulse Width	120	60		70	35		56	25		ns	
t_wMR(H)	Minimum MR Pulse Width	75	40		45	25		36	20		ns	
t_{rec}	MR Recovery Time	300	160		120	60		96	45		ns	
f_{MAX}	Maximum CP Frequency (Note 3)	4	8		7	14		8	16		MHz	

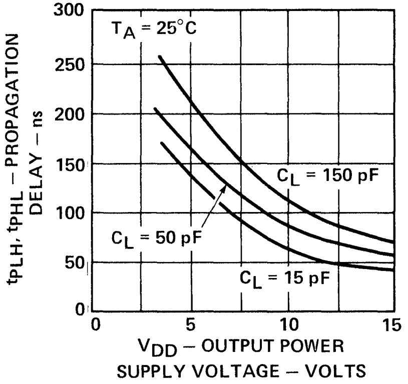
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

TYPICAL ELECTRICAL CHARACTERISTICS

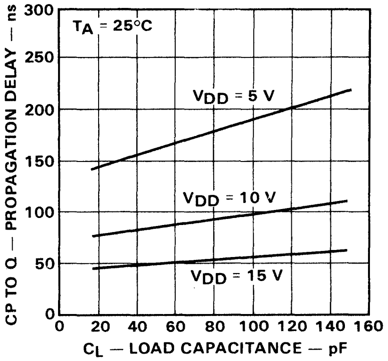
POWER DISSIPATION VERSUS FREQUENCY



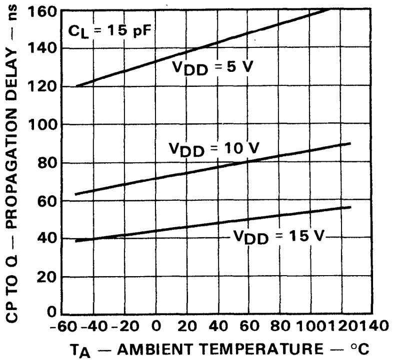
PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



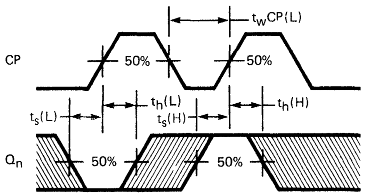
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



PROPAGATION DELAY VERSUS TEMPERATURE



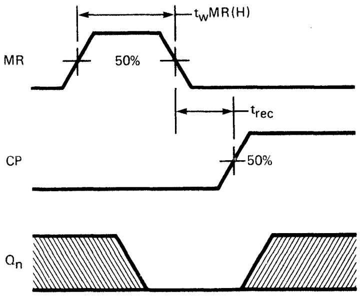
SWITCHING WAVEFORMS



SET-UP TIMES, HOLD TIMES AND MINIMUM CLOCK PULSE WIDTH

NOTE:

t_s and t_h are shown as positive values but may be specified as negative values.



RECOVERY TIME FOR MR AND MINIMUM MR PULSE WIDTH

4016B

QUAD BILATERAL SWITCHES

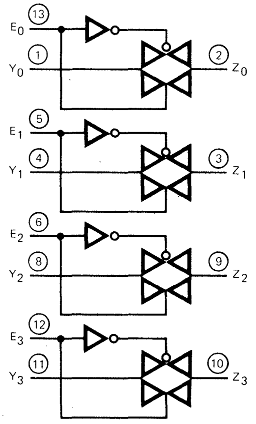
DESCRIPTION — The 4016B has four independent bilateral analog switches (transmission gates). Each switch has two Input/Output Terminals (Y_n, Z_n) and an active HIGH Enable Input (E_n). A HIGH on the Enable Input establishes a low impedance bidirectional path between Y_n and Z_n (ON condition). A LOW on the Enable Input disables the switch and establishes a high impedance between Y_n and Z_n (OFF condition).

- **DIGITAL OR ANALOG SIGNAL SWITCHING**
- **INDIVIDUAL ENABLE INPUTS (ACTIVE HIGH)**

PIN NAMES

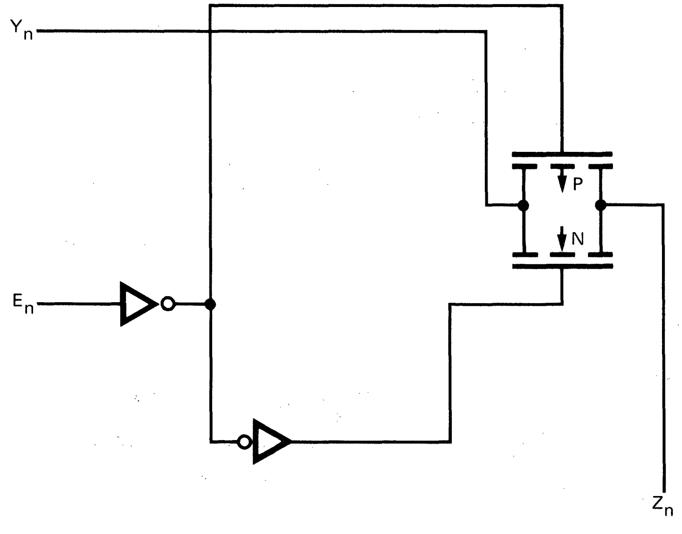
E_0 - E_3	Enable Inputs
Y_0 - Y_3	Input/Output Terminals
Z_0 - Z_3	Input/Output Terminals

LOGIC SYMBOL

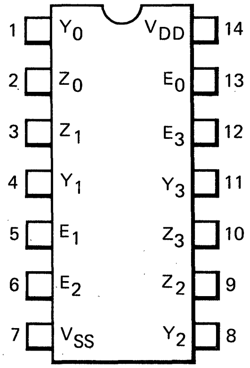


V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Numbers

LOGIC DIAGRAM (1/4 of a 4016B)



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS	
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V						
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
R_{ON}	ON Resistance	XC						610 660 840			370 400 520	Ω	MIN 25°C MAX	$V_{is} = V_{DD}$ or V_{SS}	R_L = 10 kΩ to $V_{DD}/2$ $E_n = V_{DD}$
								1900 2000 2380			790 850 1080	Ω	MIN 25°C MAX	$V_{is} = V_{DD}/2$ ±0.25 V	
		XM						600 660 960			360 400 600	Ω	MIN 25°C MAX	$V_{is} = V_{DD}$ or V_{SS}	R_L = 10 kΩ to $V_{DD}/2$ $E_n = V_{DD}$
								1870 2000 2600			775 850 1230	Ω	MIN 25°C MAX	$V_{is} = V_{DD}/2$ ± 0.25 V	
ΔR_{ON}	Δ ON Resistance Between Any Two Switches						15			10		Ω	25°C	$V_{is} = V_{DD}$ or V_{SS}, $E_n = V_{DD}$ R_L = 10 kΩ to $V_{DD}/2$	
I_Z	OFF State Leakage Current, Any Y to Z	XC										μA	MIN, 25 C MAX	$V_{is} = V_{DD}$ or V_{SS}, $E_n = V_{SS}$ $V_{os} = V_{SS}$ or V_{DD}	
		XM											MIN, 25°C MAX		
I_{DD}	Quiescent Power Supply Current	XC			1 7.5			2 15			4 30	μA	MIN, 25°C MAX	All inputs at V_{DD} or V_{SS}	
		XM			0.25 7.5			0.5 15			1 30	μA	MIN, 25°C MAX		

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25°C$ (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		17	35		14	28		13	27	ns	$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ≤ 20 ns $E_n = V_{DD}$ $V_{is} = V_{DD}$ (square wave)
t_{PHL}			15	31		10	20		4	9		
t_{PZL}	Output Enable Time		42	84		20	40		14	28	ns	$C_L = 50$ pF, $R_L = 1$ kΩ to V_{SS} or V_{DD} $E_n = V_{DD}$ (square wave) Input Transition Times ≤ 20 ns $V_{is} = V_{DD}$ or V_{SS}
t_{PZH}			45	90		22	44		18	35		
t_{PLZ}	Output Disable Time		80	160		78	157		76	155	ns	
t_{PHZ}			74	150		70	140		62	125		
	Distortion, Sine Wave Response					0.4					%	$R_L = 10$ kΩ Input Frequency = 1 kHz $E_n = V_{DD}$ $V_{is} = V_{DD}/2$ (sine wave) p-p
	Crosstalk Between Any Two Switches					0.9					MHz	$R_L = 1$ kΩ $E_A = V_{DD}$, $E_B = V_{SS}$ $V_{is} = V_{DD}/2$ (sine wave) p-p 20 Log_{10} $[V_{os}(B)/V_{is}(A)] = -50$ dB
	Crosstalk, Enable Input to Output					50					mV	Input Transition Times ≤ 20 ns $R_{L(OUT)} = 1$ kΩ $R_{L(IN)} = 50$ Ω $E_n = V_{DD}$ (square wave)
	OFF State Feedthrough					1.25					MHz	$R_L = 1$ kΩ, $E_n = V_{SS}$ $V_{is} = V_{DD}/2$ (sine wave) p-p $20 \text{ Log}_{10} (V_{os}/V_{is}) = -50$ dB
	ON State Frequency Response					40					MHz	$R_L = 1$ kΩ $V_{is} = V_{DD}/2$ (sine wave) p-p $E_n = V_{DD}$, 20 Log_{10} $(V_{os}/V_{os} @ 1 \text{ kHz}) = -3$ dB
f_{MAX}	Enable Input Frequency (Note 4)					10					MHz	$C_L = 50$ pF, $R_L = 1$ kΩ Input Transition Times ≤ 20 ns $E_n = V_{DD}$ (square wave) $V_{os} = V_{os}/2$ at DC $V_{is} = V_{DD}$
C_{is}	Input Switch Capacitance					4					pF	$V_{DD} = 10$ V $E_n = V_{SS}$ V_{is} = Open 100 kHz or 1 MHz Bridge
C_{os}	Output Switch Capacitance					4					pF	
C_{ios}	Feedthrough Switch Capacitance					0.2					pF	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11 the voltage drop across the bidirectional switch must not exceed 0.5 V at $T_A \leq 25°C$, or 0.3 V at $T_A > 25°C$. No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.

4017B

5-STAGE JOHNSON COUNTER

DESCRIPTION – The 4017B is a 5-Stage Johnson Decade Counter with ten glitch free decoded active HIGH Outputs (O_0–O_9), an active LOW Output from the most significant flip-flop ($\overline{Q_{5-9}}$), active HIGH and active LOW Clock Inputs (CP_0, $\overline{CP_1}$) and an overriding asynchronous Master Reset Input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while $\overline{CP_1}$ is LOW or a HIGH-to-LOW transition at $\overline{CP_1}$ while CP_0 is HIGH (see Functional Truth Table). When cascading 4017B counters, the $\overline{Q_{5-9}}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next 4017B.

A HIGH on the Master Reset Input (MR) resets the counter to zero ($O_0 = \overline{Q_{5-9}}$ = HIGH, O_1–O_9 = LOW) independent of the Clock Inputs (CP_0, $\overline{CP_1}$).

- **TYPICAL COUNT FREQUENCY OF 13.8 MHz AT V_{DD} = 10 V**
- **ACTIVE HIGH DECODED OUTPUTS**
- **TRIGGERS ON EITHER A HIGH-TO-LOW OR LOW-TO-HIGH TRANSITION**
- **CASCADABLE**

PIN NAMES

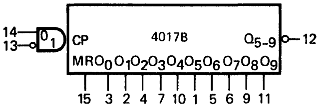
CP_0	Clock Input (L→H Triggered)
$\overline{CP_1}$	Clock Input (H→L Triggered)
MR	Master Reset Input
O_0–O_9	Decoded Outputs
$\overline{Q_{5-9}}$	Carry Output (Active LOW)

FUNCTIONAL TRUTH TABLE

MR	CP_0	$\overline{CP_1}$	OPERATION
H	X	X	$O_0 = \overline{Q_{5-9}}$ = H; O_1 - O_9 = L
L	H	H → L	Counter Advances
L	L → H	L	Counter Advances
L	L	X	No Change
L	X	H	No Change
L	H	L → H	No Change
L	H → L	L	No Change

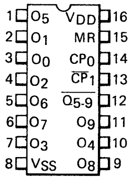
H = HIGH Level
L = LOW Level
L→H = LOW-to-HIGH Transition
H→L = HIGH-to-LOW Transition
X = Don't Care

LOGIC SYMBOL



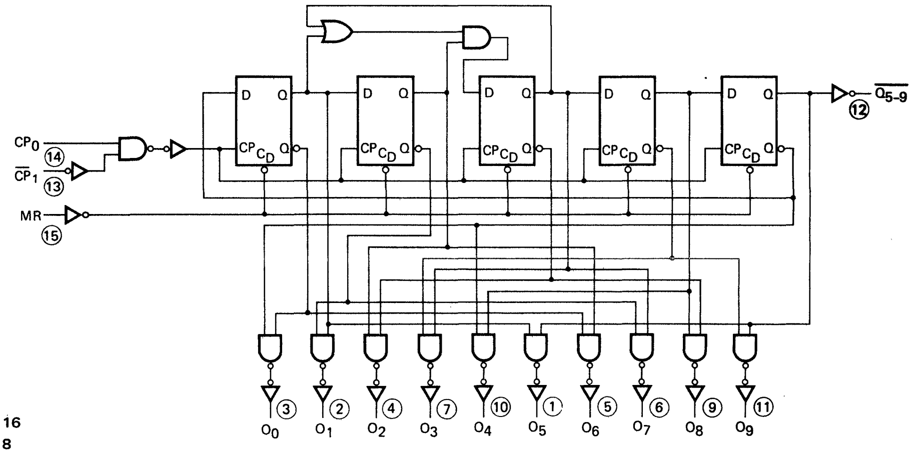
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

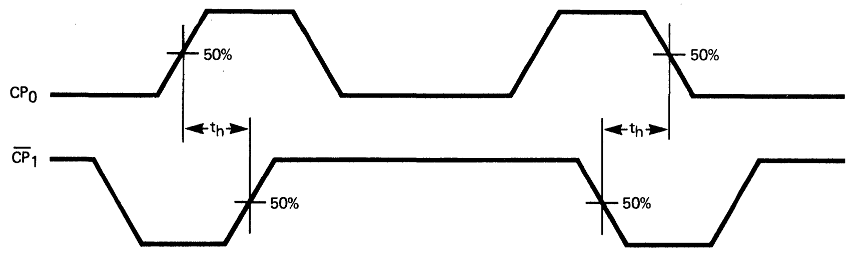
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP}_1$ to O_n		278	700		114	285		82	228	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			226	550		94	240		67	192	ns	
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP}_1$ to $\overline{O}_{5\text{-}9}$		205	525		87	225		63	180	ns	
t_{PHL}			261	650		105	250		73	200	ns	
t_{PHL}	Propagation Delay, MR to O_n		170	430		80	175		52	140	ns	
t_{PLH}	Propagation Delay, MR to $\overline{O}_{5\text{-}9}$		125	300		65	130		40	104	ns	
t_{TLH}	Output Transition Time		59	135		31	70		23	45	ns	
t_{THL}			63	135		26	70		19	45	ns	
t_wCP	Min. CP_0 or $\overline{CP}_1$ Pulse Width	200	85		70	37		56	28		ns	
t_wMR	Minimum MR Pulse Width	130	52		55	22		44	18		ns	
t_{rec}	MR Recovery Time	50	16		25	6		20	3		ns	
t_h	Hold Time, CP_0 to $\overline{CP}_1$	200	90		90	39		72	26		ns	
t_h	Hold Time, $\overline{CP}_1$ to CP_0	200	89		90	39		72	22		ns	
f_{MAX}	Input Count Frequency (Note 3)	2.5	5.8		7	13.8		8	16		MHz	

NOTES:

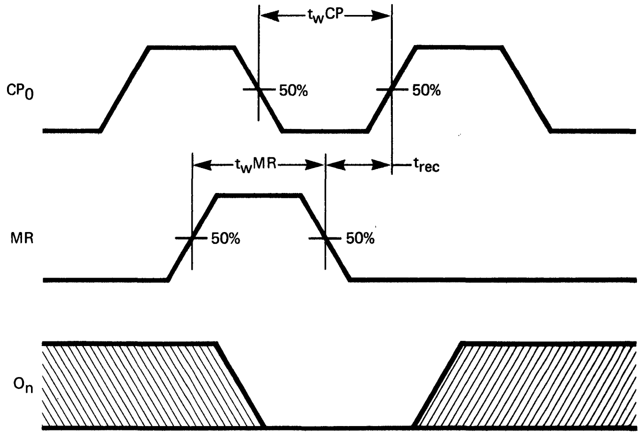
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to either Clock Input (CP_0 or $\overline{CP}_1$) be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



HOLD TIMES, CP_0 TO $\overline{CP_1}$ AND $\overline{CP_1}$ TO CP_0

Hold Times are shown as positive values, but may be specified as negative values.



MINIMUM PULSE WIDTHS FOR CP AND MR AND RECOVERY TIME FOR MR

CONDITIONS: $\overline{CP_1}$ = LOW while CP_0 is triggered on a LOW-to-HIGH transition. t_wCP and t_{rec} also apply when CP_0 = HIGH and $\overline{CP_1}$ is triggered on a HIGH-to-LOW transition.

4018B

PRESETTABLE DIVIDE-BY-N COUNTER

DESCRIPTION — The 4018B is a 5-Stage Johnson Counter with a Clock Input (CP), a Data Input (D), an asynchronous Parallel Load Input (PL), five Parallel Inputs (P_0—P_4), five active LOW buffered Outputs ($\overline{Q}_0$—$\overline{Q}_4$) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0—P_4) is asynchronously loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of the Clock (CP) and Data (D) Inputs. Data present in the counter is stored on the HIGH-to-LOW transition of the Parallel Load Input (PL). When the Parallel Load Input is LOW, the counter advances on the LOW-to-HIGH transition of the Clock Input (CP). By connecting the Outputs ($\overline{Q}_0$—$\overline{Q}_4$) to the Data Input (D), the counter operates as a divide-by-n counter ($2 \leq n \leq 10$); see below.

A HIGH on the Master Reset Input (MR) resets the counter ($\overline{Q}_0$—$\overline{Q}_4$ = HIGH) independent of all other inputs.

- **ASYNCHRONOUS MASTER RESET INPUT (ACTIVE HIGH)**
- **ACTIVE LOW FULLY BUFFERED DECODED OUTPUTS**
- **DIVIDE-BY-N WITH $2 \leq N \leq 10$**
- **CLOCK INPUT L→H EDGE-TRIGGERED**
- **ASYNCHRONOUS PARALLEL LOAD INPUT (ACTIVE HIGH)**

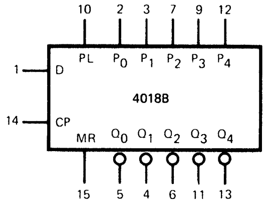
PIN NAMES

PL	Parallel Load Input
P_0—P_4	Parallel Inputs
D	Data Input
CP	Clock Input (L→H Edge-Triggered)
MR	Master Reset Input
$\overline{Q}_0$—$\overline{Q}_4$	Buffered Outputs (Active LOW)

DIVIDE-BY-N MODE SELECTION

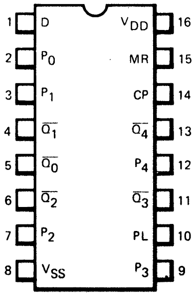
DIVIDE BY	D INPUT
2	$\overline{Q}_0$
3	$\overline{Q}_0 \cdot \overline{Q}_1$
4	$\overline{Q}_1$
5	$\overline{Q}_1 \cdot \overline{Q}_2$
6	$\overline{Q}_2$
7	$\overline{Q}_2 \cdot \overline{Q}_3$
8	$\overline{Q}_3$
9	$\overline{Q}_3 \cdot \overline{Q}_4$
10	$\overline{Q}_4$

LOGIC SYMBOL



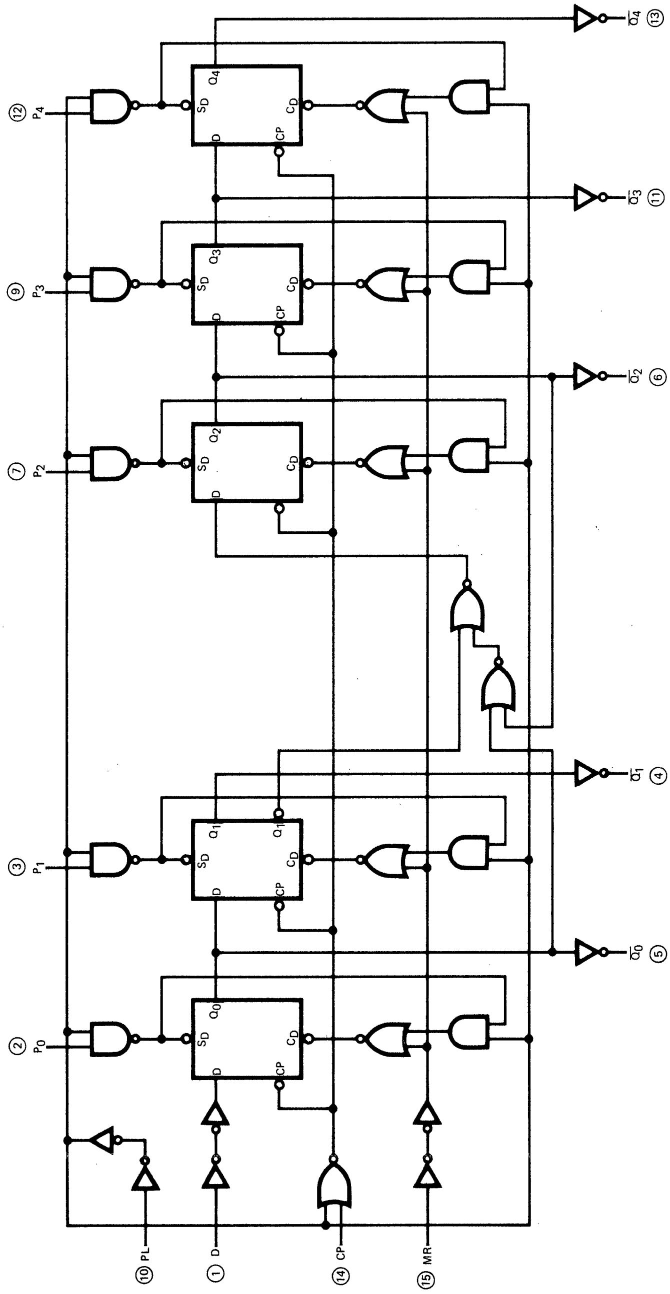
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8
○ = PIN NUMBER

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN. 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN. 25°C	
					150			300			600		MAX	

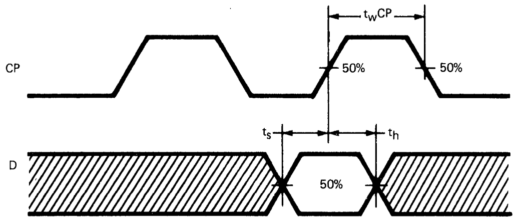
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{Qn}$		280 280	500 600		115 115	200 240		80 80	160 170	ns ns	C_L = 50 pF, R_L = 200 kΩ, Input Transition Times ≤ 20 ns
t_{PLH}	Propagation Delay, MR to $\overline{Qn}$		280	600		115	240		80	170	ns	
t_{PLH} t_{PHL}	Propagation Delay, PL to $\overline{Qn}$		280 280	600 740		115 115	240 300		80 80	170 200	ns ns	
t_{TLH} t_{THL}	Output Transition Time		59 63	135 135		31 26	75 75		23 19	45 45	ns ns	
t_{rec}	MR Recovery Time	250	150		110	50		90	40		ns	
$t_W MR$	MR Minimum Pulse Width	130	65		60	30		48	22		ns	
$t_W CP$	CP Minimum Pulse Width	260	100		130	50		100	40		ns	
t_s t_h	Set-Up Time, D to CP Hold Time, D to CP	175	85 0		75	25 0		60	35 0		ns ns	
t_s t_h	Set-Up Time, Pn to PL Hold Time, Pn to PL	175	85 0		75	25 0		60	35 0		ns ns	
f_{MAX}	Input Count Frequency (Note 3)	1.5	3		3.5	8		4.5	10		MHz	

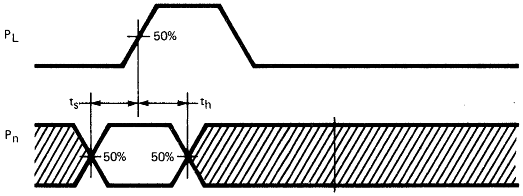
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

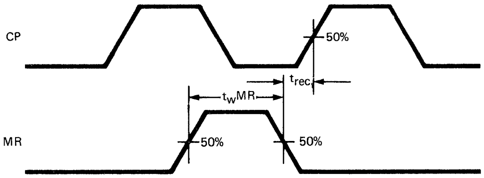
SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, D TO CP



SET-UP AND HOLD TIMES, P_n to PL



MR RECOVERY TIME AND MINIMUM MR PULSE WIDTH

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

4019B

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION – The 4019B provides four multiplexing circuits with common selection inputs; each circuit contains two inputs and one output. It may be used to select four bits of information from one of two sources. The A inputs are selected when S_A is HIGH, the B inputs when S_B is HIGH. When S_A and S_B are HIGH, output (Z_n) is the logical OR of the A_n and B_n inputs ($Z_n = A_n + B_n$). When S_A and S_B are LOW, output (Z_n) is LOW independent of the multiplexer inputs (A_n and B_n). The 4019B cannot be used to multiplex analog signals. The outputs utilize standard buffers for best performance.

PIN NAMES

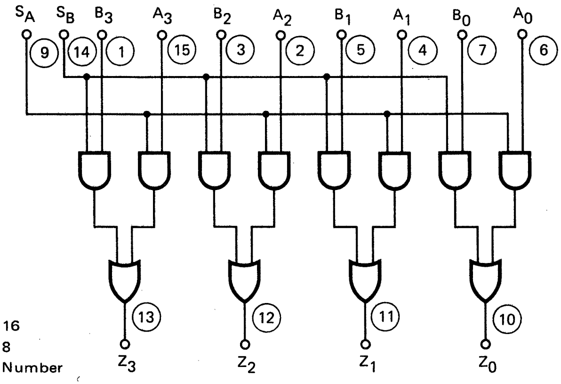
S_A, S_B	Select Inputs (Active HIGH)
$A_0 - A_3$, $B_0 - B_3$	Multiplexer Inputs
$Z_0 - Z_3$	Multiplexer Outputs

TRUTH TABLE

SELECT		INPUTS		OUTPUT
S_A	S_B	A_n	B_n	Z_n
L	L	X	X	L
H	L	L	X	L
H	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	H	H	X	H
H	H	X	H	H
H	H	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

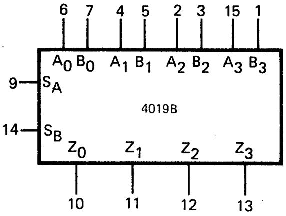
LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

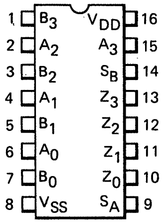
$Z_n = S_A A_n + S_B B_n$

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20 150			40 300			80 600	µA	MIN, 25°C MAX	All inputs at 0 V or V_{DD}
		XM			5 150			10 300			20 600	µA	MIN, 25°C MAX	

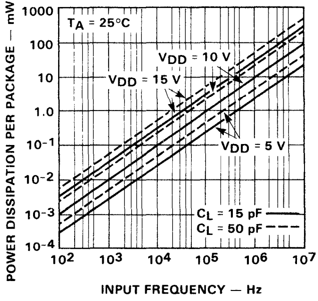
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		75	150		35	70		24	56	ns	C_L = 50 pF,
t_{PHL}	S_A, S_B, A_n or B_n to Z_n		85	160		37	75		29	60	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		80	135		42	70		32	45	ns	Input Transition
t_{THL}			90	135		40	70		30	45	ns	Times ≤ 20 ns

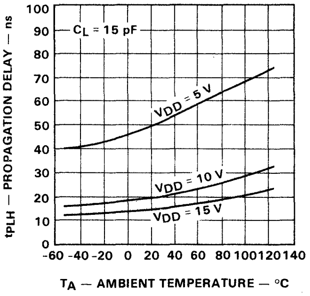
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

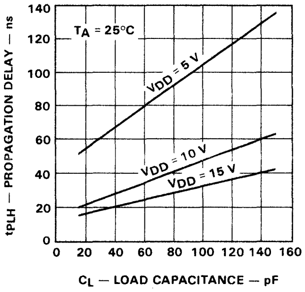
TYPICAL ELECTRICAL CHARACTERISTICS



POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

4020B
14-STAGE BINARY COUNTER

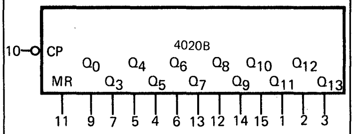
DESCRIPTION – The 4020B is a 14-Stage Binary Ripple Counter with a Clock Input ($\overline{CP}$), an overriding asynchronous Master Reset Input (MR) and twelve fully buffered Outputs (Q_0, Q_3–Q_{13}). The counter advances on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$). A HIGH on the Master Reset Input (MR) clears all counter stages and forces all Outputs (Q_0, Q_3–Q_{13}) LOW, independent of the Clock Input ($\overline{CP}$).

- **25 MHz TYPICAL COUNT FREQUENCY AT V_{DD} = 10 V**
- **COMMON ASYNCHRONOUS MASTER RESET**
- **FULLY BUFFERED OUTPUTS FROM THE FIRST STAGE AND THE LAST ELEVEN STAGES**

PIN NAMES

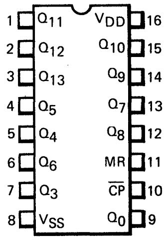
$\overline{CP}$	Clock Input (H→L Triggered)
MR	Master Reset Input (Active HIGH)
Q_0, Q_3–Q_{13}	Parallel Outputs

LOGIC SYMBOL



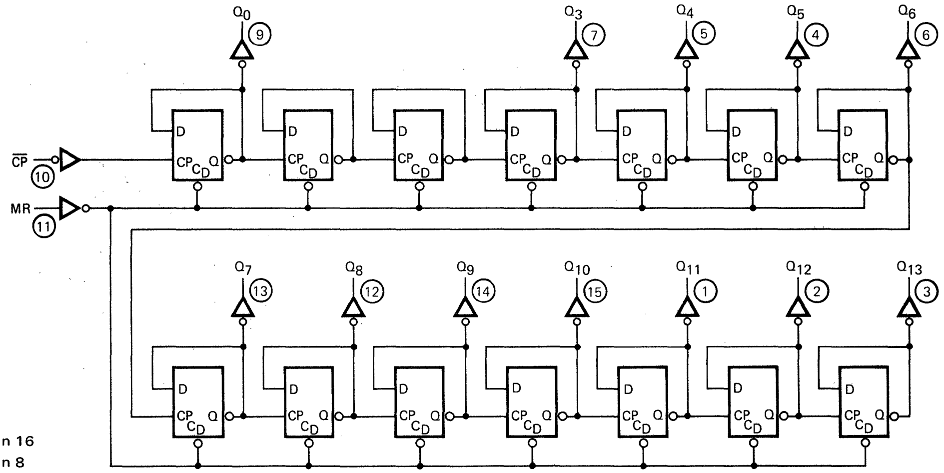
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

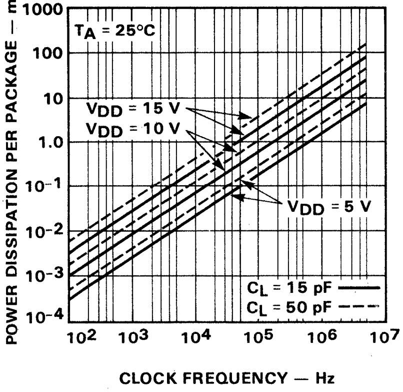
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		130	260		55	110		37	88	ns	
t_{PHL}			110	220		45	90		33	72	ns	
t_{PHL}	Propagation Delay, MR to Q_n		180	360		75	150		50	120	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{TLH}	Output Transition Time		65	135		35	70		25	45	ns	
t_{THL}			65	135		35	70		25	45	ns	
$t_W\overline{CP}(H)$	Minimum Clock Pulse Width	100	50		40	20		32	16		ns	
$t_WMR(H)$	Minimum MR Pulse Width	140	70		55	27		44	20		ns	
t_{rec}	Recovery Time for MR	85	43		35	17		28	12		ns	
f_{MAX}	Input Clock Frequency (Note 2)	5	10		12	25		14	30		MHz	

NOTES:

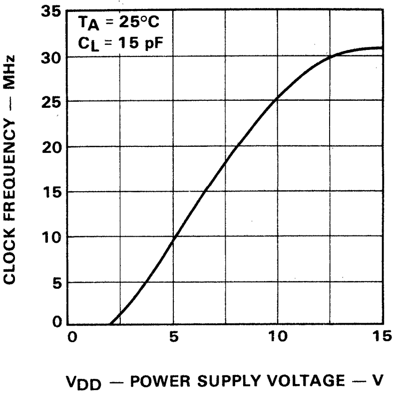
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

TYPICAL ELECTRICAL CHARACTERISTICS

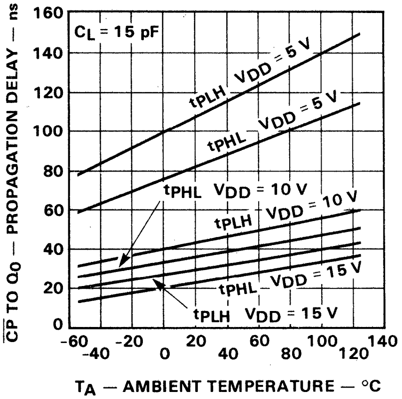
POWER DISSIPATION VERSUS CLOCK FREQUENCY



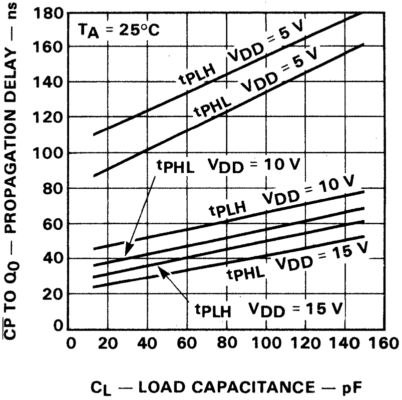
CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE



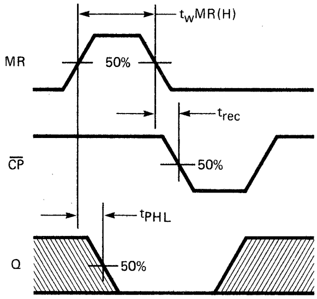
PROPAGATION DELAY VERSUS TEMPERATURE



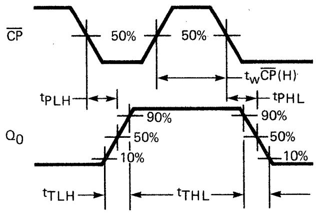
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORMS



PROPAGATION DELAY MASTER RESET TO OUTPUT, MINIMUM MASTER RESET PULSE WIDTH AND RECOVERY TIME FOR MASTER RESET



PROPAGATION DELAY CLOCK TO OUTPUT Q_0, OUTPUT TRANSITION TIMES AND MINIMUM CLOCK PULSE WIDTH

4021B

8-BIT SHIFT REGISTER

DESCRIPTION — The 4021B is an Edge-Triggered 8-Bit Shift Register (Parallel-to-Serial Converter) with a synchronous Serial Data Input (D_S), a Clock Input (CP), an asynchronous active HIGH Parallel Load Input (PL), eight asynchronous Parallel Data Inputs (P_0–P_7) and Buffered Parallel Outputs from the last three stages (Q_5–Q_7).

Information on the Parallel Data Inputs (P_0–P_7) is asynchronously loaded into the register while the Parallel Load Input (PL) is HIGH, independent of the Clock (CP) and Serial Data (D_S) inputs. Data present in the register is stored on the HIGH-to-LOW transition of the Parallel Load Input (PL).

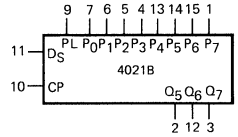
When the Parallel Load Input is LOW, data on the Serial Data Input (D_S) is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

- **TYPICAL SHIFT FREQUENCY OF 18.1 MHz AT V_{DD} = 10 V**
- **PARALLEL-TO-SERIAL DATA TRANSFER**
- **BUFFERED OUTPUTS AVAILABLE LAST THREE STAGES**
- **CLOCK INPUT IS L → H EDGE-TRIGGERED**

PIN NAMES

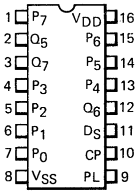
PL	Parallel Load Input
P_0-P_7	Parallel Data Inputs
D_S	Serial Data Input
CP	Clock Input (L→H Edge-Triggered)
Q_5-Q_7	Buffered Parallel Outputs from the Last Three Stages

LOGIC SYMBOL



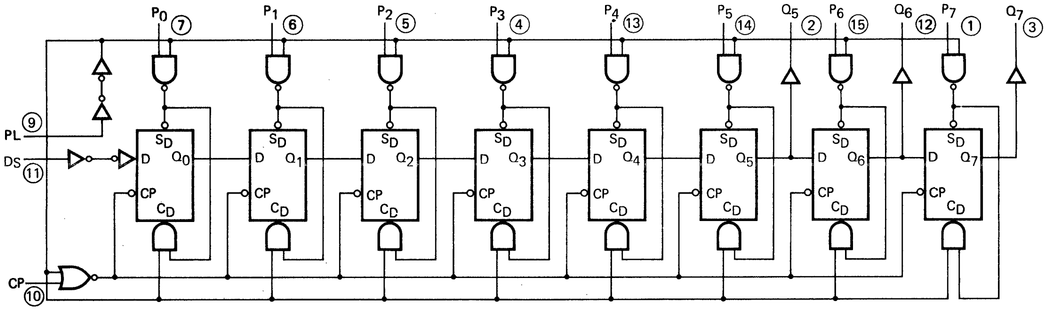
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

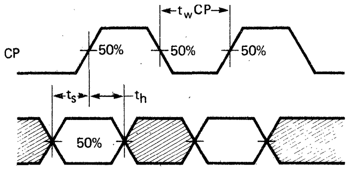
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

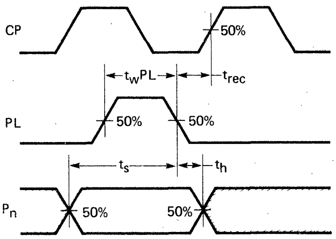
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		134			59			40		ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			184			74			49		ns	
t_{PLH}	Propagation Delay, PL to Q_n		188			78			54		ns	
t_{PHL}			274			105			72		ns	
t_{TLH}	Output Transition Time		58			31			22		ns	
t_{THL}			69			27			22		ns	
t_wCP	CP Minimum Pulse Width		61			21			14		ns	
t_wPL	PL Minumum Pulse Width		67			24			16		ns	
t_{rec}	PL Recovery Time		71			28			21		ns	
t_s	Set-Up Time D_S to CP		51			16			12		ns	
t_h	Hold Time D_S to CP		49			15			11		ns	
t_s	Set-Up Time P_n to PL		78			28			18		ns	
t_h	Hold Time, P_n to PL		72			26			16		ns	
f_{MAX}	Shift Frequency (Note 3)		7.8			18.1			21		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, D_S TO CP



MINIMUM PL PULSE WIDTH, RECOVERY TIME FOR PL, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

4022B

4-STAGE DIVIDE-BY-8 JOHNSON COUNTER

DESCRIPTION – The 4022B is a 4-Stage Divide-by-8 Johnson Counter with eight glitch free active HIGH Decoded Outputs (O_0–O_7), an active LOW Output from the most significant flip-flop ($\overline{Q_{4-7}}$), an active HIGH and an active LOW Clock Input (CP_0, $\overline{CP_1}$) and an overriding asynchronous Master Reset Input (MR).

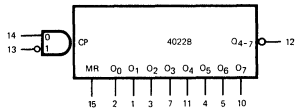
The counter is advanced by either a LOW-to-HIGH transition at CP_0 while $\overline{CP_1}$ is LOW or a HIGH-to-LOW transition at $\overline{CP_1}$ while CP_0 is HIGH (see Functional Truth Table). When cascading the counters, the $\overline{Q_{4-7}}$ Output (which is LOW while the counter is in states 4, 5, 6 and 7) can be used to drive the CP_0 Input of the next 4022B. A HIGH on the Master Reset Input (MR) resets the counter to Zero ($O_0 = \overline{Q_{4-7}}$ = HIGH, O_1 – O_7 = LOW) independent of the Clock Inputs (CP_0, $\overline{CP_1}$).

- **CLOCK EDGE-TRIGGERED ON EITHER A LOW-TO-HIGH TRANSITION OR A HIGH-TO-LOW TRANSITION**
- **BUFFERED CARRY OUTPUT ($\overline{Q_{4-7}}$) AVAILABLE FOR CASCADING**
- **BUFFERED FULLY DECODED OUTPUTS**

PIN NAMES

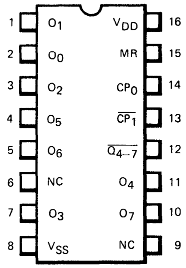
CP_0	Clock Input (L→H Edge-Triggered)
$\overline{CP_1}$	Clock Input (H→L Edge-Triggered)
MR	Master Reset Input
O_0–O_7	Decoded Outputs
$\overline{Q_{4-7}}$	Carry (Active LOW) Output

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 6, 9

CONNECTION DIAGRAM
DIP (TOP VIEW)



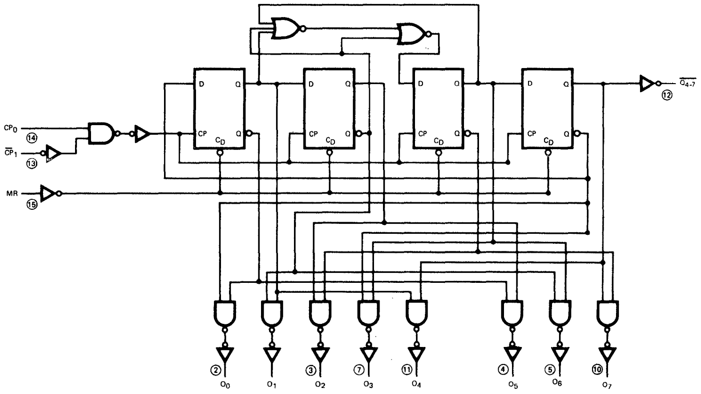
NOTE:
The Flatpak version has the same pinouts (connection Diagram) as the Dual In-line package

FUNCTIONAL TRUTH TABLE

MR	CP_0	$\overline{CP_1}$	OPERATION
H	X	X	$O_0 = \overline{Q_{4-7}}$ = H; O_1–O_7 = L
L	H	H→L	Counter Advances
L	L→H	L	Counter Advances
L	L	X	No Change
L	X	H	No Change
L	H	L→H	No Change
L	L→L	L	No Change

H = HIGH Level
I = LOW Level
L→H = LOW-to-HIGH Transition
H→L = HIGH-to-LOW Transition
X = Don't Care

LOGIC DIAGRAM



NC = Pin 6, 9
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

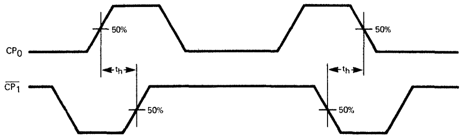
DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25°C$ (See Note 2)

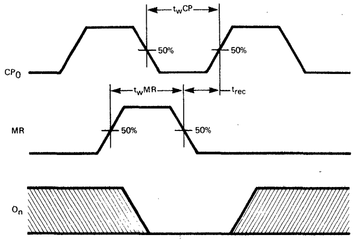
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		245	615		95	240		60	150	ns	$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ≤ 20 ns
t_{PHL}	CP_0 or $\overline{CP}_1$ to O_n		195	490		75	190		50	125		
t_{PLH}	Propagation Delay,		190	490		75	190		50	125	ns	
t_{PHL}	CP_0 or $\overline{CP}_1$ to $\overline{Q}_{4-7}$		245	615		90	240		60	150		
t_{PHL}	Propagation Delay, MR to O_n		130	325		55	135		40	100	ns	
t_{PLH}	Propagation Delay, MR to $\overline{Q}_{4-7}$		110	275		45	110		35	90	ns	
t_{TLH}	Output Transition Time		70	115		35	90		25	65	ns	
t_{THL}			70	115		35	90		25	65		
t_wCP	Min. CP_0 or $\overline{CP}_1$ Pulse Width	90	35		40	15		25	10		ns	
t_wMR	Minimum MR Pulse Width	90	35		40	15		25	10		ns	
t_{rec}	MR Recovery Time	35	10		20	5		15	5		ns	
t_h	Hold Time, CP_0 to $\overline{CP}_1$	190	70		85	25		70	15		ns	
t_h	Hold Time, $\overline{CP}_1$ to CP_0	190	85		85	30		70	20		ns	
f_{MAX}	Input Count Frequency (Note 3)	2.5	6		7	16		8	24		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at $V_{DD} = 5$ V, 4 µs at $V_{DD} = 10$ V, and 3 µs at $V_{DD} = 15$ V.



HOLD TIMES, CP_0 TO $\overline{CP}_1$ AND $\overline{CP}_1$ TO CP_0

NOTE: Note: Hold Times are shown as positive values, but may be specified as negative values.



MINIMUM PULSE WIDTHS FOR CP AND MR AND RECOVERY TIME FOR MR

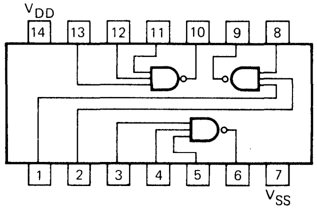
CONDITIONS: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW-to-HIGH transition. t_wCP and t_{rec} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH-to-LOW transition.

4023B

TRIPLE 3-INPUT NAND GATE

DESCRIPTION — This CMOS logic element provides a 3-input positive NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

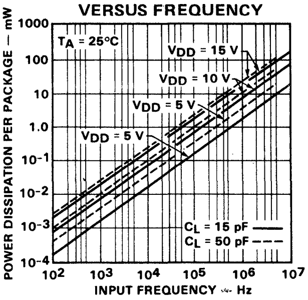
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		45	110		25	60		19	48	ns	C_L = 50 pF,
t_{PHL}			51	110		25	60		12	48	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		45	135		18	70		17	45	ns	Input Transition
t_{THL}			45	135		18	70		12	45	ns	Times ⩽ 20 ns

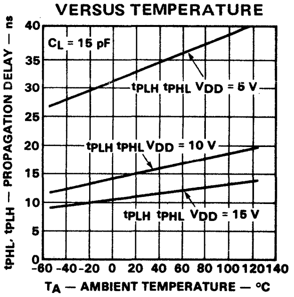
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

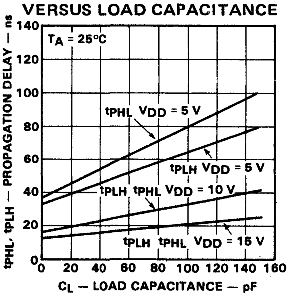
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



4024B

7-STAGE BINARY COUNTER

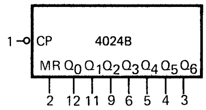
DESCRIPTION — The 4024B is a 7-Stage Binary Ripple Counter with a Clock Input ($\overline{CP}$), an overriding asynchronous Master Reset Input (MR) and seven fully Buffered Parallel Outputs (Q_0-Q_6). The counter advances on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$). A HIGH on the Master Reset Input (MR) clears all counter stages and forces all Outputs (Q_0-Q_6) LOW, independent of the Clock Input ($\overline{CP}$).

- **TYPICAL COUNT FREQUENCY OF 30 MHz AT V_{DD} = 10 V**
- **CLOCK TRIGGERED ON THE HIGH-TO-LOW TRANSITION**
- **ASYNCHRONOUS ACTIVE HIGH MASTER RESET**
- **OUTPUTS AVAILABLE FROM ALL SEVEN STAGES**

PIN NAMES

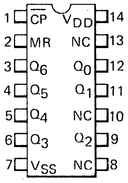
$\overline{CP}$	Clock Input (H→L Triggered)
MR	Master Reset Input
Q_0-Q_6	Buffered Parallel Outputs

LOGIC SYMBOL



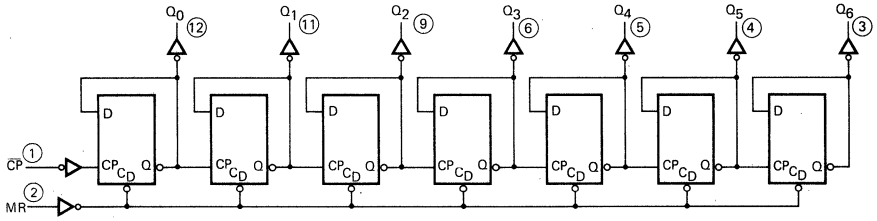
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 8, 10 and 13

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 8, 10 and 13
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

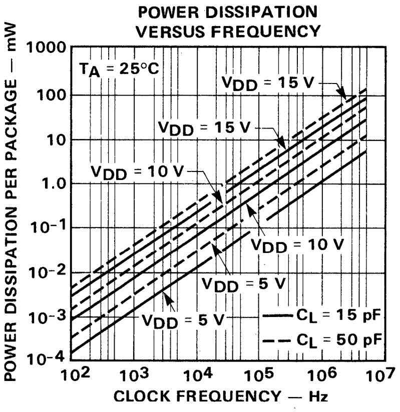
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

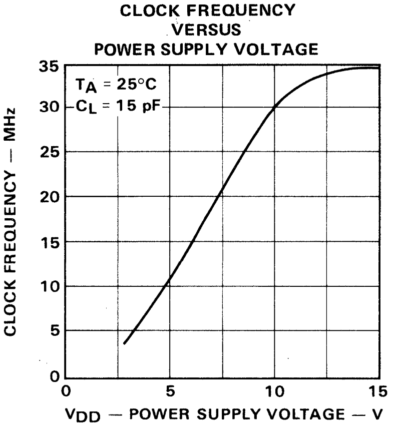
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		100	200		45	90		30	72	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			97	195		40	80		25	64	ns	
t_{PHL}	Propagation Delay, MR to Q_n		130	260		50	100		35	80	ns	
t_{TLH}	Output Transition Time		60	130		30	70		25	45	ns	
t_{THL}			60	130		30	70		25	45	ns	
$t_w\overline{CP}$	$\overline{CP}$ Minimum Pulse Width	90	45		35	17		28	13		ns	
t_wMR	MR Minimum Pulse Width	80	40		30	15		24	12		ns	
t_{rec}	MR Recovery Time	60	30		25	12		20	9		ns	
f_{MAX}	Input Count Frequency (Note 3)	6	12		15	30		18	36		MHz	

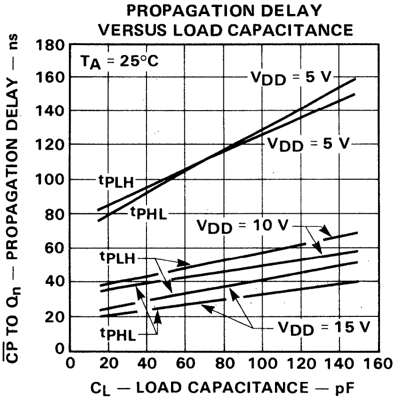
NOTES:

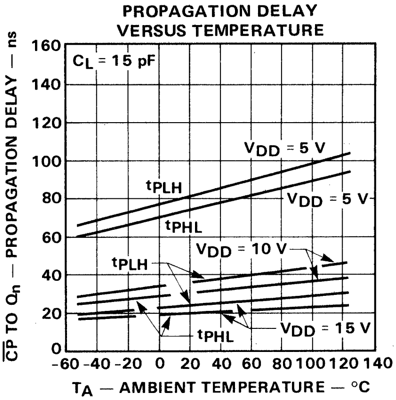
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

TYPICAL ELECTRICAL CHARACTERISTICS

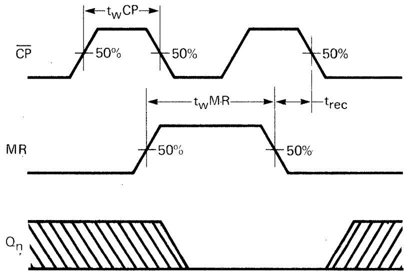

POWER DISSIPATION VERSUS FREQUENCY


CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE


PROPAGATION DELAY VERSUS LOAD CAPACITANCE


PROPAGATION DELAY VERSUS TEMPERATURE

SWITCHING WAVEFORMS



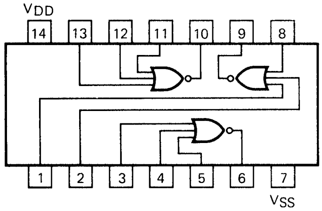
MINIMUM PULSE WIDTH
FOR $\overline{CP}$ AND MR AND MR RECOVERY TIME

4025B

TRIPLE 3-INPUT NOR GATE

DESCRIPTION — This CMOS logic element provides a 3-input positive NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	µA	MIN, 25°C	
					7.5			15			30		MAX	

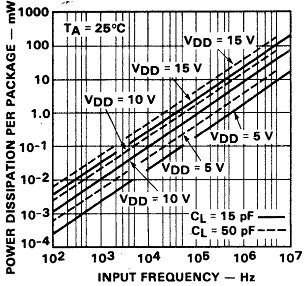
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		45	110		20	60		15	48	ns	C_L = 50 pF,
t_{PHL}			47	110		25	60		21	48	ns	R_L = 200 kΩ
t_{TLH}	Output Transistion Time		38	135		20	70		15	45	ns	Input Transition
t_{THL}			38	135		15	70		11	45	ns	Times ⩽ 20 ns

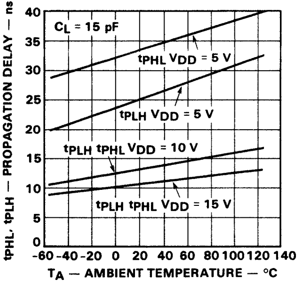
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

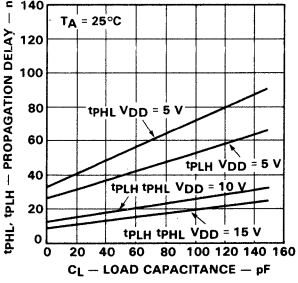
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



4027B

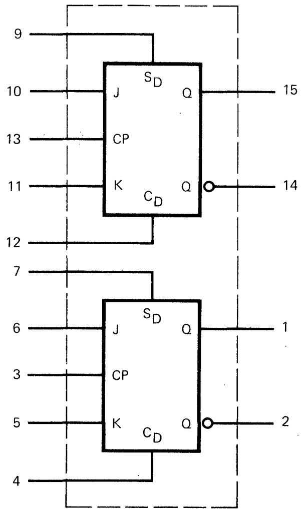
DUAL JK FLIP-FLOP

DESCRIPTION – The 4027B is a Dual JK Flip-Flop which is edge-triggered and features independent Direct Set, Direct Clear, and Clock inputs. Data is accepted when the Clock is LOW and transferred to the output on the positive-going edge of the Clock. The active HIGH asynchronous Clear Direct (C_D) and Set Direct (S_D) are independent and override the J, K, or Clock inputs. The outputs are buffered for best system performance.

PIN NAMES

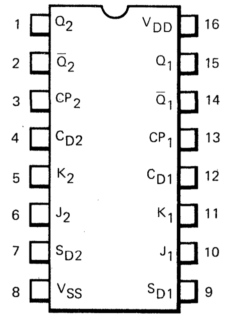
J, K	Synchronous Inputs
CP	Clock Input (L → H Edge-Triggered)
S_D	Asynchronous Direct Set Input (Active HIGH)
C_D	Asynchronous Direct Clear Input (Active HIGH)
Q	True Output
$\overline{Q}$	Complement Output

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLES

ASYNCHRONOUS INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
L	H	L	H
H	L	H	L
H	H	H	H

L = LOW Level
H = HIGH Level
⎍ = Positive-Going Transition
Q_{n+1} = State After Clock Positive Transition

SYNCHRONOUS INPUTS			OUTPUTS	
CP	J	K	Q_{n+1}	$\overline{Q}_{n+1}$
⎍	L	L	NO CHANGE	
⎍	H	L	H	L
⎍	L	H	L	H
⎍	H	H	$\overline{Q}_n$	Q_n

Conditions: $S_D = C_D$ = LOW

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			4			8			16	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					30			60			120		MAX	
		XM			1			2			4	µA	MIN, 25°C	
					30			60			120		MAX	

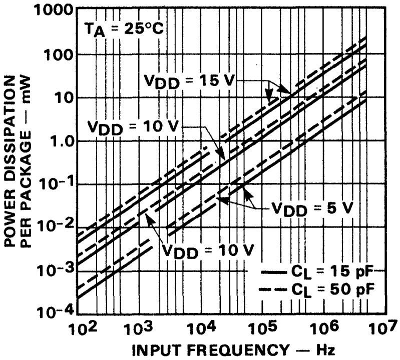
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q, $\overline{Q}$		100	200		45	85		30	68	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			100	200		45	85		30	68	ns	
t_{PLH}	Propagation Delay, S_D to Q		180	350		90	175		75	140	ns	
t_{PHL}	Propagation Delay, C_D to Q		180	350		90	175		75	140	ns	
t_{TLH}	Output Transition Time		85	150		45	85		30	50	ns	
t_{THL}			85	150		45	85		30	50	ns	
t_s	Set-Up Time, J, K to CP	100	45		40	20		32	15		ns	
t_h	Hold Time, J, K to CP	0	-25		0	-10		0	-5		ns	
t_wCP(L)	Minimum Clock Pulse Width	150	75		70	35		56	25		ns	
t_wS_D(H)	Minimum S_D Pulse Width	150	75		60	30		48	25		ns	
$t_wC_{D(H)}$	Minimum C_D Pulse Width	150	75		60	30		48	25		ns	
$t_{rec}S_D$	Recovery Time for S_D	0	-5		0	-4		0	-3		ns	
$t_{rec}C_D$	Recovery Time for C_D	0	-5		0	-4		0	-3		ns	
f_{MAX}	Maximum CP Frequency (Note 2)	4	8		8	16		9	19		MHz	

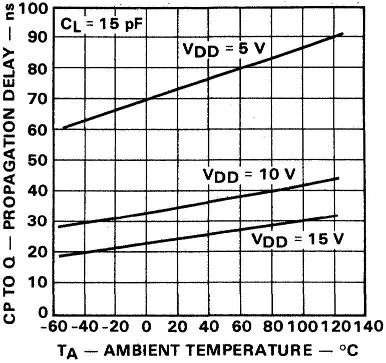
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

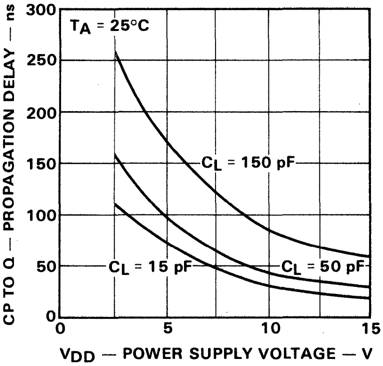
TYPICAL ELECTRICAL CHARACTERISTICS



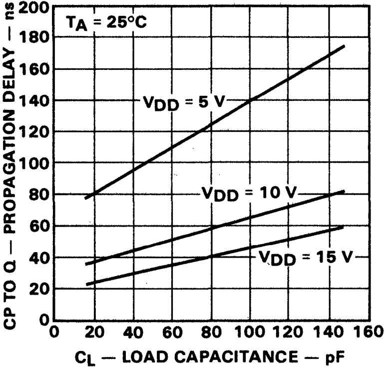
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE

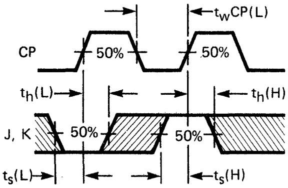


PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE

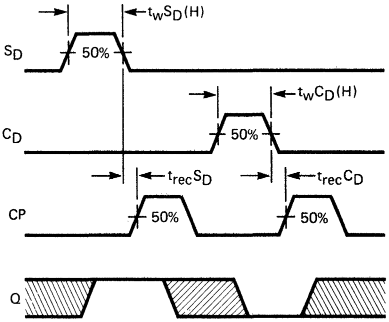


PROPAGATION DELAY VERSUS LOAD CAPACITANCE

SWITCHING WAVEFORMS



NOTE:
t_s & t_h are shown as positive values but may be specified as negative values.



SET-UP TIMES, HOLD TIMES, AND MINIMUM CLOCK PULSE WIDTH

RECOVERY TIME FOR S_D, RECOVERY TIME FOR C_D, MINIMUM S_D PULSE WIDTH, AND MINIMUM C_D PULSE WIDTH

4028B
1-OF-10 DECODER

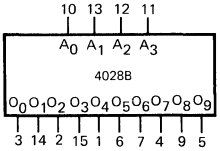
DESCRIPTION – The 4028B is a CMOS 4 Bit BCD to 1-of-10 active HIGH decoder. A 1-2-4-8 BCD code applied to inputs A_0 through A_3 causes the selected output to be HIGH, the other nine will be LOW. If desired, the 4028B may be used as a 1-of-8 decoder with enable; 3-bit octal inputs are applied to inputs A_0, A_1, and A_2 selecting an output 0 through 7. Input A_3 then becomes an active LOW enable, forcing the selected output LOW when A_3 is HIGH. The 4028B may also be used as an 8-input demultiplexer with an active LOW data input. The outputs are fully buffered for best performance.

- **BCD TO 1-OF-10 DECODER**
- **1-OF-8 DECODER WITH ACTIVE LOW ENABLE**
- **8-INPUT DEMULTIPLEXER WITH ACTIVE LOW DATA INPUT**

PIN NAMES

$A_0 - A_3$	Address Inputs, 1-2-4-8 BCD
$O_0 - O_9$	Outputs (Active HIGH)

LOGIC SYMBOL



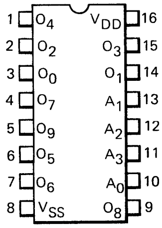
V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUTS				OUTPUTS									
A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9
L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	H	L	H	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L
L	H	L	H	L	L	L	L	L	H	L	L	L	L
L	H	H	L	L	L	L	L	L	L	H	L	L	L
L	H	H	H	L	L	L	L	L	L	L	H	L	L
H	L	L	L	L	L	L	L	L	L	L	L	H	L
H	L	L	H	L	L	L	L	L	L	L	L	L	H
H	L	H	L	L	L	L	L	L	L	L	L	H	L
H	L	H	H	L	L	L	L	L	L	L	L	L	H
H	H	L	L	L	L	L	L	L	L	L	L	H	L
H	H	L	H	L	L	L	L	L	L	L	L	L	H
H	H	H	L	L	L	L	L	L	L	L	L	H	L
H	H	H	H	L	L	L	L	L	L	L	L	L	H

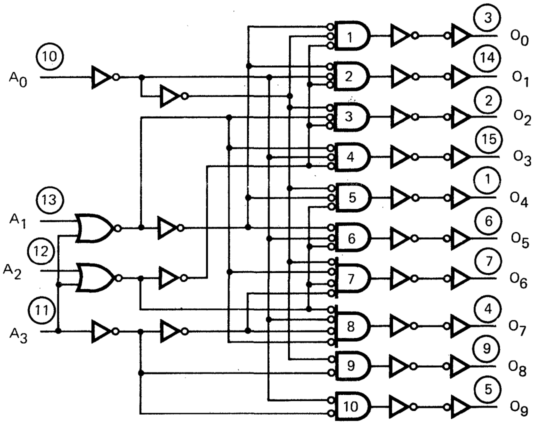
H = HIGH Level
L = LOW Level

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

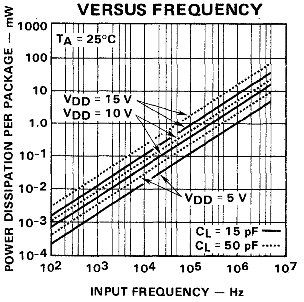
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, A_n to O_n		167	325		66	145		45	53	ns	C_L = 50 pF,
t_{PHL}			157	325		57	145		40	46	ns	R_L = 200 kΩ
t_{TLH}	Output Transistion Time		85	200		40	100		31	70	ns	Input Transition
t_{THL}			110	200		37	100		25	70	ns	Times ≤ 20 ns

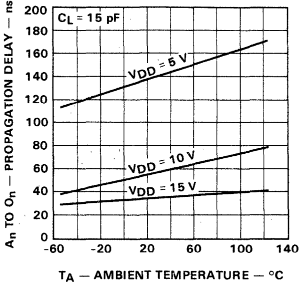
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

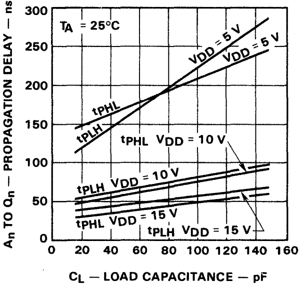
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



4029B

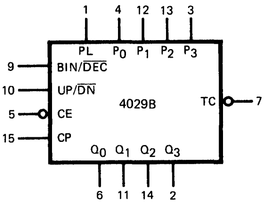
SYNCHRONOUS UP/DOWN COUNTER

DESCRIPTION – The 4029B is a Synchronous Edge-Triggered Up/Down 4-Bit Binary/BCD Decade Counter with a Clock Input (CP), an active LOW Count Enable Input ($\overline{CE}$), an Up/Down Control Input (UP/$\overline{DN}$), a Binary/Decade Control Input (BIN/$\overline{DEC}$), an overriding asynchronous active HIGH Parallel Load Input (PL), four Parallel Data Inputs (P_0-P_3), four Parallel Buffered Outputs (Q_0-Q_3) and an active LOW Terminal Count Output ($\overline{TC}$).

Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions. With the Parallel Load Input (PL) LOW, operation is synchronous and is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). Operation is determined by the three synchronous Mode Control Inputs; UP/$\overline{DN}$, BIN/$\overline{DEC}$ and $\overline{CE}$ (see the Mode Selection Table). These inputs must be stable only during the set-up time prior to the LOW-to-HIGH transition of the Clock Input (CP) and the hold time after this clock transition. The Terminal Count Output ($\overline{TC}$) is LOW when the counter is at its terminal count, as determined by the counting mode, and the Count Enable Input ($\overline{CE}$) is LOW (see Logic Equation for $\overline{TC}$).

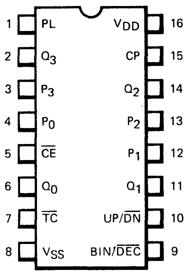
- **BINARY OR DECADE UP/DOWN COUNTER**
- **ASYNCHRONOUS PARALLEL LOAD**
- **ACTIVE LOW COUNT ENABLE**
- **CLOCK EDGE-TRIGGERED ON THE LOW-TO-HIGH TRANSITION**
- **ACTIVE LOW TERMINAL COUNT FOR CASCADING**
- **TYPICAL COUNT FREQUENCY OF 12 MHz AT V_{DD} = 10 V**

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

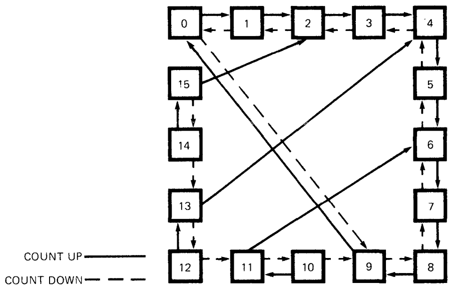
PL	Parallel Load Input
P_0-P_3	Parallel Data Inputs
BIN/$\overline{DEC}$	Binary/Decade Control Input
UP/$\overline{DN}$	Up/Down Control Input
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Input (L→H Edge-Triggered)
Q_0-Q_3	Buffered Parallel Outputs
$\overline{TC}$	Terminal Count Output (Active LOW)

MODE SELECTION TABLE

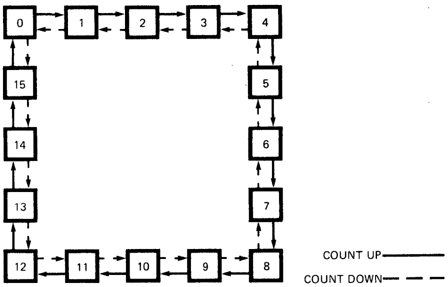
PL	BIN/$\overline{DEC}$	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
H	X	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	X	H	X	No Change
L	L	L	L	⌠	Count Down, Decade
L	L	H	L	⌠	Count Up, Decade
L	H	L	L	⌠	Count Down, Binary
L	H	H	L	⌠	Count Up, Binary

H = HIGH Level
L = LOW Level
X = Don't Care
⌠ = Positive-Going Transition

4029B STATE DIAGRAM, BIN/$\overline{DEC}$ = LOW



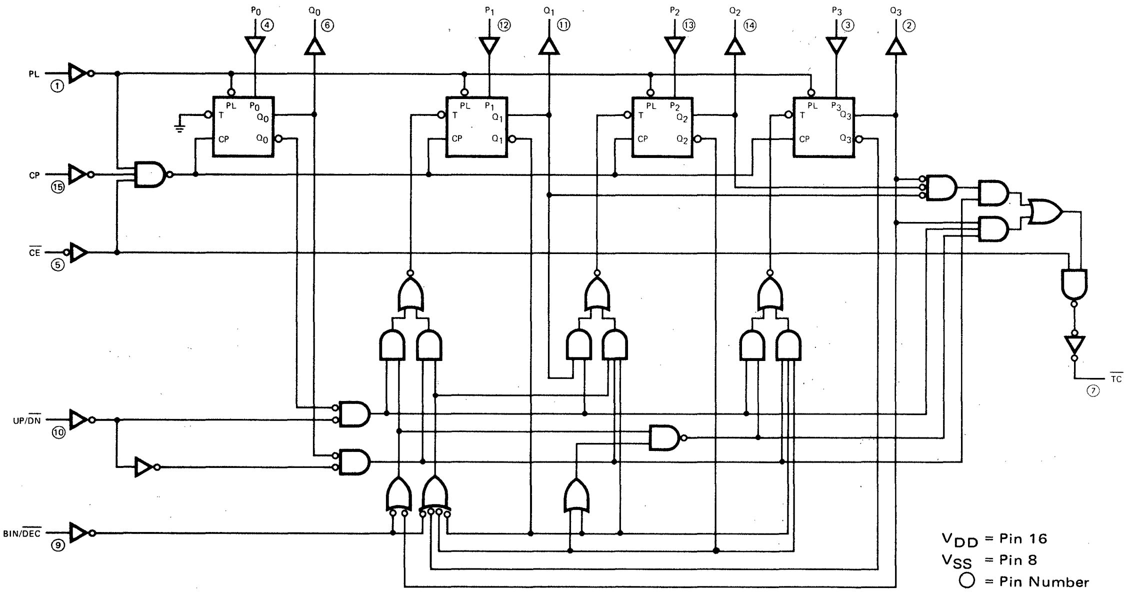
4029B STATE DIAGRAM, BIN/$\overline{DEC}$ = HIGH



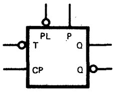
LOGIC EQUATION FOR TERMINAL COUNT

$$TC = CE \bullet [UP \bullet Q_0 \bullet Q_3 \bullet (\overline{BIN} + (Q_1 \bullet Q_2)) + (\overline{UP} \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)]$$

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number



$\overline{PL}$ (Parallel Load Input) — Asynchronously Loads P into Q, Overriding all Other Inputs
P (Parallel Input) — Data on this Pin is Asynchronously Loaded into Q, when $\overline{PL}$ is LOW Overriding all Other Inputs
$\overline{T}$ (Toggle Input) — Forces the Q Output to Synchronously Toggle when a LOW is Placed on this Input.
CP (Clock Pulse Input)
Q, $\overline{Q}$ (True and Complimentary Outputs)

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

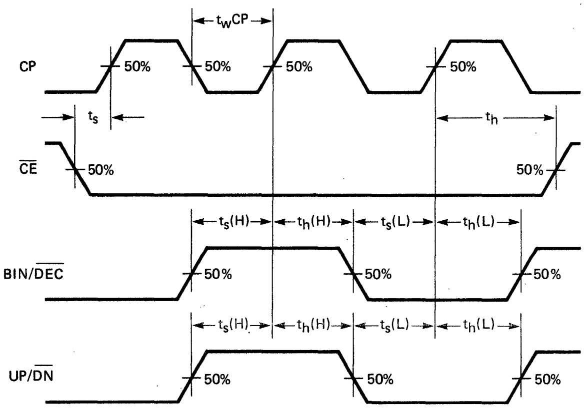
Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

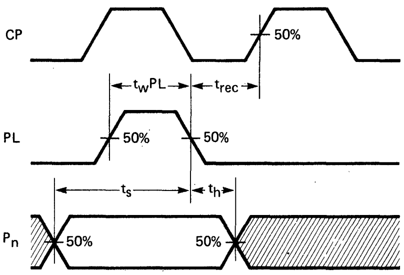
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, CP to Q_n		150	350		62	160		41	128	ns	
t_{PHL}			150	350		59	160		39	128	ns	
t_{PLH}	Propagation Delay, CP to $\overline{TC}$		167	450		71	180		48	144	ns	
t_{PHL}			252	650		100	245		66	196	ns	
t_{PLH}	Propagation Delay, PL to Q_n		170	325		70	150		45	120	ns	
t_{PHL}			220	450		90	195		62	156	ns	
t_{TLH}	Output Transition Time		60	135		31	75		23	45	ns	
t_{THL}			65	135		25	75		18	45	ns	
t_wCP	CP Minimum Pulse Width	125	50		60	21		48	14		ns	C_L = 50 pF,
t_wPL	PL Minumum Pulse Width	150	60		55	21		44	16		ns	R_L = 200 kΩ
t_{rec}	PL Recovery Time	150	62		60	24		48	17		ns	Input Transition
t_s	Set-Up Time, BIN/$\overline{DEC}$ to CP	250	106		100	41		80	29		ns	Times ≤ 20 ns
t_h	Hold Time, BIN/$\overline{DEC}$ to CP	0	-90		0	-35		0	-25		ns	
t_s	Set-Up Time, UP/$\overline{DN}$ to CP	325	145		130	55		104	38		ns	
t_h	Hold Time, UP/$\overline{DN}$ to CP	0	-90		0	-35		0	-25		ns	
t_s	Set-Up Time, $\overline{CE}$ to CP	275	118		120	49		96	23		ns	
t_h	Hold Time, $\overline{CE}$ to CP	0	-40		0	-15		0	-10		ns	
t_s	Set-Up Time, P_n to PL	70	29		30	11		24	8		ns	
t_h	Hold Time, P_n to PL	0	-40		0	-20		0	-20		ns	
f_{MAX}	Input Clock Frequency (Note 2)	2	5		5	12		6	14		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



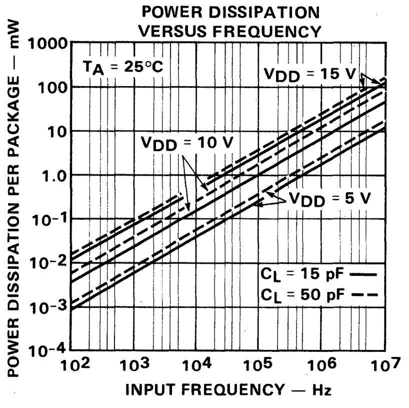
MINIMUM CP WIDTH, SET-UP AND HOLD TIMES, $\overline{CE}$ TO CP, BIN/$\overline{DEC}$ TO CP AND UP/$\overline{DN}$ TO CP

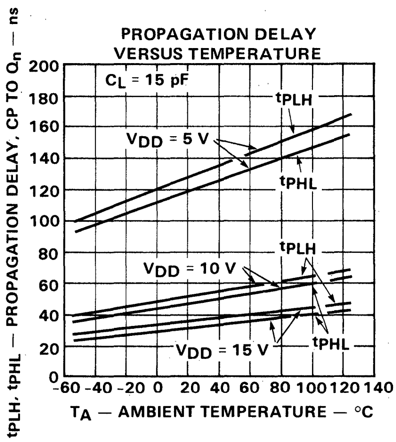


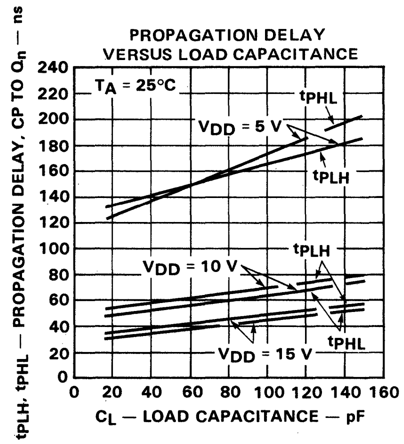
MINIMUM PL PULSE WIDTH, RECOVERY TIME FOR PL, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

TYPICAL ELECTRICAL CHARACTERISTICS


POWER DISSIPATION VERSUS FREQUENCY


PROPAGATION DELAY VERSUS TEMPERATURE


PROPAGATION DELAY VERSUS LOAD CAPACITANCE

APPLICATIONS

Interconnection techniques for multistage counting are shown in Figures 1 through 4. When using the schemes shown in Figures 1, 3 and 4, the BIN/$\overline{\text{DEC}}$ and UP/$\overline{\text{DN}}$ Inputs may be changed only when the Clock Input to the first stage is HIGH. However, when using the scheme shown in Figure 2, UP/$\overline{\text{DN}}$, BIN/$\overline{\text{DEC}}$ and $\overline{\text{CE}}$ may be changed independent of the state of the Clock Input. The methods illustrated in Figures 1 and 3 will operate with long transition times at the Clock Input to the first counter; whereas, the other schemes require a fast transition at the Clock Input.

Figure 1 is a ripple clock expansion scheme in which the maximum counting frequency is limited only by the frequency capability of the first counter. The disadvantage of this technique is that the Outputs of the most significant stage do not change until the clock has rippled through all the preceding stages.

A fully synchronous expansion method is shown in Figure 2. Since the Clock Input is applied simultaneously to all stages, the Outputs of all stages change simultaneously. The maximum counting frequency is limited by the time required for the Count Enable to ripple through all the stages before the next Clock Input is applied.

The semi-synchronous technique illustrated in Figure 3 allows a higher counting frequency than the method shown in Figure 2 by allowing $\overline{\text{TC}}$ to take either 10 or 16 clock periods to ripple from the second stage to the most significant stage (10 clock periods when BIN/$\overline{\text{DEC}}$ = L, 16 clock periods when BIN/$\overline{\text{DEC}}$ = H). The Outputs of all stages, except the first, change simultaneously. The Outputs of the first stage change before the other stages.

The speed advantage of this scheme is lost if the count direction or count modulus is rapidly changed.

The method shown in Figure 4 is the same as in Figure 3 except an external gate is added to reduce the delay between the Clock Input to the first stage and the Clock Input to the following stages.

APPLICATIONS (Cont'd)

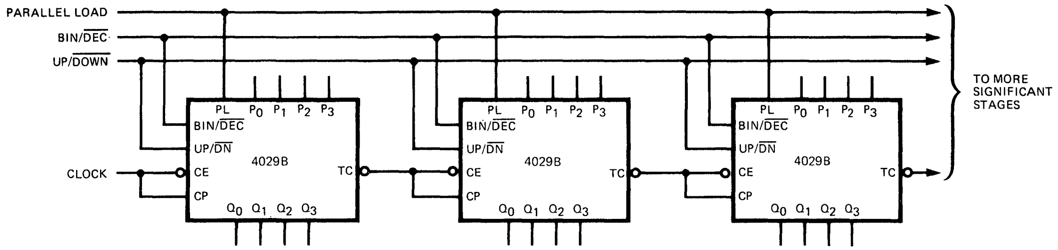


Fig. 1 RIPPLE CLOCK EXPANSION

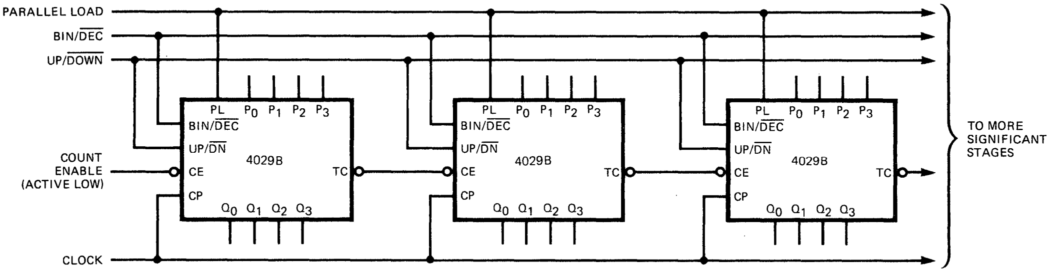


Fig. 2 PARALLEL CLOCK EXPANSION (FULLY SYNCHRONOUS)

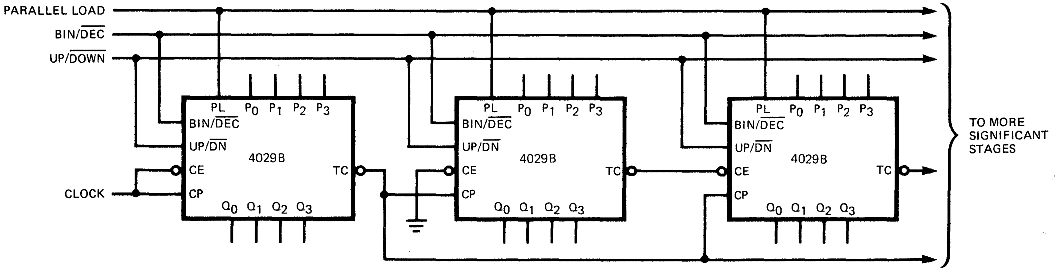


Fig. 3 SEMI-SYNCHRONOUS EXPANSION

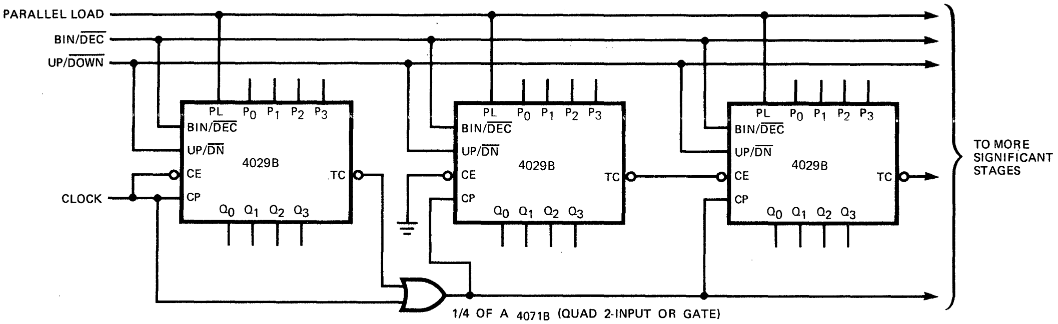


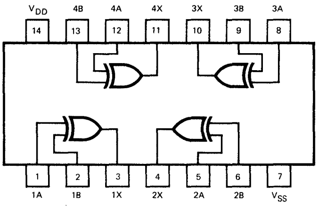
Fig. 4 HIGH SPEED SEMI-SYNCHRONOUS EXPANSION

4030B

QUAD EXCLUSIVE-OR GATE

DESCRIPTION — The 4030B CMOS logic element provides the Exclusive-OR function. The outputs are fully buffered for best performance. The 4030B is a direct replacement for the 74C86/54C86 and the 14507.

F4030 QUAD EXCLUSIVE-OR GATE



$X = \bar{A}B + A\bar{B}$

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

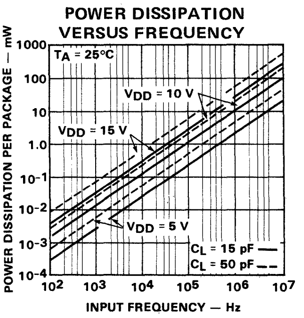
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	µA	MIN, 25°C	
					7.5			15			30		MAX	

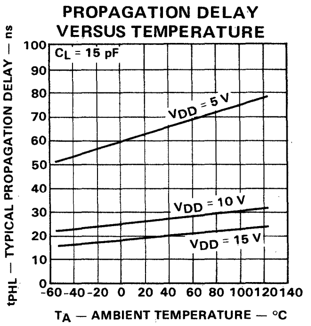
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

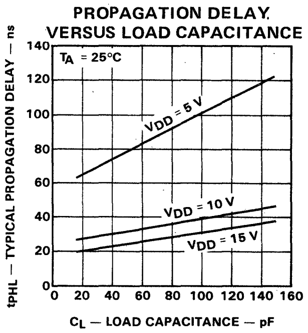
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, A or B to X		85	170		45	90		27	72	ns	C_L = 50 pF,
t_{PHL}			85	170		45	90		27	72	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		50	100		23	50		17	35	ns	Input Transition
t_{THL}			50	100		23	50		17	35	ns	Times ≤ 20 ns

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS


POWER DISSIPATION VERSUS FREQUENCY


PROPAGATION DELAY VERSUS TEMPERATURE


PROPAGATION DELAY VERSUS LOAD CAPACITANCE

4031B

64-STAGE STATIC SHIFT REGISTER

DESCRIPTION – The 4031B is an edge-triggered 64-Stage Static Shift Register with two Serial Data Inputs (D_0, D_1), a Data Select Input (S), a Clock Input (CP), a buffered Clock Output (CO) and buffered Outputs from the 64th bit position (Q_{63}, $\overline{Q_{63}}$).

Data from the selected Data Inputs (D_0 or D_1), as determined by the state of the Select Input (S), is shifted into the first shift register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP). D_0 is selected by a LOW on the Select Input (S) and D_1 is selected by a HIGH on the Select Input (S).

Registers can be cascaded by connecting all the Clock Inputs (CP) together or by driving the Clock Input (CP) of the right-most register with the system clock and connecting the Clock Output (CO) to the Clock Input (CP) of the preceding register. When the second technique is used in the recirculating mode, a flip-flop must be used to store the Output (Q_{63}) of the right-most register until the left-most register is clocked.

- **CLOCK INPUT IS L→H EDGE-TRIGGERED**
- **DATA SELECT INPUT (S) ALLOWS DATA INPUT AT EITHER D_0 OR D_1 INPUTS**
- **EASILY CASCADED**
- **TRUE AND COMPLEMENTARY BUFFERED OUTPUTS AVAILABLE FROM 64TH STAGE**

PIN NAMES

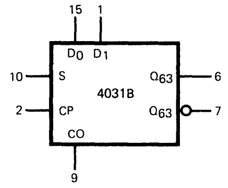
D_0, D_1	Data Inputs
S	Data Select Input
CP	Clock Input (L→H Edge-Triggered)
CO	Buffered Clock Output
Q_{63}	Buffered Output from the 64th Stage
$\overline{Q_{63}}$	Complementary Buffered Output from the 64th Stage

TRUTH TABLE

S	D_0	D_1	Data Into Flip-Flop 1
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

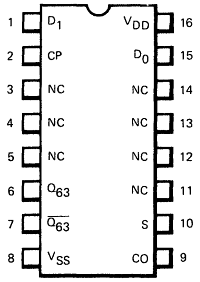
L = Low Level
H = High Level
X = Don't Care

LOGIC SYMBOL



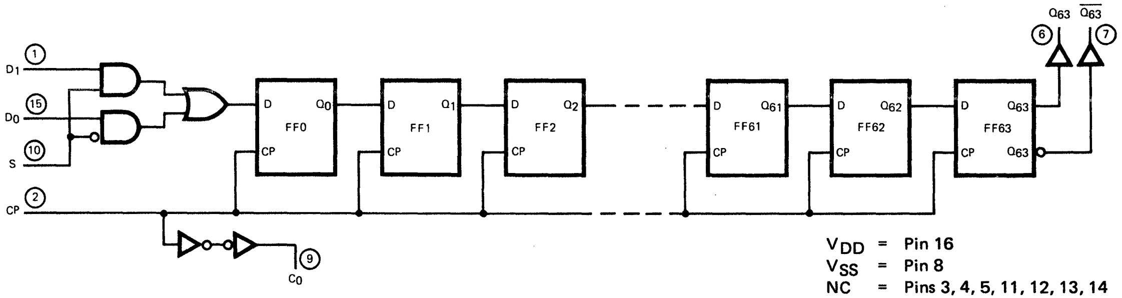
V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pins 3,4,5,11,12,13,14

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpack version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pins 3, 4, 5, 11, 12, 13, 14
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

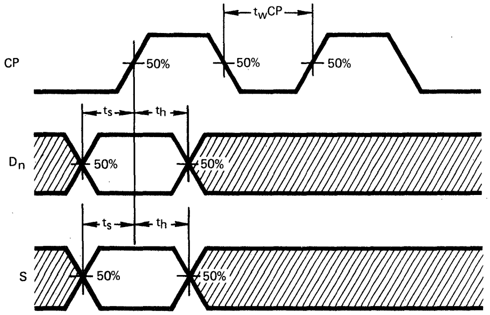
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to Q_{63}, $\overline{Q}_{63}$		120 120			60 60			40 40		ns ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to CO		45 45			25 25			20 20		ns ns	
t_{TLH} t_{THL}	Output Transition Time		65 65			35 35			15 15		ns ns	
$t_wCP(L)$	Minimum Clock Pulse Width		25			10			8		ns	
t_s	Set-Up Time, S to CP		75			40			30		ns	
t_h	Hold Time, S to CP		40			20			15		ns	
t_s	Set-Up Time D_n to CP		75			40			30		ns	
t_h	Hold Time, D_n to CP		40			20			15		ns	
f_{MAX}	Max. Clock Frequency (Note 3)		4			8			9		MHz	

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH, SET-UP AND HOLD TIMES, D_n TO CP AND S TO CP

NOTE: Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

4034B

8-BIT UNIVERSAL BUS REGISTER

GENERAL DESCRIPTION – The 4034B is an 8 Bit Bi-directional Parallel/Serial Input/Output Bus Register with a Serial Data Input (D_S), a Clock Input (CP), an active HIGH asynchronous or synchronous Paralleled Load/Parallel Enable Input ($PL/\overline{PE}$), two mode control inputs, Asynchronous/Synchronous ($A/\overline{S}$) and Data Transfer (P/Q), two sets of eight bi-directional Parallel Data Inputs/Outputs (P_0-P_7 and Q_0-Q_7), and an active HIGH Output Enable Input (EO_P) controlling the P_0-P_7 Parallel Data Inputs/Outputs.

The Data Transfer Mode Control Input (P/Q) determines the direction of data flow. When P/Q is HIGH P_0-P_7 act as a parallel data inputs and Q_0-Q_7 act as parallel data outputs. When P/Q is LOW, Q_0-Q_7 act as parallel data inputs and P_0-P_7 act as parallel data outputs. A LOW on the Output Enable Input (EO_P) forces the P_0-P_7 Input/Outputs to assume a high impedance "OFF" state, regardless of other input conditions.

An Asynchronous/Synchronous ($A/\overline{S}$) Mode Control Input allows either asynchronous or synchronous data transfer. With the $A/\overline{S}$ input HIGH, parallel data may be transferred asynchronously, independent of the Clock Input (CP), at the P_0-P_7 or Q_0-Q_7 Parallel Data Inputs/Outputs with the direction of data transfer dependent upon the state of the P/Q input. Asynchronous parallel data transfer at either P_0-P_7 or Q_0-Q_7 occurs when both the Asynchronous/Synchronous ($A/\overline{S}$) and the Parallel Load/Parallel Enable ($PL/\overline{PE}$) Inputs are HIGH. With the $A/\overline{S}$ input LOW parallel or serial data may be transferred synchronously. Synchronous serial data transfer on the Serial Data Inputs (D_S) occurs on the LOW-to-HIGH transition at the Clock Input (CP) when both $PL/\overline{PE}$ and $A/\overline{S}$ inputs are LOW. With $A/\overline{S}$ LOW and $PL/\overline{PE}$ HIGH, synchronous parallel data transfer on either P_0-P_7 or Q_0-Q_7 occurs on the LOW-to-HIGH transition at the Clock Input (CP). The direction of data transfer is dependent upon the state of the P/Q input.

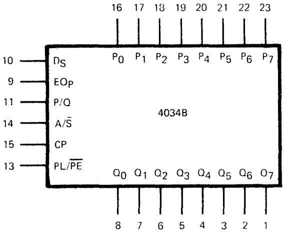
The 4034B is useful in applications requiring bi-directional transfer of parallel data between two data buses, conversion of serial data to parallel form and transfer of the parallel data to either of two data buses, recirculation of parallel data, or acceptance of parallel data from either of two buses for conversion to serial form.

- **BI-DIRECTIONAL DATA TRANSFER**
- **ASYNCHRONOUS OR SYNCHRONOUS PARALLEL OPERATION**
- **SYNCHRONOUS SERIAL OPERATION**
- **3-STATE OUTPUT ENABLE**
- **SERIAL-TO-PARALLEL OR PARALLEL-TO-SERIAL DATA TRANSFER**
- **PARALLEL LOAD OR PARALLEL ENABLE**

PIN NAMES

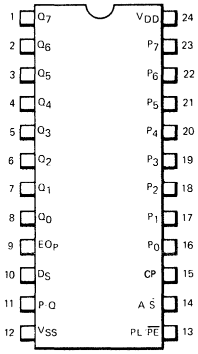
D_S	Serial Data Input
P_0-P_7	Parallel Data Inputs/Outputs
Q_0-Q_7	Parallel Data Inputs/Outputs
$PL/\overline{PE}$	Parallel Load/Parallel Enable Input
CP	Clock Input
$A/\overline{S}$	Asynchronous/Synchronous Mode Control Input
P/Q	Data Transfer Mode Control Input
EO_P	Output Enable Input for Pn Parallel Data Inputs/Outputs

LOGIC SYMBOL



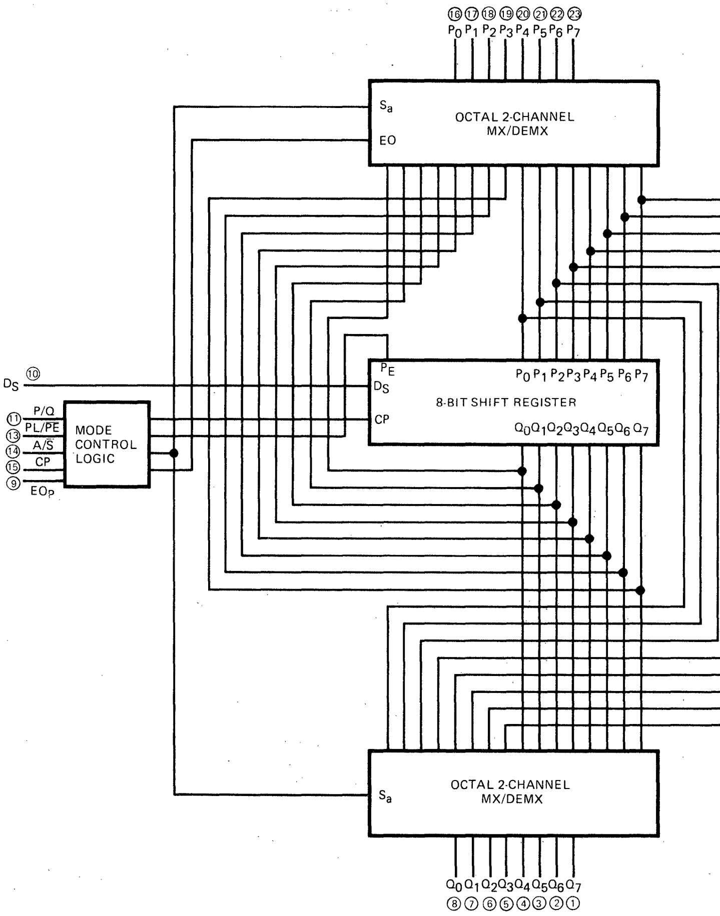
V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAMS
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12
○ = Pin Number

MODE SELECTION TABLE

EO_P	$PL/\overline{PE}$	P/Q	$A/\overline{S}$	MODE	OPERATION
L	L	L	X	Serial	Synchronous Serial data input, P and Q parallel data outputs disabled.
L	L	H	X	Serial	Synchronous Serial data input, Q Parallel data output.
L	H	L	L	Parallel	Q Synchronous Parallel data inputs, P Parallel data outputs disabled.
L	H	L	H	Parallel	Q Asynchronous Parallel data inputs, P Parallel data outputs disabled.
L	H	H	L	Parallel	P Parallel data inputs disabled, Q Parallel data outputs, synchronous data recirculation.
L	H	H	H	Parallel	P Parallel data inputs disabled, Q Parallel data outputs, asynchronous data recirculation.
H	L	L	X	Serial	Synchronous serial data input, P Parallel data output.
H	L	H	X	Serial	Synchronous serial data input, Q Parallel data output.
H	H	L	L	Parallel	Q Synchronous Parallel data input, P Parallel data output.
H	H	L	H	Parallel	Q Asynchronous Parallel data input, P Parallel data output.
H	H	H	L	Parallel	P Synchronous Parallel data input, Q Parallel data output.
H	H	H	H	Parallel	P Asynchronous Parallel data input, Q Parallel data output.

X = Don't Care, H = HIGH Level, L = LOW Level

Note:
Outputs change at positive transition of clock in the serial mode and when the $A/\overline{S}$ input is LOW in the parallel mode.
During transfer from parallel to serial operation, A/S should remain LOW in order to prevent D_S transfer into flip-flops.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC									1.6 12	μA	MIN, 25°C MAX	Output Returned to V_{DD}, $EO_P = V_{SS}$
		XM									0.4 12		MIN, 25°C MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6 -12	μA	MIN, 25°C MAX	Output Returned to V_{SS}, $EO_P = V_{SS}$
		XM									-0.4 -12		MIN, 25°C MAX	
I_{DD}	Quiescent Power Supply Current	XC			20 150			40 300			80 600	μA	MIN, 25°C MAX	All inputs at 0 V or V_{DD}
		XM			5 150			10 300			20 600		MIN, 25°C MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0V, T_A = 25°C (See Note 2)
ASYNCHRONOUS MODE ONLY

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5V			V_{DD} = 10V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, PL/$\overline{PE}$ to		300			160			120		ns	C_L = 50 pF, R_L = 200 Ω Input Transition Times ≤20 ns
t_{PHL}	Qn or Pn		300			160			120		ns	
t_{PLH}	Propagation Delay, A/$\overline{S}$ to		285			150			115		ns	
t_{PHL}	Pn or Qn		285			150			115		ns	
t_WA/$\overline{S}$(H)	A/$\overline{S}$ Minimum Pulse Width (HIGH)		150			75			55		ns	
t_WPL/$\overline{PE}$(H)	PL/$\overline{PE}$ Minimum Pulse Width(HIGH)		150			75			55		ns	
t_WP/Q	P/Q Minimum Pulse Width		150			75			55		ns	
t_s	Set-Up Time, Pn or Qn to PL/$\overline{PE}$		35			15			12		ns	
t_h	Hold-Time, Pn or Qn to PL/$\overline{PE}$		-10			-5			-2		ns	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)
SYNCHRONOUS MODE ONLY

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to		300			155			120		ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤20 ns
t_{PHL}	Q_n or P_n		300			155			120		ns	
t_WCP	CP Minimum Pulse Width		100			50			40		ns	
t_s	Set-Up Time, PL/$\overline{PE}$ to CP		35			15			12		ns	
t_h	Hold Time, PL/$\overline{PE}$ to CP		-10			-5			-2		ns	
t_s	Set-Up Time, D_S to CP		35			15			12		ns	
t_h	Hold Time, D_S to CP		-10			-5			-2		ns	
t_s	Set-Up Time, A/$\overline{S}$ to CP		35			15			12		ns	
t_h	Hold Time, A/$\overline{S}$ to CP		-10			-5			-2		ns	
t_s	Set-Up Time, P/Q to CP		35			15			12		ns	
t_h	Hold Time, P/Q to CP		-10			-5			-2		ns	
f_{MAX}	Input Count Frequency (Note 3)		4			8			9		MHz	

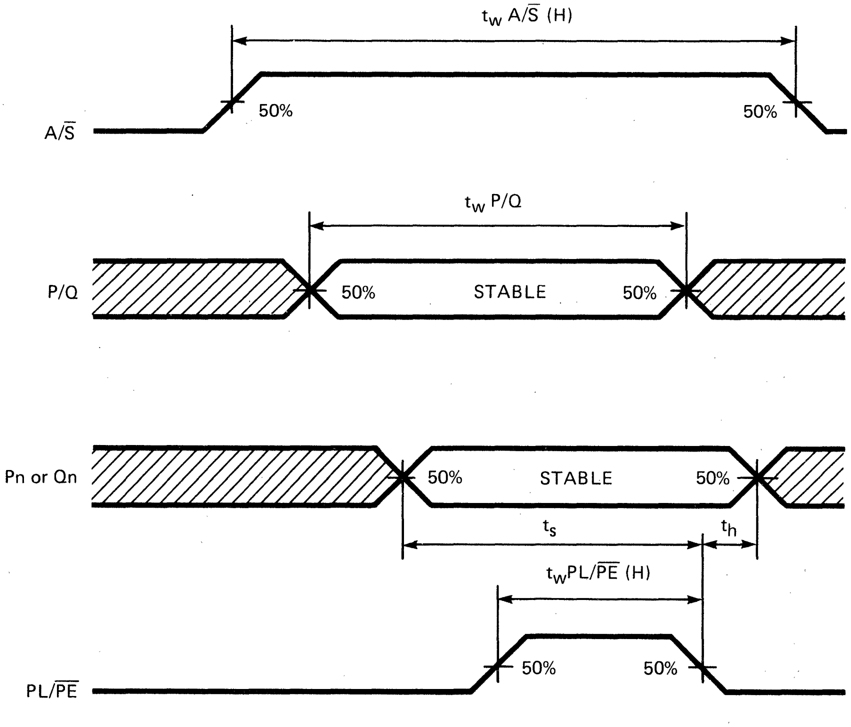
Notes are on the following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0V, T_A = 25°C (See Note 2) ALL MODES OF OPERATION

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5V			V_{DD} = 10V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, P/Q to Qn or Pn		300			160			120		ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽20 ns
t_{PHL}			300			160			120		ns	
t_{PZH}	Output Enable Time (Note 5)		60			37			25		ns	
t_{PZL}			60			37			25		ns	
t_{PHZ}	Output Disable Time (Note 5)		60			37			25		ns	
t_{PLZ}			60			37			25		ns	
t_{TLH}	Output Transition Time		85			45			30		ns	
t_{THL}			85			45			30		ns	
$t_W EO_P(H)$	EO_P Minimum Pulse Width (HIGH)		150			75			55		ns	

Notes:
1. Additional dc characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.
5. For t_{PZH} and t_{PHZ}, R_L = 1 kΩ to V_{SS}. For t_{PZL} and t_{PLZ}, R_L = 1 kΩ to V_{DD}.

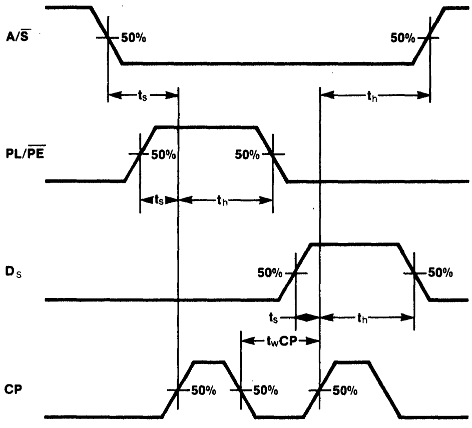
AC WAVEFORMS
ASYNCHRONOUS MODE ONLY



Minimum Pulse Widths for A/$\overline{S}$, P/Q and PL/$\overline{PE}$ and Set-Up and Hold Times Pn or Qn to PL/$\overline{PE}$

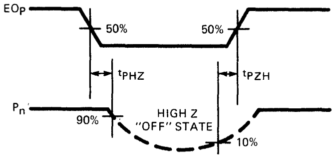
AC WAVEFORMS (Cont'd)

SYNCHRONOUS MODE ONLY

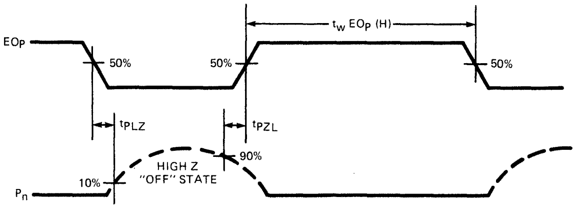


SET–UP AND HOLD–TIMES $A/\overline{S}$ TO CP, $PL/\overline{PE}$ TO CP AND D_S TO CP AND MINIMUM CLOCK PULSE WIDTH

ALL MODES OF OPERATION



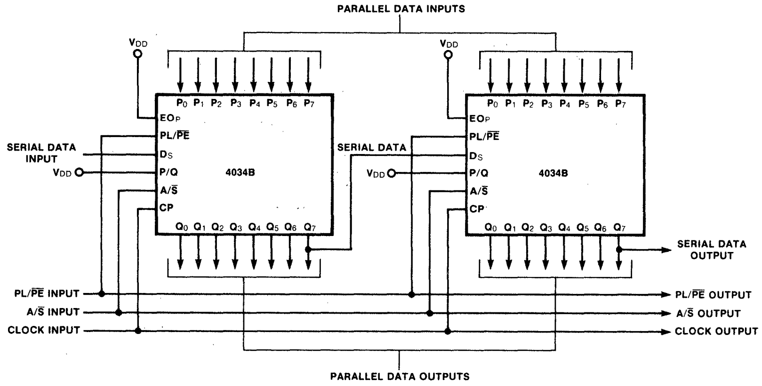
OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}), OUTPUT DISABLE TIME (t_{PLZ}) AND MINIMUM EO_P PULSE WIDTH

NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

TYPICAL APPLICATIONS



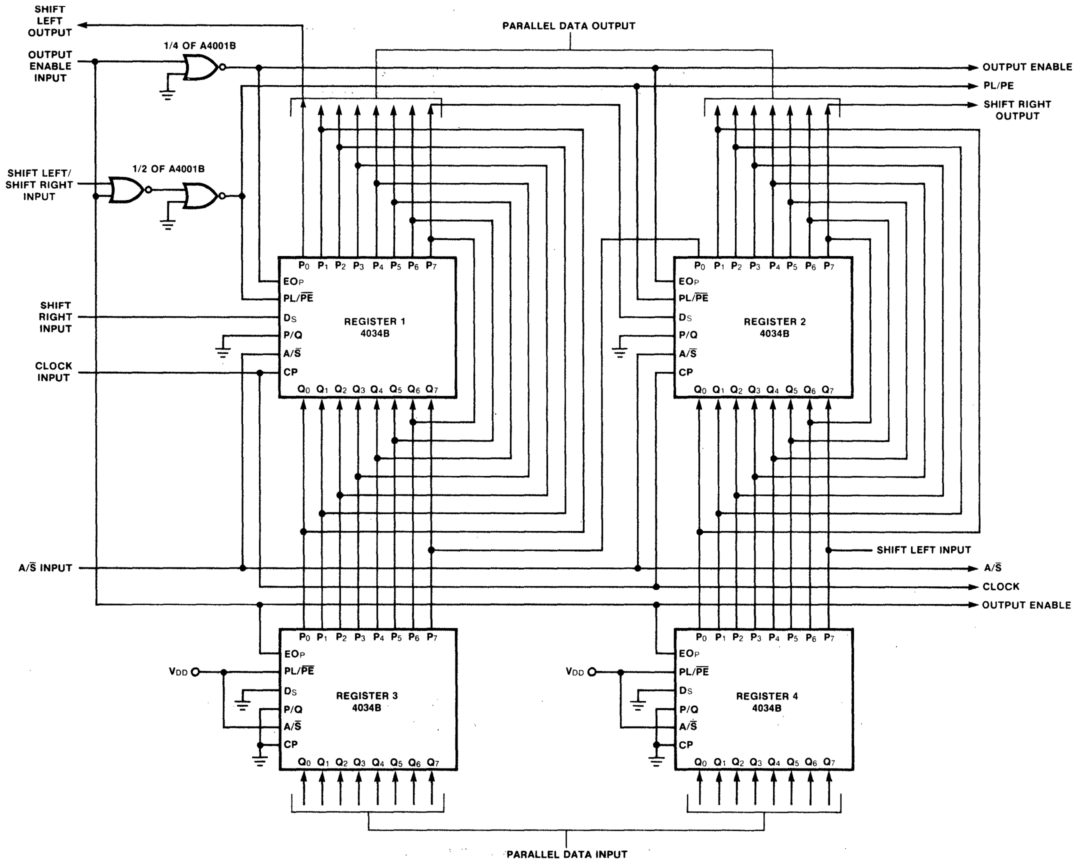


FIG. 2 SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS

NOTE:

A "HIGH" ("LOW") on the Shift Left/Shift Right Input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "HIGH" on the Output Enable Input disables the "P" Parallel Data lines on registers 1 and 2 and enables the "P" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used registers 3 and 4 and associated logic are not required.

The shift left input must be disabled during parallel entry.

4035B

4-BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION — The 4035B is a fully synchronous edge-triggered 4-Bit Shift Register with a Clock Input (CP), four synchronous Parallel Data Inputs (P_0–P_3), two synchronous Serial Data Inputs (J, $\overline{K}$), a synchronous Parallel Enable Input (PE), Buffered Parallel Outputs from all 4-bit positions (Q_0–Q_3), a True/Complement Input (T/$\overline{C}$) and an overriding asynchronous Master Reset Input (MR).

Operation is synchronous (except for Master Reset) and is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is HIGH, data is loaded into the register from Parallel Inputs (P_0–P_3) on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is LOW, data is shifted into the first register position from the Serial Data Inputs (J, $\overline{K}$) and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP). D-type entry is obtained by tying the two Serial Data Inputs (J, $\overline{K}$) together.

The Outputs (Q_0–Q_3) are either inverting or non-inverting, depending on the True/Complement Input (T/$\overline{C}$). With the T/$\overline{C}$ Input HIGH, the Outputs (Q_0–Q_3) are non-inverting (Active HIGH). With the T/$\overline{C}$ Input LOW, the Outputs (Q_0–Q_3) are inverting (Active LOW).

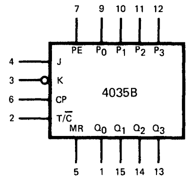
A HIGH on the Master Reset Input (MR) resets all four bit positions (Q_0–Q_3 = LOW if T/$\overline{C}$ = HIGH, Q_0–Q_3 = HIGH if T/$\overline{C}$ = LOW) independent of all other input conditions.

- **TYPICAL SHIFT FREQUENCY OF 17 MHz AT V_{DD} = 10 V**
- **J, $\overline{K}$ INPUTS TO THE FIRST STAGE**
- **T/$\overline{C}$ INPUT FOR TRUE OR COMPLEMENTARY OUTPUTS**
- **SYNCHRONOUS PARALLEL ENABLE**
- **CLOCK EDGE-TRIGGERED ON LOW-TO-HIGH TRANSITION**
- **ASYNCHRONOUS MASTER RESET**

PIN NAMES

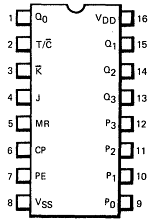
PE	Parallel Enable Input
P_0–P_3	Parallel Data Inputs
J	First Stage J Input (Active HIGH)
$\overline{K}$	First Stage K Input (Active LOW)
CP	Clock Input (L→H Edge-Triggered)
T/$\overline{C}$	True/Complement Input
MR	Master Reset Input
Q_0–Q_3	Buffered Parallel Outputs

LOGIC SYMBOL



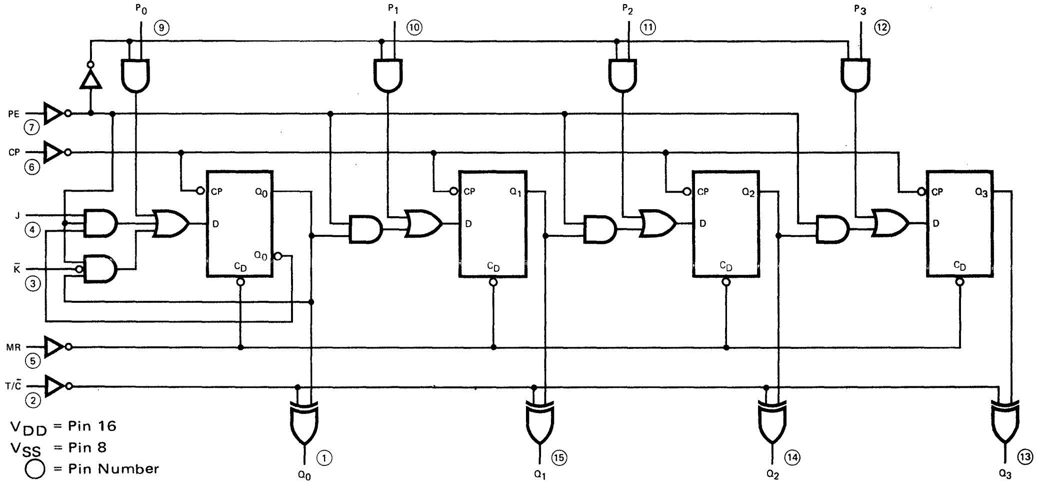
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

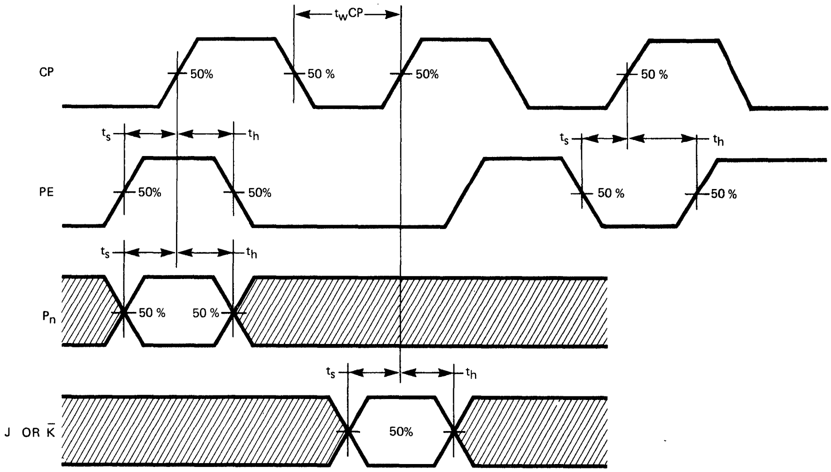
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25°C$ (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to Q_n		200 200	400 400		90 90	180 180		60 60	140 140	ns	$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, MR to Q_n		250 250	500 500		120 120	230 230		75 75	180 180	ns	
t_{PLH} t_{PHL}	Propagation Delay, $T/\overline{C}$ to Q_n		125 125	250 250		55 55	120 120		40 40	95 95	ns	
t_{TLH} t_{THL}	Output Transition Time		85 85	135 135		45 45	75 75		30 30	45 45	ns	
t_wCP	CP Minimum Pulse Width	125	50		55	20		44	14		ns	
t_wMR	MR Minimum Pulse Width	150	60		70	25		56	20		ns	
t_{rec}	MR Recovery Time	120	60		54	30		43	22		ns	
t_s	Set-Up Time, P_n to CP	250	100		110	46		88	32		ns	
t_h	Hold Time, P_n to CP	10	-90		5	-32		0	-22			
t_s	Set-Up Time, PE to CP	250	100		110	46		88	32		ns	
t_h	Hold Time, PE to CP	10	-90		5	-32		0	-22			
t_s	Set-Up Time, J, $\overline{K}$ to CP	275	130		125	48		100	30		ns	
t_h	Hold Time, J, $\overline{K}$ to CP	25	-100		10	-37		5	-23			
f_{MAX}	Maximum Input Clock Frequency (Note 3)	4	8		8	17		10	20		MHz	

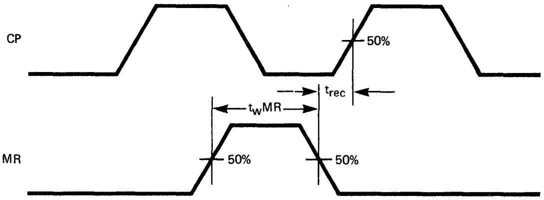
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at $V_{DD} = 5$ V, 4 μs at $V_{DD} = 10$ V, and 3 μs at $V_{DD} = 15$ V.

SWITCHING WAVEFORMS



MINIMUM CP PULSE WIDTH AND SET-UP AND HOLD TIMES, PE TO CP, P_n TO CP, AND J OR $\overline{K}$ TO CP



MR RECOVERY TIME AND MINIMUM MR PULSE WIDTH

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

4040B

12-STAGE BINARY COUNTER

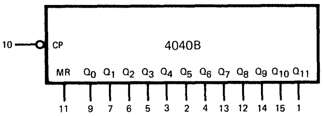
DESCRIPTION – The 4040B is a 12-Stage Binary Ripple Counter with a Clock Input ($\overline{CP}$), an overriding asynchronous Master Reset Input (MR) and twelve fully buffered Outputs (Q_0-Q_{11}). The counter advances on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$). A HIGH on the Master Reset Input (MR) clears all counter stages and forces all Outputs (Q_0 - Q_{11}) LOW, independent of the Clock Input ($\overline{CP}$).

- **25 MHz TYPICAL COUNT FREQUENCY AT V_{DD} = 10 V**
- **CLOCK IS H→L TRIGGERED**
- **COMMON ASYNCHRONOUS MASTER RESET**
- **FULLY BUFFERED OUTPUTS FROM ALL 12 STAGES**

PIN NAMES

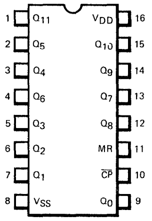
$\overline{CP}$	Clock Input (H→L Triggered)
MR	Master Reset Input (Active HIGH)
Q_0-Q_{11}	Parallel Outputs

LOGIC SYMBOL



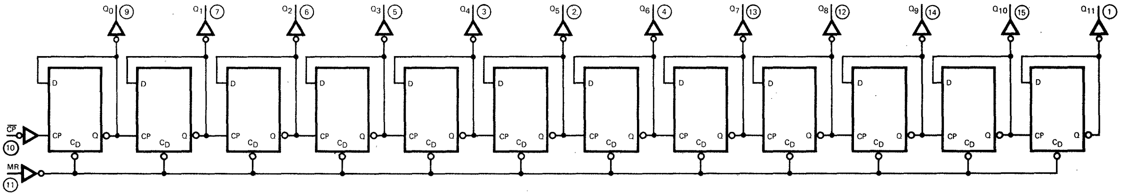
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20 150			40 300			80 600	µA	MIN, 25°C MAX	All inputs at 0 V or V_{DD}
		XM			5 150			10 300			20 600	µA	MIN, 25°C MAX	

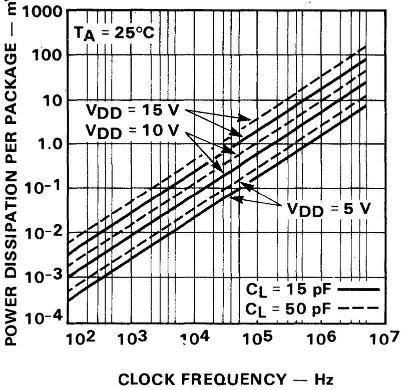
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

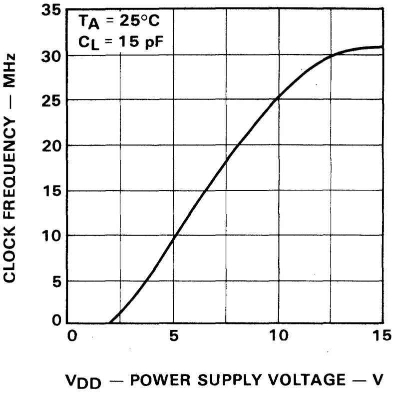
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		130	260		55	110		37	88	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			110	220		45	90		33	72	ns	
t_{PHL}	Propagation Delay, MR to Q_n		180	360		75	150		50	120	ns	
t_{TLH}	Output Transition Time		65	135		35	70		25	45	ns	
t_{THL}			65	135		35	70		25	45	ns	
$t_w\overline{CP}(H)$	Minimum Clock Pulse Width	100	50		40	20		32	16		ns	
$t_wMR(H)$	Minimum MR Pulse Width	140	70		55	27		44	20		ns	
t_{rec}	Recovery Time for MR	85	43		35	17		28	12		ns	
f_{MAX}	Input Clock Frequency (Note 2)	5	10		12	25		14	30		MHz	

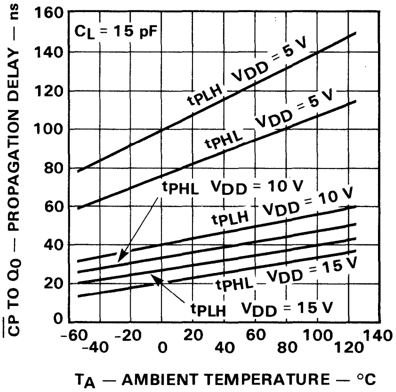
NOTES:

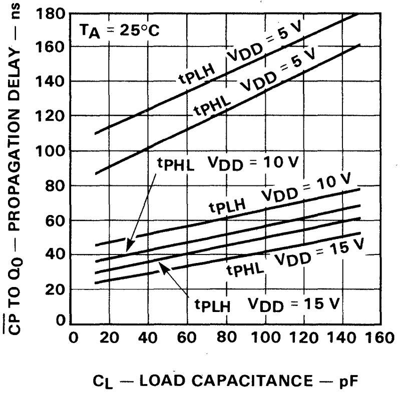
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

TYPICAL ELECTRICAL CHARACTERISTICS

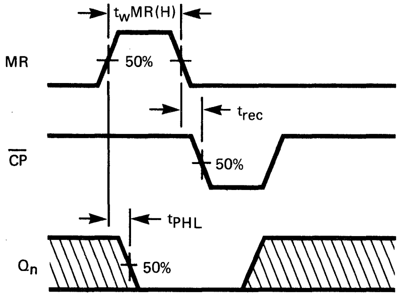

POWER DISSIPATION VERSUS CLOCK FREQUENCY


CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE

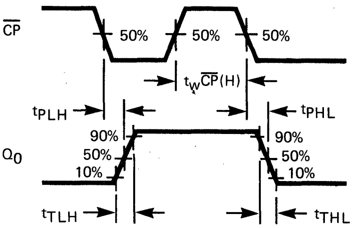

PROPAGATION DELAY VERSUS TEMPERATURE


PROPAGATION DELAY VERSUS LOAD CAPACITANCE

SWITCHING WAVEFORMS



PROPAGATION DELAY MASTER RESET TO OUTPUT, MINIMUM MASTER RESET PULSE WIDTH AND RECOVERY TIME FOR MASTER RESET



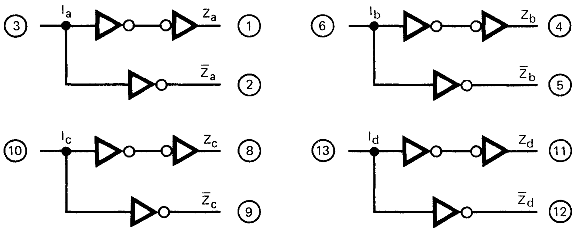
PROPAGATION DELAY CLOCK TO OUTPUT Q_0, OUTPUT TRANSITION TIMES AND MINIMUM CLOCK PULSE WIDTH

4041B

QUAD TRUE/COMPLEMENT BUFFER

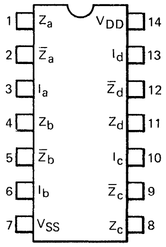
GENERAL DESCRIPTION — The 4041B is a Quad True/Complement Buffer which provides both an inverted active LOW Output ($\overline{Z}$) and a non-inverted active HIGH Output (Z) for each Input (I).

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Number

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

I_a, I_b, I_c, I_d	Buffer Input
Z_a, Z_b, Z_c, Z_d	Buffered True Output
$\overline{Z}a, \overline{Z}_b, \overline{Z}_c, \overline{Z}_d$	Buffered Complementary Output

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OH}	Output HIGH Current		-2.7			-5.4			-15.5			mA	MIN	V_{OUT} = 4.6 V for V_{DD} = 5 V
			-2.25			-4.5			-13				25°C	V_{OUT} = 9.5 V for V_{DD} = 10 V
			-1.6			-3.2			-8.7				MAX	V_{OUT} = 13.5 V for V_{DD} = 15 V
														Inputs at V_{DD} or V_{SS} per Logic Function
I_{OL}	Output LOW Current		2.7			6.25			18			mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 5 V
			2.25			5			15				25°C	V_{OUT} = 0.5 V for V_{DD} = 10 V
			1.6			3.5			10				MAX	V_{OUT} = 1.5 V for V_{DD} = 15 V
														Inputs at V_{DD} or V_{SS} per Logic Function
I_{DD}	Quiescent Power Supply Current	XC			4			8			16	μA	MIN 25°C	All inputs at 0 V or V_{DD}
					30			60			120		MAX	
		XM			1			2			4	μA	MIN 25°C	
					30			60			120		MAX	

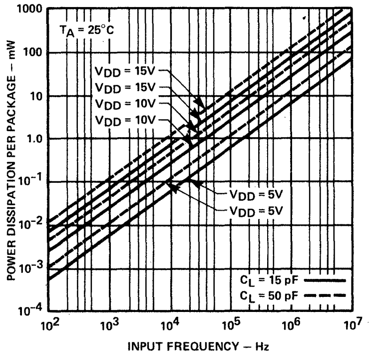
AC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25°C$ (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5V$			$V_{DD} = 10V$			$V_{DD} = 15V$				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		60	125		25	60		20	48	ns	$C_L = 50$ pF,
t_{PHL}			60	125		25	60		20	48	ns	$R_L = 200$ kΩ
t_{TLH}	Output Transition Time		30	75		15	40		12	30	ns	Input Transition
t_{THL}			30	75		15	40		12	30	ns	Times ≤20 ns

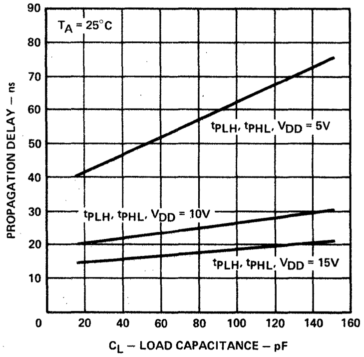
NOTES:
1. Additional dc characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation delays and output transition times are graphically described in this section under 4000 B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

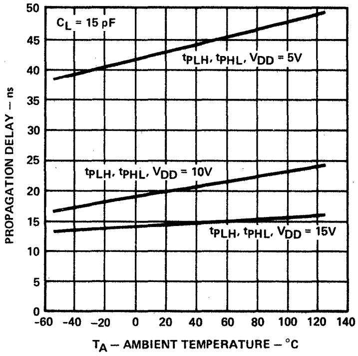
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



PROPAGATION DELAY VERSUS TEMPERATURE



4042B

QUAD D LATCH

DESCRIPTION – The 4042B is a 4-Bit Latch with four Data Inputs (D_0-D_3), four buffered Latch Outputs (Q_0-Q_3), four buffered Complementary Latch Outputs ($\overline{Q}_0$-$\overline{Q}_3$) and two Common Enable Inputs (E_0 and E_1). Information on the Data Inputs (D_0-D_3) is transferred to the Outputs (Q_0-Q_3) while both Enable Inputs (E_0, E_1) are in the same state, either HIGH or LOW. The Outputs (Q_0-Q_3) follow the Data Inputs (D_0-D_3) as long as both Enable Inputs (E_0, E_1) remain in the same state. When the two Enable Inputs (E_0, E_1) are different, the Data Inputs (D_0-D_3) do not affect the Outputs (Q_0-Q_3) and the information in the latch is stored. The $\overline{Q}_0$–$\overline{Q}_3$ Outputs are always the complement of the Q_0-Q_3 Outputs. The Exclusive-OR input structure allows the choice of either polarity for the Enable Input. With one Enable Input HIGH, the other Enable Input is active HIGH; with one Enable Input LOW, the other Enable Input is active LOW.

The last moment prior to the trailing end of the enable condition that the Latch Outputs can still be affected by the inputs is specified as a set-up time. A negative set-up time, as typically exhibited by this device, means that the latches respond to input changes after the end of the enable condition. Following established industry practice, a hold time is specified, defining the time after the end of the enable condition, that the inputs must be held stable, so that they do not affect the state of the latches. It follows from this definition, that the hold time is identical with the negative set-up time. Set-up and hold times have a tolerance, due to manufacturing process variations, temperature and supply voltage changes. For predictable operation the data input levels must be held stable over the full spread of this timing window starting with the earliest set-up time (largest positive or smallest negative value) to the latest hold time.

- **ACTIVE HIGH OR ACTIVE LOW ENABLE**
- **TRUE AND COMPLEMENTARY OUTPUTS (Q & $\overline{Q}$)**

PIN NAMES

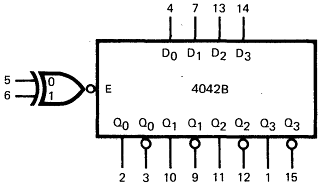
D_0-D_3	Data Inputs
E_0, E_1	Enable Inputs
Q_0-Q_3	Parallel Latch Outputs
$\overline{Q}_0$-$\overline{Q}_3$	Complementary Parallel Latch Outputs

TRUTH TABLE

E_0	E_1	LATCH CONDITION
L	L	Enabled
L	H	Not Enabled
H	L	Not Enabled
H	H	Enabled

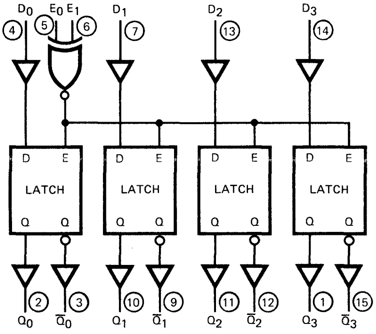
L = LOW Level
H = HIGH Level

LOGIC SYMBOL



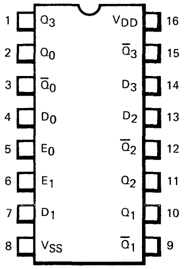
V_{DD} = Pin 16.
V_{SS} = Pin 8

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

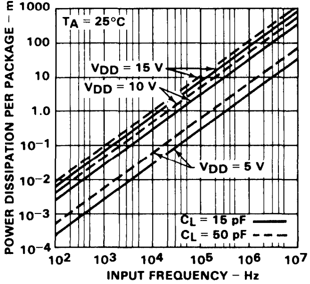
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, Data to Output		101	200		45	90		33	72	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			99	200		44	88		33	70	ns	
t_{PLH}	Propagation Delay, Enable to Output		156	310		66	132		47	106	ns	
t_{PHL}			137	275		58	116		41	93	ns	
t_{TLH}	Output Transition Time		65	135		31	70		25	45	ns	
t_{THL}			60	135		26	70		20	45	ns	
t_s	Set-Up Time, D_n to E_0 or E_1	10	-12		10	-6		8	-4		ns	
t_h	Hold Time, D_n to E_0 or E_1	50	25		25	13		20	7		ns	
t_wE_n	Minimum Enable Pulse Width	80	40		32	16		26	12		ns	

NOTES:

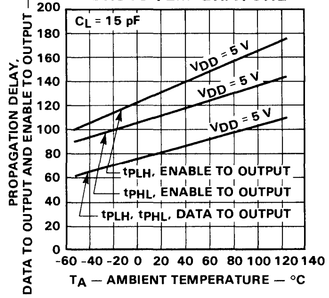
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

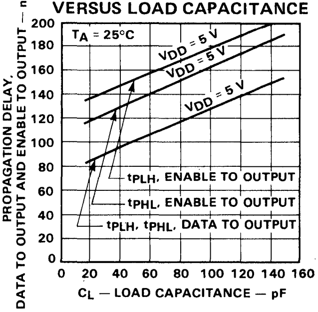
TYPICAL POWER DISSIPATION VERSUS FREQUENCY



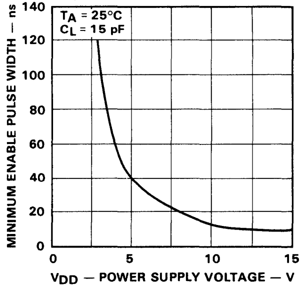
PROPAGATION DELAY VERSUS TEMPERATURE



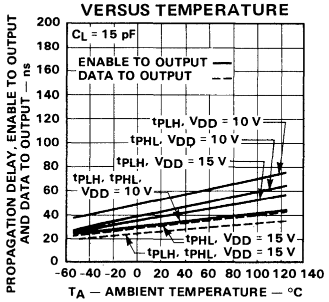
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



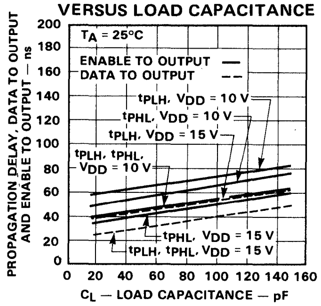
MINIMUM ENABLE PULSE WIDTH VERSUS POWER SUPPLY VOLTAGE



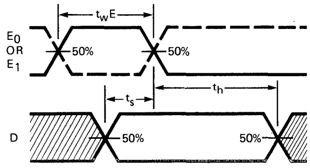
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

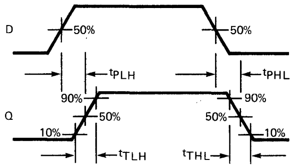


SWITCHING WAVEFORMS

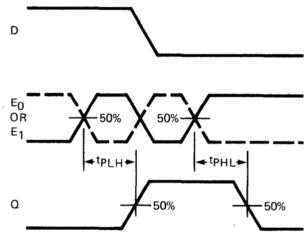


SET-UP AND HOLD TIMES, MINIMUM ENABLE PULSE WIDTH

NOTE:
Either E_0 or E_1 is held HIGH or LOW while the other Enable Input is pulsed as per the Truth Table. t_s and t_h are shown as positive values but may be specified as negative values.



PROPAGATION DELAY DATA TO OUTPUT AND TRANSITION TIMES, WITH LATCH ENABLED



PROPAGATION DELAY ENABLE TO OUTPUT

NOTE:
Either E_0 or E_1 is held HIGH or LOW while the other Enable Input is pulsed as per the Truth Table.

4043B

QUAD R/S LATCH WITH 3-STATE OUTPUTS

DESCRIPTION – The 4043B is a Quad R/S Latch with 3-State Outputs with a common Output Enable (EO). Each latch has an active HIGH Set Input (S_n), an active HIGH Reset Input (R_n) and an active HIGH 3-State Output (Q_n).

When the Output Enable Input (EO) is HIGH, the state of the Latch Outputs (Q_n) can be determined from the Truth Table (see below). When the Output Enable Input (EO) is LOW, the Latch Outputs are in the high impedance OFF state. The Output Enable Input (EO) does not affect the state of the latch.

- **3-STATE BUFFERED OUTPUTS (ACTIVE HIGH)**
- **COMMON OUTPUT ENABLE**
- **SET INPUTS TO EACH LATCH (ACTIVE HIGH)**
- **RESET INPUTS TO EACH LATCH (ACTIVE HIGH)**

PIN NAMES

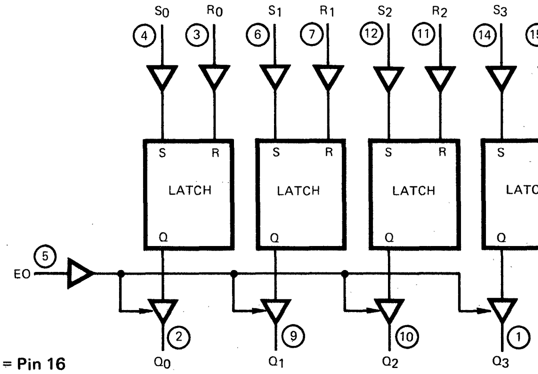
EO	Common Output Enable Input
S_0–S_3	Set Inputs
R_0–R_3	Reset Inputs
Q_0–Q_3	3-State Buffered Latch Outputs

TRUTH TABLE

INPUTS			OUTPUT
EO	S_n	R_n	Q_n
L	X	X	High Impedance
H	H	L	H
H	L	H	L
H	H	H	H
H	L	L	No Change

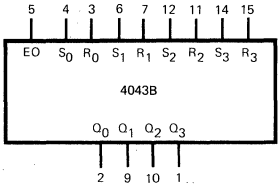
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC DIAGRAM



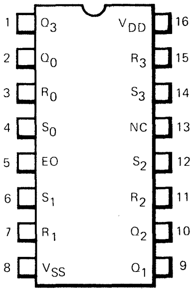
V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 13
○ = Pin Number

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 13

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpack version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC									1.6	µA	MIN, 25°C	Output Returned to V_{DD}, EO = V_{SS}
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	µA	MIN, 25°C	Output Returned to V_{SS} EO = V_{SS}
											- 12		MAX	
		XM									-0.4		MIN, 25°C	
											- 12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20		MIN, 25°C	
					150			300			600		MAX	

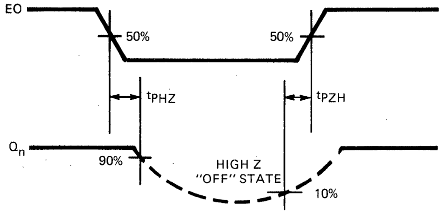
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, S_n to Q_n		80	145		30	70		24	56	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}	Propagation Delay, R_n to Q_n		75	135		25	60		20	48	ns	
t_{PZH}	Output Enable Time		30	55		20	40		15	32	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			40	75		20	40		15	32	ns	(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable Time		20	45		20	40		18	32	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			30	55		20	40		15	32	ns	(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		60	135		30	75		20	45	ns	
t_{THL}			60	135		30	75		20	45	ns	
t_WS_n	Minimum S_n Pulse Width	60	32		30	13		24	15		ns	
t_WR_n	Minimum R_n Pulse Width	60	32		30	13		24	15		ns	

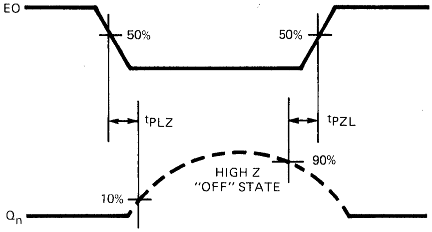
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

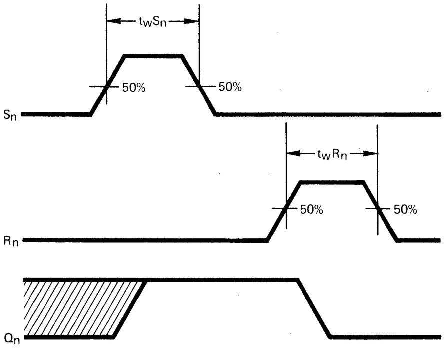
SWITCHING WAVEFORMS



OUTPUT ENABLE TIME
(t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



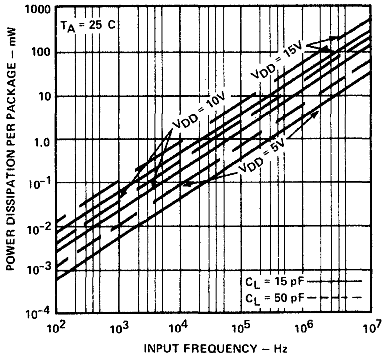
OUTPUT ENABLE TIME
(t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})



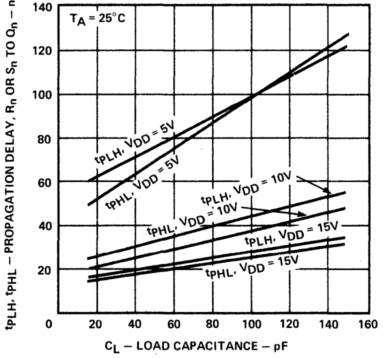
MINIMUM R_N AND S_N PULSE WIDTHS
AND RECOVERY TIMES FOR R_N AND S_N

TYPICAL ELECTRICAL CHARACTERISTICS

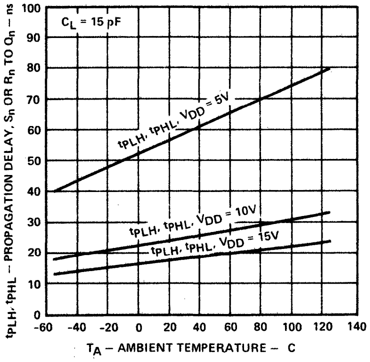
POWER DISSIPATION VERSUS INPUT FREQUENCY



PROPAGATION DELAY, R_n OR S_n TO Q_n, VERSUS LOAD CAPACITANCE



PROPAGATION DELAY, R_n OR S_n TO Q_n, VERSUS TEMPERATURE



4044B

QUAD R/S LATCH WITH 3-STATE OUTPUTS

DESCRIPTION – The 4044B is a Quad R/S Latch with 3-state Outputs with a common Output Enable Input (EO). Each latch has an active LOW Set Input ($\overline{S}_n$), an active LOW Reset Input ($\overline{R}_n$) and an active HIGH 3-State Output (Q_n).

When the Output Enable Input (EO), is HIGH, the state of the Latch Outputs (Q_n) can be determined from the Truth Table (see below). When the Output Enable Input (EO) is LOW, the Latch Outputs are in the high impedance OFF state. The Output Enable Input (EO) does not affect the state of the latch.

- **3-STATE BUFFERED OUTPUTS (ACTIVE HIGH)**
- **COMMON OUTPUT ENABLE**
- **SET INPUTS TO EACH LATCH (ACTIVE LOW)**
- **RESET INPUTS TO EACH LATCH (ACTIVE LOW)**

PIN NAMES

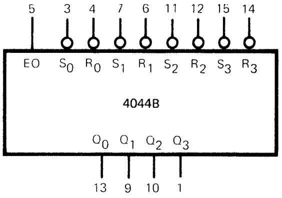
EO	Output Enable Input
$\overline{S}_0$–$\overline{S}_3$	Set Inputs (Active LOW)
$\overline{R}_0$–$\overline{R}_3$	Reset Inputs (Active LOW)
Q_0–Q_3	3-State Buffered Latch Outputs

TRUTH TABLE

INPUTS			OUTPUT
EO	$\overline{S}_n$	$\overline{R}_n$	Q_n
L	X	X	High Impedance
H	L	H	H
H	H	L	L
H	L	L	L
H	H	H	No Change

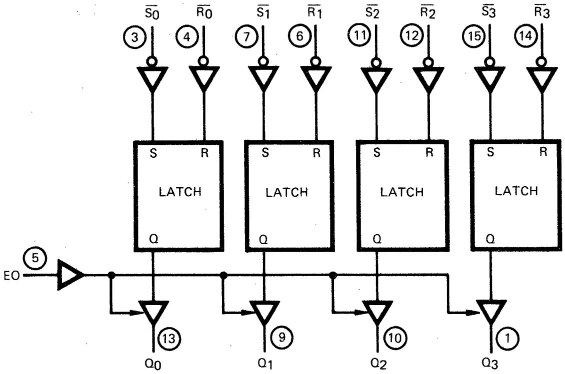
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC SYMBOL



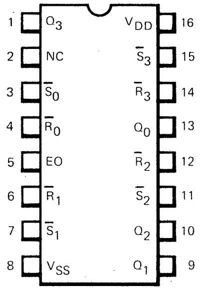
V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 2

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 2
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpack version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DD}, EO = V_{SS}
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	μA	MIN, 25°C	Output Returned to V_{SS}, EO = V_{SS}
											- 12		MAX	
		XM									-0.4		MIN, 25°C	
											- 12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			4			8			16	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					30			60			120		MAX	
		XM			1			2			4		MIN, 25°C	
					30			60			120		MAX	

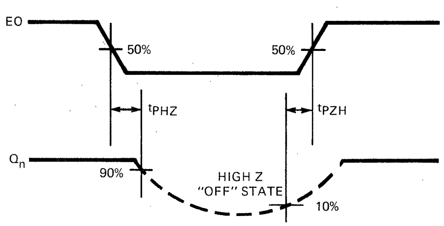
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{S}_n$ to Q_n		70	135		30	65		24	52	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}	Propagation Delay, $\overline{R}_n$ to Q_n		70	135		30	65		20	52	ns	
t_{PZH}	Output Enable Time		30	70		15	40		12	32	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			42	90		20	50		15	40	ns	(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable Time		22	55		20	50		15	40	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			30	70		20	50		15	40	ns	(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		60	135		30	75		20	45	ns	
t_{THL}			60	135		30	75		20	45	ns	
$t_w\overline{S}_n$	Minimum $\overline{S}_n$ Pulse Width	55	27		25	14		20	10		ns	
$t_w\overline{R}_n$	Minimum $\overline{R}_n$ Pulse Width	55	27		25	14		20	10		ns	

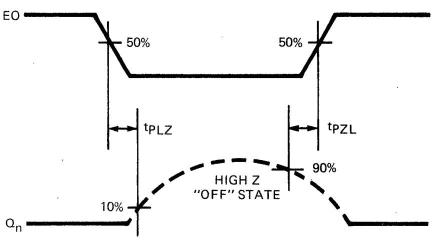
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

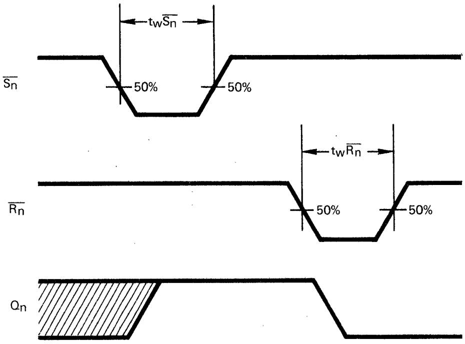
SWITCHING WAVEFORMS



OUTPUT ENABLE TIME
(t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



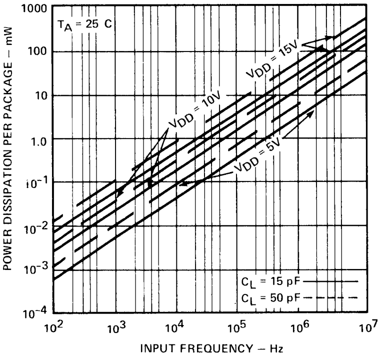
OUTPUT ENABLE TIME
(t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})



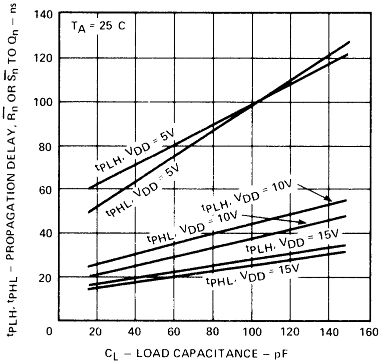
MINIMUM $\overline{S_N}$ AND $\overline{R_N}$ PULSE WIDTHS

TYPICAL ELECTRICAL CHARACTERISTICS

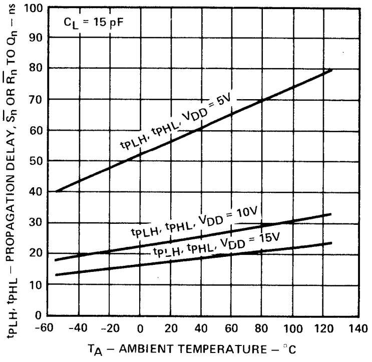
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY, $\overline{R}_n$ OR $\overline{S}_n$ TO Q_n VERSUS LOAD CAPACITANCE



PROPAGATION DELAY $\overline{S}_n$ OR $\overline{R}_n$ TO Q_n VERSUS TEMPERATURE



4045B

21-STAGE BINARY COUNTER

GENERAL DESCRIPTION – The 4045B is a timing circuit consisting of an on-chip crystal oscillator circuit, a 21-stage binary ripple counter, two output pulse shaping circuits, two output buffers and one 20V Zener diode for protection against power supply transients. The device has an External Crystal Input (I_X), an External Crystal Output (0_X), source connections to the n-channel and p-channel transistors of the oscillator circuit (S_N and S_P), and a Data Output (Q_{20}) and Complimentary Data Output ($\overline{Q_{20}}$) from the 21st stage of the binary ripple counter, both with 0.03125% duty cycles.

The 4045B may be used with an external crystal oscillator circuit as shown in the Block Diagram or an external clock pulse may be applied to the Crystal Output (O_X) with the Crystal Input (I_X) tied to the Crystal Output (O_X) and to the source connections (Sp and S_N). A Schmitt trigger is provided to allow slow rise and fall times on the External Clock Input signal.

The crystal oscillator circuit can be made less sensitive to variations in the power supply voltage by adding external resistors R_1 and R_2 (see block diagram). If these external resistors are not required, source connection S_P must be tied to V_{DD} and source connection S_N must be tied to V_{SS}.

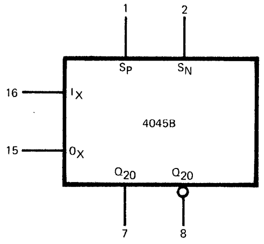
The Buffered Output (Q_{20}) provides an Output signal with a frequency of $1/2^{21}$ times the input frequency and a duty cycle of 0.03125%. The Complimentary Buffered Output provides the same output signal with a 180° phase shift from Q_{20}. As shown in the Block Diagram, an input frequency of 2.097152 MHz will yield output signals with frequencies of 1 Hz duty cycles of 1/32 seconds and a phase shift (between Q_{20} and $\overline{Q_{20}}$) of a one-half second.

- **ON-CHIP CRYSTAL OSCILLATOR OR EXTERNAL CLOCK INPUT**
- **HIGH OUTPUT DRIVE CAPABILITY**
- **EXTERNAL SOURCE CONNECTIONS FOR IMPROVED TIMING STABILITY**
- **ON-CHIP ZENER DIODES FOR SUPPLY REGULATION**

PIN NAMES

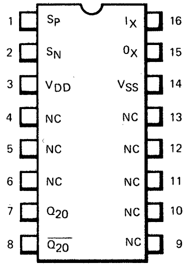
I_X	External Crystal Input
S_P	Source Connection-to-p-channel transistor
S_N	Source Connection-to-n-channel transistor
0_X	External Crystal Output
Q_{20}	Data Output
$\overline{Q_{20}}$	Complimentary Data Output

LOGIC SYMBOL



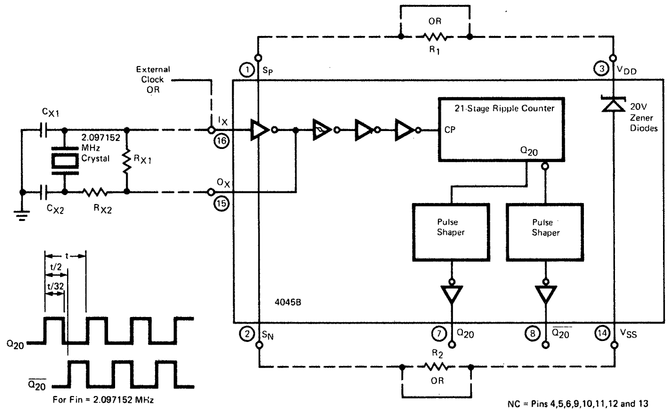
V_{DD} = PIN 3
V_{SS} = PIN 14
NC = PINS 4, 5, 6, 9, 10, 11, 12 AND 13

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

BLOCK DIAGRAM



For Fin = 2.097152 MHz
t = 1 second

NC = Pins 4,5,6,9,10,11,12 and 13
○ = Pin Number

4046B

MICROPOWER PHASE-LOCKED LOOP

DESCRIPTION — The 4046B is a Micropower Phase-Locked Loop consisting of a low power linear Voltage-Controlled Oscillator, a Source Follower Circuit, two different Phase Comparators, and a Zener diode. The Voltage-Controlled Oscillator has two External Capacitor connections (C_{exta}, C_{extb}), two External Resistor connections (R_{exta}, R_{extb}), a Voltage-Controlled Oscillator Input (I_{VCO}) and a Voltage-Controlled Oscillator Output (O_{VCO}). The Source Follower Circuit provides a Demodulated Output (O_D) from the Voltage-Controlled Oscillator. An active LOW Enable Input ($\overline{E}$) common to both the Voltage-Controlled Oscillator and the Source Follower Circuit is also provided. Phase Comparator I and Phase Comparator II have common Signal (I_S) and Comparator (I_C) Inputs and separate outputs; Phase Comparator I Output (O_{PCI}), Phase Comparator II Output (O_{PCII}), and Phase Pulse Output (O_{PII}). An input to the Zener diode (I_Z) is also provided.

The Voltage-Controlled Oscillator requires one external capacitor (C_1) and one external resistor (R_1) to determine operational frequency range. A second external resistor (R_2) may be used to allow frequency offset. External resistor R_3 and external capacitor C_2 combined serve as a low pass filter to the Voltage-Controlled Oscillator Input (I_{VCO}). Output O_D is provided to avoid loading the low pass filter. External resistor R_4 is required if this output is utilized. O_D must be left open when not utilized. The output from the Voltage-Controlled Oscillator (O_{VCO}) may be connected directly or indirectly through CMOS frequency dividers (i.e., the 4018B, 4020B, 4022B, 4024B, 4029B, 4040B, 4518B, 4520B, 40160B, 40161B, 40162B, 40163B, 40192B or 40193B) to the Comparator Input (I_C). With the Enable Input (E) HIGH both the Voltage-Controlled Oscillator and the Source Follower Circuit are OFF to minimize power consumption. With $\overline{E}$ LOW, both are enabled.

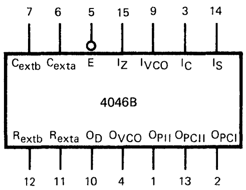
For direct-coupling between O_{VCO} and I_C, the voltage swing at the Voltage-Controlled Oscillator Output (O_{VCO}) must be within standard CMOS logic levels ($V_{OH} \geqslant 0.7 \times V_{DD}$ and $V_{OL} \leqslant 0.3 \times V_{DD}$); otherwise the signal from O_{VCO} must be capacitively coupled to the Signal Input (I_S).

Phase Comparator I is an Exclusive OR circuit ($I_C \oplus I_S$). I_C and I_S must have 50% duty cycles to maximize lock range. When the Output of Phase Comparator I (O_{PCI}) is connected back to the Voltage-Controlled Oscillator through the low pass filter network, an averaged voltage to I_{VCO} forces oscillation at a center frequency.

Phase Comparator II is an edge-triggered digital memory network with four flip-flop stages, associated control circuitry and a 3-state output. Phase Comparator II triggers on LOW-to-HIGH transitions at the Signal (I_S) and Comparator (I_C) Inputs and is independent of duty cycle at these inputs. The Output of Phase Comparator II (O_{PCII}) provides voltage levels and duty cycles corresponding to frequency and phase differentials between I_C and I_S. When O_{PCII} is connected to the Voltage-Controlled Oscillator Input (I_{VCO}) through the low pass filter network, a corresponding voltage across capacitor C_2 is adjusted until the Signal (I_S) and Comparator (I_C) Inputs are equal in both frequency and phase. At this point Phase Comparator II maintains a constant voltage across Capacitor C_2. When this stability has been established, the Phase Pulse Output (O_{PII}) is HIGH indicating a locked condition. Power dissipation in the low pass filter is reduced when Phase Comparator II is used.

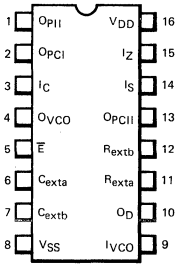
A zener diode is provided for regulating the power supply voltage, if necessary.

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



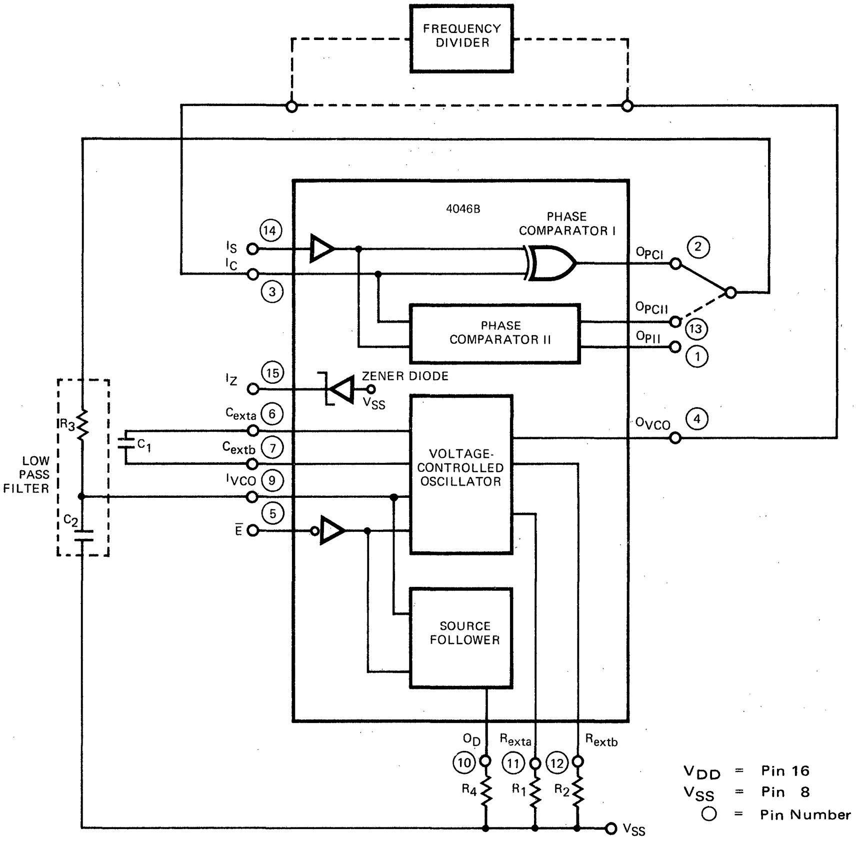
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

- **VERY LOW POWER CONSUMTPION**
- **HIGH VCO LINEARITY, 1% TYPICAL**
- **CHOICE OF 2-PHASE COMPARATORS**
- **ENABLE INPUT (ACTIVE LOW) FOR LOW POWER DISSIPATION IN STANDBY MODE**
- **ON-CHIP ZENER DIODE FOR SUPPLY REGULATION**
- **VCO FREQUENCY DRIFT WITH TEMPERATURE = 0.04% / °C TYPICAL AT V_{DD} = 10 V**

PIN NAMES

I_Z	Zener Diode Input
I_S	Signal Input
I_C	Comparator Input
I_{VCO}	Voltage-Controlled Oscillator Input
$\overline{E}$	Enable Input (Active LOW)
C_{exta}, C_{extb}	External Capacitor Connections
R_{exta}, R_{extb}	External Resistor Connections
O_{PCI}	Phase Comparator I Output
O_{PCII}	Phase Comparator II Output
O_{PII}	Phase Pulse Output
O_D	Demodulator Output
O_{VCO}	Voltage-Controlled Oscillator Output

BLOCK DIAGRAM



V_{DD} = Pin 16

V_{SS} = Pin 8

○ = Pin Number

$10\ k\Omega \leqslant R_1 \leqslant 1\ M\Omega$

$10\ k\Omega \leqslant R_2 \leqslant 1\ M\Omega$

$10\ k\Omega \leqslant R_4 \leqslant 1\ M\Omega$

$C_1 \geqslant 100$ pF at $V_{DD} = 5$ V

$C_1 \geqslant 50$ pF at $V_{DD} = 10$ V

FUNCTIONAL DESCRIPTION – The 4046B, Micropower Phase-Locked Loop consists of a low power linear Voltage-Controlled Oscillator (VCO), a Source Follower circuit (SF), two Phase Comparators (PCI and PCII) and a Zener diode.

VOLTAGE-CONTROLLED OSCILLATOR

The VCO requires one external capacitor (C_1) and one external resistor (R_1) to determine operational frequency range. External resistor R_2 is used to allow for frequency offset, if required. It is recommended that R_1 and R_2 have a value between 10 kΩ and 1 MΩ. At $V_{DD} = 5$ V, C_1 should be greater than or equal to 100 pF, and at $V_{DD} = 10$ V, C_1 should be greater than or equal to 50 pF.

External resistor R_3 and external capacitor C_2 combined serve as a low-pass filter to the Voltage-Controlled Oscillator Input (I_{VCO}). The user is allowed a wide range of resistor-to-capacitor ratios for R_3 and C_2 because of the high imput impedance at I_{VCO} (approximately 10^{12} Ω).

To avoid loading of the low-pass filter, the Demodulator Output (O_D) should be connected through external resistor R_4 as shown in the Block Diagram. It is recommended that R_4 have a value between 10 kΩ and 1 MΩ. If the O_D output is not utilized it must be left open.

The Voltage-Controlled Oscillator Output (O_{VCO}) provides a 0.3 V_{DD} to 0.7 V_{DD} output voltage swing and may be connected to the Comparator Input (I_C). O_{VCO} may, also be connected indirectly to I_C via CMOS frequency dividers (i.e., the 4018B, 4022B, 4029B, 4040B, 4518B, 4520B, 40160B, 40161B, 40162B, 40163B, 40192B, and 40193B.)

An Enable Input ($\overline{E}$) to the VCO and SF is provided for minimum stand-by power dissipation. With the $\overline{E}$ Input HIGH both the VCO and the SF are OFF. With $\overline{E}$ LOW, both are enabled.

PHASE COMPARATORS

For direct-coupling between O_{VCO} and I_C, the voltage swing at O_{VCO} must be within standard CMOS logic levels ($V_{OH} \geqslant 0.7\ V_{DD}$ and $V_{OL} \leqslant 0.3\ V_{DD}$); otherwise the signal from O_{VCO} must be capacitively coupled to the self-biasing amplifier at the I_S Input.

Phase Comparator I is an Exclusive OR circuit ($I_C \oplus I_S$). For maximum lock range, inputs to I_C and I_S must have 50% duty cycles. (Lock range, $2f_L$, is defined as that frequency range of input signals upon which the 4046B will stay locked from an initial locked condition). With no signal or noise input, Phase Comparator I provides an average output voltage equal to $V_{DD}/2$ at the O_{PCI} Output. This average output voltage is supplied to the I_{VCO} Input through the low-pass filter, which in turn forces the VCO to oscillate at a center frequency (f_O).

Capture range $2f_C$, is defined as that frequency range of input signals upon which the 4046B will lock from an initial unlocked condition. Capture range for PCI is directly dependent upon the characteristics of the low-pass filter network and may be as great as the lock range. Thus, PCI allows the user a phase-locked loop system which will remain in a locked condition despite high amounts of noise in the input signal.

It should be noted that with the use of PCI the system may lock onto input signals with frequencies that are near harmonics to the center frequency of the VCO. It should further be noted that the phase angle between the I_C and I_S Inputs will vary between 0° and 180°. At the center frequency the phase angle is 90°. *Figure 2* illustrates a typical Phase Angle versus Average Output Voltage response characteristic for PCI. *Figure 3* illustrates the typical waveforms for a phase-locked loop system employing PCI and locked at a center frequency.

Phase Comparator II is edge-triggered digital memory network with four flip-flop stages, associated control circuitry and a 3-state output, controlled internally. PCII triggers on LOW-to-HIGH transitions at the Signal (I_S) and Comparator (I_C) Inputs and is independent of duty cycle at these inputs. If the input frequency at I_S is higher than the input frequency at I_C, the p-channel output transistor at O_{PCII} is turned "ON" continuously, pulling the output (O_{PCII}) toward V_{DD}. If the input frequency at I_C is higher than the input frequency at I_S, the n-channel output transistor at O_{PCII} is turned "ON" continuously, pulling the output toward V_{SS}. If the input frequencies at I_S and I_C are equal, but I_S lags I_C in phase, the n-channel output transistor is turned "ON" for a period of time corresponding to the phase difference. If the input frequencies at I_S and I_C are equal, but I_C lags I_S in phase, the p-channel output transistor is turned "ON" for a period of time corresponding to the phase difference. Thus, over a period of time the voltage at capacitor C_2 is adjusted until the I_C and I_S input signals are of the same frequency and phase. Once this stability is reached, both p- and n-channel output transistors at O_{PCII} are "OFF". O_{PCII} becomes an open circuit holding the voltage across C_2 constant.

Once this stability is attained, the Phase Pulse Output (O_{PII}) is HIGH indicating a locked condition.

With PCII no phase difference is present between I_C and I_S over the entire VCO frequency range. Furthermore, since the 3-state Phase Comparator II Output (O_{PCII}) is mostly in the "OFF" condition, power dissipation through the low-pass filter is minimized. It should also be noted that $2f_C = 2f_L$ independent of the filter network in a phase-locked loop utilizing PCII. *Figure 4* shows typical waveforms for a phase-locked loop system employing Phase Comparator II and locked at a center frequency.

Fig. 2 CHARACTERISTICS OF PHASE COMPARATOR I AT THE LOW PASS FILTER OUTPUT.

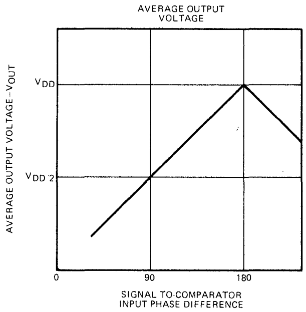


Fig. 3 A PLL SYSTEM USING PHASE COMPARATOR I.

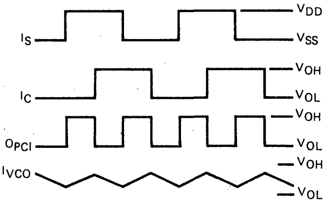


Fig. 4 A PLL SYSTEM USING PHASE COMPARATOR II

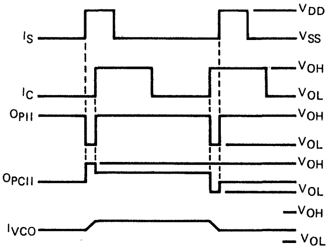


Fig. 5 TYPICAL LOW-PASS FILTERS.

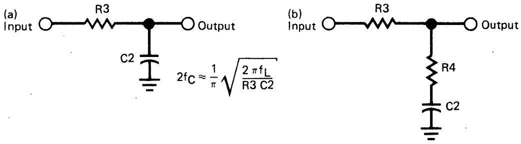
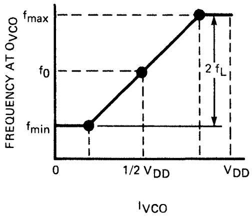


Fig. 6 DESIGN INFORMATION.

<table>
<tr><th>Characteristic</th><th>Using Phase Comparator 1</th><th>Using Phase Comparator 2</th></tr>
<tr><td>No signal on input I_S</td><td>VCO in PLL system adjusts to center frequency (f_0).</td><td>VCO in PLL system adjusts to minimum frequency (f_{min}).</td></tr>
<tr><td>Phase angle between I_S and I_C</td><td>90° at center frequency (f_0), approaching 0° and 180° at ends of lock range ($2f_L$).</td><td>Always 0° in lock (positive rising edges).</td></tr>
<tr><td>Locks on harmonics of center frequency.</td><td>Yes</td><td>No</td></tr>
<tr><td>Signal input noise rejection.</td><td>HIGH</td><td>LOW</td></tr>
<tr><td>Lock frequency range (2fL).</td><td colspan="2">The frequency range of the input signal on which the loop will stay locked if it was initially in lock. $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$.</td></tr>
<tr><td rowspan="2">Capture frequency range ($2f_C$).</td><td colspan="2">The frequency range of the input signal on which the loop will lock if it was initially out of lock.</td></tr>
<tr><td>Depends on low-pass filter characteristics (Figure 5) $f_C \leqslant f_L$</td><td>$f_C = f_L$</td></tr>
<tr><td>Center frequency (f_0).</td><td colspan="2">The frequency of O_{VCO} when $I_{VCO} = 1/2\ V_{DD}$</td></tr>
<tr><td>O_{VCO} freqency (f).
NOTE: The information presented here is meant only as a design guide.</td><td colspan="2">$$f \approx \frac{K\left[\frac{I_{VCO}-1.65}{R_1}+\frac{V_{DD}-1.35}{R_2}\right]}{(C_1+32)\,(V_{DD}+1.6)}\ \text{MHz (at 25°C)}$$
where:
V_{DD} in V; $5\ V \leqslant V_{DD} \leqslant 15\ V$
I_{VCO} in V; $1.65\ V \leqslant I_{VCO} \leqslant (V_{DD} - 1.35\ V)$
R_1 and R_2 in MΩ; $R_1, R_2 \geqslant 0.005$ MΩ
C_1 in pF; $C_1 \geqslant 50$ pF
$K = 0.95$ @ $V_{DD} = 5$ V
$= 0.95$ @ $V_{DD} = 10$ V
$= 1.08$ @ $V_{DD} = 15$ V

 </td></tr>
</table>

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

ELECTRICAL CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER		LIMITS									UNITS	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{TLH} t_{THL}	Propagation Delay, Output Transition Time			72 72			48 48			38 38		ns	C_L = 50 pF R_L = 200 kΩ Input Transition Times ≤ 20 ns
PHASE COMPARATORS													
R_{IN}	Input Resistance	I_S		200			400			700		MΩ	
		I_C		10^6			10^6			10^6			
V_{IN}	AC Coupled Input Sensitivity for I_S			200			400			700		mV p-p	
	DC Coupled Input Sensitivity for I_S, I_C		See Note 1 for V_{IH} and V_{IL} Characteristics										
VOLTAGE CONTROLLED OSCILLATER													
	Temperature-Frequency Stability			0.12 0.24			0.04 0.08			0.015 0.03		%/°C	No Frequency Offset, f_{min} = 0 See Note 3
				0.06 0.12			0.05 0.10			0.03 0.06			Frequency Offset, $f_{min} \neq 0$ See Note 4
	Linearity			1			1			1		%	See Note 2
	Output Duty Cycle			50			50			50		%	O_{VCO} tied to I_C
R_{IN}	Input Resistance to I_{VCO}			10^6			10^6			10^6		MΩ	
f_{max}	Maximum Operating Frequency			0.9			1.7			2.3		MHz	See Note 6
SOURCE FOLLOWER													
V_D	Offset Voltage at O_D			1.65			1.65			1.65		V	$R_4 > 10$ kΩ
	Linearity			0.1			0.6			0.8		%	See Note 5
ZENER DIODE													
V_Z	Zener Voltage			7			7			7		V	I_Z = 50 μA
R_Z	Zener Dynamic Resistance			100			100			100		Ω	I_Z = 1 mA

Notes:

1. Additional dc characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. I_{VCO} = 2.5 V ± 0.3 V, $R_1 > 10$ kΩ for V_{DD} = 5 V. I_{VCO} = 5 V ± 2.5 V, $R_1 > 400$ kΩ for V_{DD} = 10 V. I_{VCO} = 7.5 V ± 5 V, $R_1 > 1$ MΩ for V_{DD} = 15 V.
3. $R_2 = \infty$, $\%/°C \propto 1/(f-V_{DD})$.
4. $\%/°C \propto 1/(f-V_{DD})$.
5. $R_4 > 50$ kΩ, I_{VCO} = 2.5 V ± 0.3 V for V_{DD} = 5 V. I_{VCO} = 5 V ± 2.5 V for V_{DD} = 10 V, I_{VCO} = 7.5 V ± 5 V for V_{DD} = 15 V.
6. R_1 = 5 kΩ, $R_2 = \infty$, $I_{VCO} = V_{DD}$, C_1 = 50 pF.

4047B

MONOSTABLE/ASTABLE MULTIVIBRATOR

DESCRIPTION – The 4047B is a Monostable/Astable Multivibrator capable of operating in either the monostable or astable mode. Operation in either mode requires an external capacitor (C_x) between pins 1 and 3 (C_{ext},R_{ext}/C_{ext}) and an external resistor (R_x) between pins 2 and 3 (R_{ext},R_{ext}/C_{ext}). These external timing components (R_x,C_x) determine the output pulse width in the monostable mode and the output frequency in the astable mode. The 4047B also has active HIGH and active LOW astable mode Enable Inputs (E_{A0},$\overline{E}_{A1}$), active HIGH and active LOW Trigger Inputs (T_0,$\overline{T}_1$) for operation in the monostable mode, a Retrigger Input (I_{RT}), an Oscillator Output (O), active HIGH and active LOW flip-flop Outputs (Q,$\overline{Q}$) and an overriding asynchronous Master Reset Input (MR).

ASTABLE OPERATION. Astable operation is obtained by either a HIGH on the E_{A0} input or a LOW on the $\overline{E}_{A1}$ input. The frequency of the 50% duty cycle output at the Q and $\overline{Q}$ outputs is determined by the external timing components (R_x,C_x). A frequency twice that of the Q and $\overline{Q}$ outputs is available at the Oscillator Output (O). However, a 50% duty cycle is not guaranteed. The 4047B can be used as a gated oscillator by controlling the E_{A0} and $\overline{E}_{A1}$ inputs.

MONOSTABLE OPERATION. Monostable operation is obtained by connecting the E_{A0} input LOW and the $\overline{E}_{A1}$ input HIGH. The device can be triggered by either a LOW-to-HIGH transition at the T_0 input while the $\overline{T}_1$ input is LOW or a HIGH-to-LOW transition at the $\overline{T}_1$ input while the T_0 is HIGH. The output pulse width at Q and $\overline{Q}$ is determined by the external timing components (R_x,C_x). The device can be retriggered by applying a simultaneous LOW-to-HIGH transition to both the Retrigger Input (I_{RT}) and the T_0 input while the $\overline{T}_1$ input is LOW.

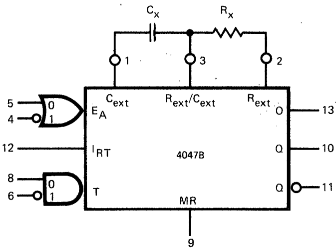
A HIGH on the Master Reset Input (MR) resets the output flip-flop (Q = LOW, $\overline{Q}$ = HIGH independent of all other input conditions.

- **MONOSTABLE OR ASTABLE OPERATION**
- **TRUE AND COMPLEMENTARY BUFFERED OUTPUTS**
- **ENABLED WITH EITHER A LOW OR A HIGH LEVEL IN THE ASTABLE MODE**
- **TRIGGERED ON EITHER A LOW-TO-HIGH OR A HIGH-TO-LOW TRANSITION IN THE MONOSTABLE MODE**
- **ASYNCHRONOUS MASTER RESET**
- **IN THE MONOSTABLE MODE, OUTPUT PULSE WIDTH IS INDEPENDENT OF THE TRIGGER PULSE**
- **RETRIGGERABLE OPTION AVAILABLE FOR PULSE WIDTH EXPANSION**
- **IN THE ASTABLE MODE, MAY BE UTILIZED AS EITHER A FREE RUNNING OR GATED OSCILLATOR WITH A 50% OUTPUT DUTY CYCLE**

PIN NAMES

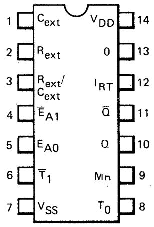
C_{ext}	External Capacitor Connection
R_{ext}	External Resistor Connection
R_{ext}/C_{ext}	Common External Capacitor and Resistor Connection
I_{RT}	Retrigger Input
T_0	Trigger Input (L → H Triggered)
$\overline{T}_1$	Trigger Input (H → L Triggered)
E_{A0}	Enable Input (Active HIGH)
$\overline{E}_{A1}$	Enable Input (Active LOW)
MR	Master Reset
O	Oscillator Output
Q,$\overline{Q}$	True and Complementary Buffered Outputs

LOGIC SYMBOL



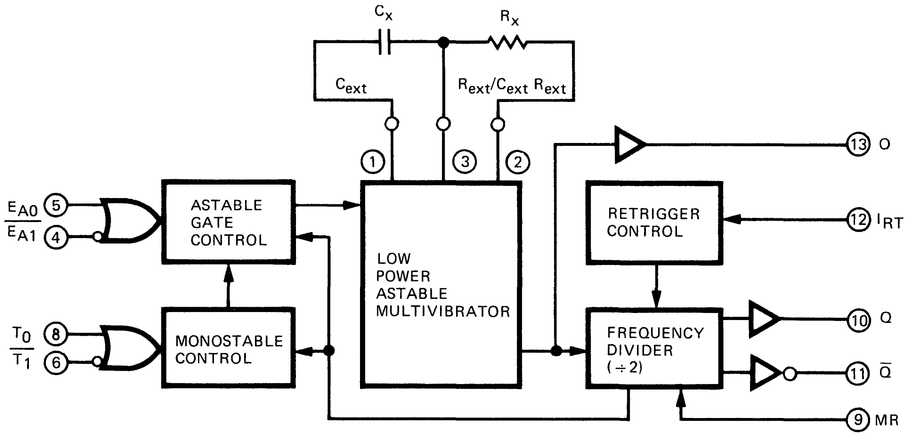
V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



V_{DD} = PIN 14
V_{SS} = PIN 7
○ = PIN NUMBER

MODE SELECTION

INPUTS						FUNCTION
E_{A0}	$\overline{E_{A1}}$	T_0	$\overline{T_1}$	I_{RT}	MR	
H	X	L	H	L	L	Astable Multivibrator (Free Running)
X	L	L	H	L	L	Astable Multivibrator (Free Running)
⎍	H	L	H	L	L	Astable Multivibrator (True Gating)
L	⊔	L	H	L	L	Astable Multivibrator (Complement Gating)
L	H	↑	L	L	L	Monostable Multivibrator (Positive-Edge Triggering)
L	H	H	↓	L	L	Monostable Multivibrator (Negative-Edge Triggering)
L	H	↑	L	↑	L	Monostable Multivibrator (Retriggering)
X	X	X	X	X	H	Reset

H = HIGH LEVEL
L = LOW LEVEL
⎍ = POSITIVE PULSE
⊔ = NEGATIVE PULSE
↑ = POSITIVE-GOING TRANSITION
↓ = NEGATIVE-GOING TRANSITION
X = DON'T CARE

OPERATION RULES

1. Under normal operating conditions of the 4047B, signals at the Common External Capacitor and Resistor Connection (R_{ext}/C_{ext}) may go above V_{DD} or below V_{SS}. A different input protection circuit has been utilized that is not as effective as the standard input protection circuit on all other inputs. Additional care in handling is advised.

2. An external resistor (R_X) and an external timing capacitor (C_X) are required as shown in the Block Diagram. To simply maintain oscillation there are no limits on R_X or C_X. However, in the interests of accuracy and predictability it is recommended that C_X be much greater than stray capacitance in the system and R_X be much greater than the series "ON" resistance of the 4047B. In addition, as R_X becomes very large, short-term instabilities may be introduced. Recommended component values are listed below:

$C_X \geqslant 100$ pF	for astable operation
$C_X \geqslant 1000$ pF	for monostable operation
$10\ k\Omega \leqslant R_X \leqslant 1\ M\Omega$	

3. In the astable mode of operation, the output period at the Q output (T_Q) is determined as follows:

   $T_Q = 4.40 \cdot R_X \cdot C_X$, typically where:
   C_X is in farads
   R_X is in ohms
   T_Q is in seconds

   Actual output period (T_Q) will vary with fluctuations in temperature, power supply voltage, and individual device-to-device threshold voltages.

4. In the monostable mode of operation the output pulse width at the Q output (tw_Q) is determined as follows:

   $tw_Q = 2.48 \cdot R_X \cdot C_X$, typically where:
   C_X is in farads
   R_X is in ohms
   tw_Q is in seconds

   Actual output pulse width (tw_Q) will vary with fluctuations in temperature, power supply voltage, and individual device-to-device threshold voltages.

5. It should be noted that in the astable mode of operation, the first positive half cycle will have a duration equal to $tw_Q = 2.48 \cdot R_X \cdot C_X$. Succeeding positive half cycles will have a duration of $T_Q = 4.40 \cdot R_X \cdot C_X$,.

6. Under all operating conditions, C_X and R_X must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

7. V_{DD} and ground wiring should conform to good high frequency standards so that switching transients on V_{DD} and ground leads do not cause interaction between devices. Use of a 0.01 to 0.1 μF bypass capacitor between V_{DD} and ground located near the 4047B is recommended.

8. In the retriggering mode of operation extended output pulse width at the Q or $\overline{Q}$ outputs may be obtained by applying more than one input pulse to the T_0 and I_{RT} inputs simultaneously.

9. An overriding active HIGH, Master Reset Input (MR) is provided on the 4047B device. By applying a HIGH to the Master Reset Input, any timing cycle can be terminated or any new cycle inhibited until the HIGH Master Reset signal is removed. Trigger inputs will not produce spikes in the output when Master Reset is HIGH.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent	XC			20			40			80	μA	MIN, 25°C	All inputs
	Power				150			300			600		MAX	at 0 V or V_{DD}
	Supply	XM			5			10			20	μA	MIN, 25°C	
	Current				150			300			600		MAX	

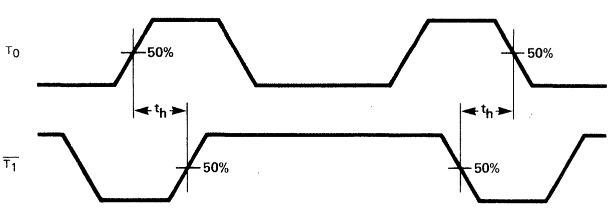
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, E_{A0} OR		100			50	125		38	100	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤20 ns
t_{PHL}	$\overline{E_{A1}}$ to 0		100			50	125		38	100	ns	
t_{PLH}	Propagation Delay, E_{A0} OR		160			74	185		56	148	ns	
t_{PHL}	$\overline{E_{A1}}$ to Q or $\overline{Q}$		160			74	185		56	148	ns	
t_{PLH}	Propagation Delay, T_0 OR		210			94	235		68	108	ns	
t_{PHL}	$\overline{T_1}$ to Q or $\overline{Q}$		210			94	235		68	108	ns	
t_{PLH}	Propagation Delay, T_0, I_{RT}		116			60	130		46	104	ns	
t_{PHL}	to Q or $\overline{Q}$		116			60	130		46	104	ns	
t_{PLH}	Propagation Delay, MR to		100			44	125		28	100	ns	
t_{PHL}	Q or $\overline{Q}$		100			44	125		28	100	ns	
t_{TLH}	Output Transition		65	135		31	75		24	45	ns	
t_{THL}	Time		60	135		25	75		20	45	ns	
t_w	Minimum Pulse Width (Any Input)	400	160		170	68		136	44		ns	
t_{rec}	MR Recovery Time	0	-30		0	-15		0	-10		ns	
t_h	Hold Time, T_0 to $\overline{T_1}$	64	32		32	16		26	13		ns	
t_h	Hold Time, $\overline{T_1}$ to T_0	64	32		32	16		26	13		ns	

Notes:

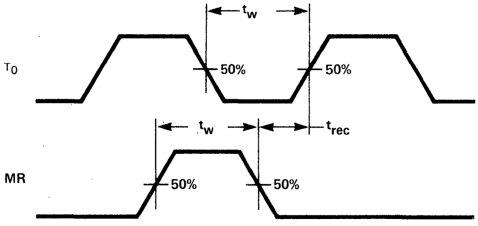
1. Additional dc characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. It is recommended that input rise and fall times to the T_0, T_1, or I_{RT} Inputs be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V and 3 μs at V_{DD} = 15 V. Also input rise and fall times to E_{A0} and E_{A1} should be less than 500 ns at any V_{DD} voltage.

SWITCHING WAVEFORMS



HOLD-TIMES, T_0 TO $\overline{T_1}$ AND $\overline{T_1}$ TO T_0

Hold Times are shown as positive values, but may be specified as negative values.



MINIMUM PULSE WIDTHS AND RECOVERY TIME FOR MR

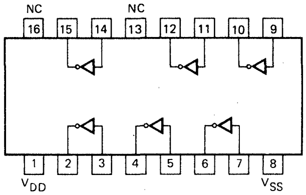
CONDITIONS: $\overline{T_1}$ = LOW while T_0 is triggered on a LOW-to-HIGH transition. t_w and t_{rec} also apply when T_0 = HIGH and $\overline{T_1}$ is triggered on a HIGH-to-LOW transition.

4049B • 4050B

4049B HEX INVERTING BUFFER • 4050B HEX NON-INVERTING BUFFER

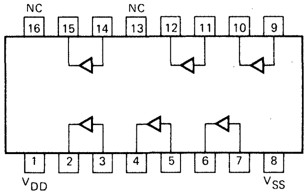
DESCRIPTION – These CMOS buffers provide high current output capability suitable for driving TTL or high capacitance loads. Since input voltages in excess of the buffers' supply voltage are permitted, these buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. The 4049B provides six inverting buffers, the 4050B six non-inverting buffers. Their guaranteed fan out into common bipolar logic elements is shown in Table 1.

4049B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)

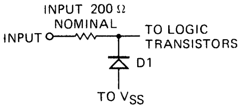


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

4050B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



INPUT PROTECTION



NOTE: Typical Breakdown Voltage of Diode D1 is 20 V.

TABLE 1
Guaranteed fan out of 4049B, 4050B into common logic families

DRIVEN ELEMENT	GUARANTEED FAN OUT
Standard TTL, DTL	2
9LS, 93L, 74LS	9
74L	16

Conditions: $V_{DD} = V_{CC} = 5.0 \pm 0.25$ V
$V_{OL} \leq 0.5$ V, T_A = 0 to 75 °C

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, 4049BXM and 4050BXM (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OH}	Output HIGH Current	-1.85									mA	MIN	V_{OUT} = 2.5 V for V_{DD} = 5 V Inputs at 0 or V_{DD} per Function
		-1.25	-2.5									25°C	
		-0.9										MAX	
		-0.62			-1.85			-5.5			mA	MIN	V_{OUT} = 4.5 V for V_{DD} = 5 V V_{OUT} = 9.5 V for V_{DD} = 10 V V_{OUT} = 13.5 V for V_{DD} = 15 V Inputs at 0 or V_{DD} per Function
		-0.5	-1		-1.25	-2.5		-3.75	-7.5			25°C	
		-0.35			-0.9			-2.7				MAX	
I_{OL}	Output LOW Current	3.75			10			30			mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 5 V V_{OUT} = 0.5 V for V_{DD} = 10 V V_{OUT} = 1.5 V for V_{DD} = 15 V Inputs at 0 or V_{DD} per Function
		3	6		8	16		24	48			25°C	
		2.1			5.6			16.8				MAX	
		3.3									mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 4.5 V Inputs at 0 V or V_{DD} per Function
		2.6	5.2									25°C	
		1.8										MAX	
I_{DD}	Quiescent Power Supply Current			1			2			4	μA	MIN, 25°C	All Inputs at 0 V or V_{DD}
				30			60			120		MAX	

Notes on the following page.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, 4049BXC and 4050BXC (Cont'd) (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OH}	Output HIGH Current	-1.5									mA	MIN	V_{OUT} = 2.5 V for V_{DD} = 5 V
		-1.25	-2.5								mA	25°C	Inputs at 0 or V_{DD}
		-1.0									mA	MAX	per Function
													V_{OUT} = 4.5 V for V_{DD} = 5 V
		-0.6			-1.5			-4.5			mA	MIN	V_{OUT} = 9.5 V for V_{DD} = 10 V
		-0.5	-1		-1.25	-2.5		-3.75	-7.5		mA	25°C	V_{OUT} = 13.5 V for V_{DD} = 15 V
		-0.4			-1.0			-3			mA	MAX	Inputs at 0 or V_{DD}
													per Function
I_{OL}	Output LOW Current												V_{OUT} = 0.4 V for V_{DD} = 5 V
		3.6			9.6			28			mA	MIN	V_{OUT} = 0.5 V for V_{DD} = 10 V
		3.0	6		8	16		24	48		mA	25°C	V_{OUT} = 1.5 V for V_{DD} = 15 V
		2.5			6.6			19			mA	MAX	Inputs at 0 or V_{DD}
													per Function
		3.1									mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 4.5 V
		2.6	5.2								mA	25°C	Inputs at 0 V or V_{DD}
		2.1									mA	MAX	per Function
I_{DD}	Quiescent Power Supply Current			4			8			16	µA	MIN,25°C	All inputs at 0 V or V_{DD}
				30			60			120		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4049B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		65	130		30	65		29	52	ns	C_L = 50 pF,
t_{PHL}			50	105		25	50		17	40		R_L = 200 kΩ
t_{TLH}	Output Transition Time		73	145		40	80		30	60	ns	Input Transition
t_{THL}			33	65		13	25		9	20		Times ≤ 20 ns

NOTES:

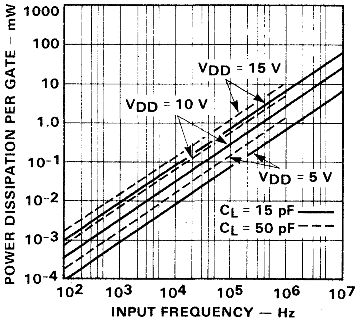
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4050B only (See Note 2)

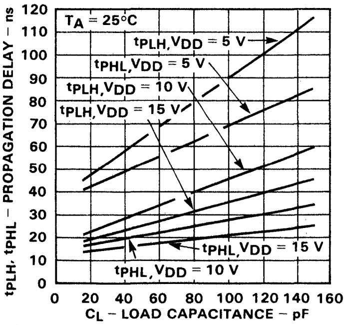
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay		65 43	130 95		30 23	65 45		24 17	52 36	ns	C_L = 50 pF, R_L = 200 kΩ
t_{TLH} t_{THL}	Output Transition Time		73 33	145 65		90 13	80 25		30 9	60 20	ns	Input Transition Times ≤ 20 ns

Notes on preceeding page.

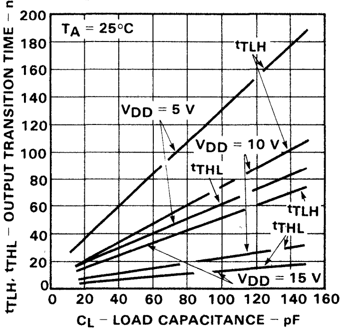
TYPICAL ELECTRICAL CHARACTERISTICS



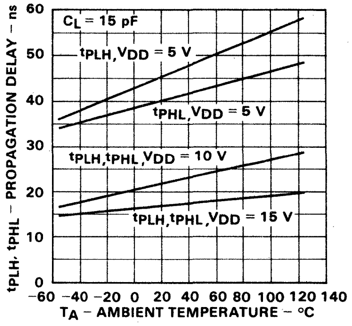
TYPICAL POWER DISSIPATION VERSUS FREQUENCY



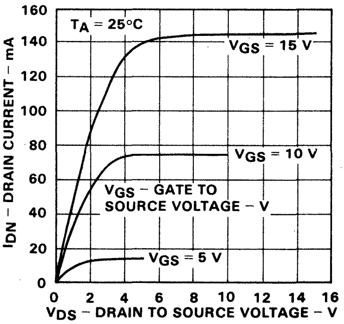
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



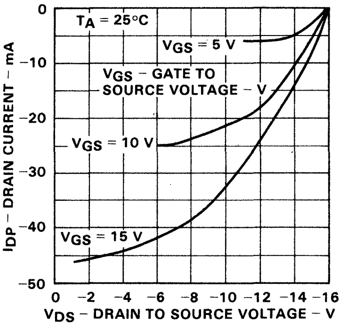
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



PROPAGATION DELAY VERSUS TEMPERATURE



N-CHANNEL DRAIN CHARACTERISTICS



P-CHANNEL DRAIN CHARACTERISTICS

4051B

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION — The 4051B is an 8-Channel Analog Multiplexer/Demultiplexer with three Address Inputs (A_0–A_2), an active LOW Enable Input ($\overline{E}$), eight Independent Inputs/Outputs (Y_0–Y_7) and a Common Input/Output (Z).

The 4051B contains eight bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0–Y_7) and the other side connected to a Common Input/Output (Z). With the Enable Input ($\overline{E}$) LOW, one of the eight switches is selected (low impedance, ON state) by the three Address Inputs (A_0–A_2). With the Enable Input ($\overline{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Address Inputs.

V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0–A_2, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs (Y_0–Y_7, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}–V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

PIN NAMES

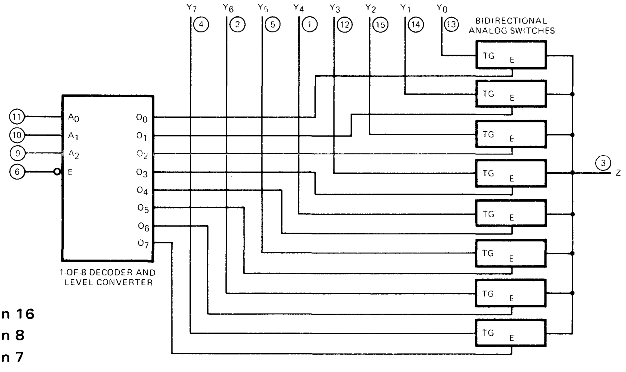
Y_0–Y_7	Independent Inputs/Outputs
A_0–A_2	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
Z	Common Input/Output

TRUTH TABLE

INPUTS				CHANNELS							
$\overline{E}$	A_2	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z	Y_4–Z	Y_5–Z	Y_6–Z	Y_7–Z
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
H	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

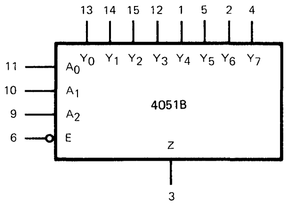
L = LOW Level
H = HIGH Level
X = Don't Care

4051B FUNCTIONAL LOGIC DIAGRAM



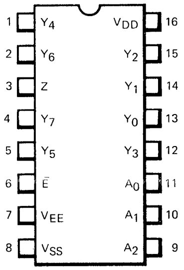
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7
○ = Pin Numbers

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		95	900		55	380		35	210	Ω	MIN	$V_{is} = V_{DD}$ to V_{EE} Note 2
				100	1000		65	500		40	280		25°C	
				125	1100		100	600		65	340		MAX	
		XM		90	850		50	340		30	190	Ω	MIN	
				100	1000		65	500		40	280		25°C	
				150	1150		110	660		70	370		MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels			25			10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	$\overline{E} = V_{DD}$ $V_{SS} = V_{DD}/2$ $V_{is} = V_{DD}$ or V_{EE} $V_{os} = V_{EE}$ or V_{DD}
		XM						80						
	Any Channel OFF	XC						100						$\overline{E} = V_{SS} = V_{DD}/2$ $V_{is} = V_{DD}$ or V_{EE} $V_{os} = V_{EE}$ or V_{DD}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40			80	μA	MIN, 25°C	$V_{SS} = V_{EE}$ All inputs at V_{DD} or V_{EE}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		25 10			10 6			6 4		ns	C_L = 50 pF, R_L = 200 kΩ $\overline{E} = V_{SS} = V_{EE}$, A_n or $V_{is} = V_{DD}$ or V_{EE} Note 5
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		170 210			95 125			80 95		ns	
t_{PZL} t_{PZH}	Output Enable Time		185 205			95 105			75 85		ns	C_L = 50 pF, R_L = 1 kΩ E or $A_n = V_{SS} = V_{EE}$ $V_{is} = V_{DD}$ or V_{EE} Note 5
t_{PLZ} t_{PHZ}	Output Disable Time		1250 1240			1130 1120			1080 1070		ns	
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	R_L = 10 kΩ $V_{SS} = V_{DD}/2$, $\overline{E} = V_{EE}$, $V_{is} = V_{DD}/2$ (sine wave) p-p f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ $\overline{E} = V_{EE}$ $V_{is} = V_{DD}/2$ (sine wave) p-p at -40 dB $V_{SS} = V_{DD}/2$, 20 Log_{10} (V_{os}/V_{is}) = -40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ, $V_{SS} = V_{DD}/2$ $\overline{E} = V_{DD}$ $V_{is} = V_{DD}/2$ (sine wave) p-p 20 Log_{10} (V_{os}/V_{is}) = -40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ, $\overline{E} = V_{SS}$ $V_{is} = V_{DD}/2$ (sine wave) p-p $V_{SS} = V_{DD}/2$ 20 Log_{10} (V_{os}/V_{os} @ 1 kHz) = -3 dB

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. $\overline{E} = V_{SS}$ R_L = 10 kΩ, any channel selected and $V_{SS} = V_{EE}$ or $V_{DD/2}$.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
5. $V_{IN} = V_{DD}$ (Square Wave), Input transition times ≤ 20 ns, R_L = 10 kΩ.
6. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 2, 4, 5, 12, 13, 14, or 15 the voltage drop across the bidirectional switch must not exceed 0.5 V at $T_A \leq 25°$C, or 0.3 V at $T_A > 25°$C. No V_{DD} current will flow through R_L if the switch current flows into terminal 3.

4052B

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The 4052B is a Dual 4-Channel Analog Multiplexer/Demultiplexer with common channel select logic. Each Multiplexer/Demultiplexer has four independent Inputs/Outputs (Y_0–Y_3) and a Common Input/Output (Z). The common channel select logic includes two Address Inputs (A_0, A_1) and an active LOW Enable Input ($\overline{E}$).

Both multiplexer/demultiplexers contain four bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0–Y_3) and the other side connected to a Common Input/Output (Z). With the Enable Input LOW, one of the four switches is selected (low impedance, ON state) by the two Address Inputs. With the Enable Input HIGH, all switches are in the high impedance OFF state, independent of the Address Inputs.

V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0, A_1, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs (Y_0–Y_3, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}–V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **DIGITAL OR ANALOG MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

PIN NAMES

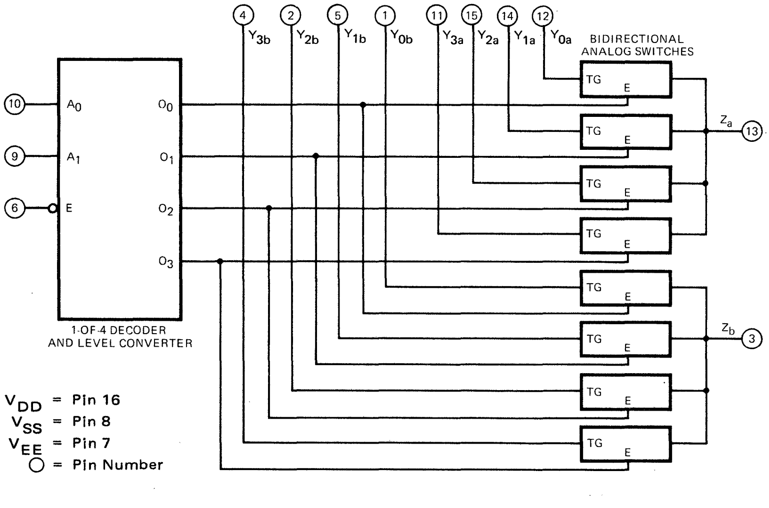
Y_{0a}–Y_{3a}	Independent Inputs/Outputs
Y_{0b}–Y_{3b}	Independent Inputs/Outputs
A_0, A_1	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
Z_a, Z_b	Common Input/Output

TRUTH TABLE

INPUTS			CHANNELS			
$\overline{E}$	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z
L	L	L	ON	OFF	OFF	OFF
L	L	H	OFF	ON	OFF	OFF
L	H	L	OFF	OFF	ON	OFF
L	H	H	OFF	OFF	OFF	ON
H	X	X	OFF	OFF	OFF	OFF

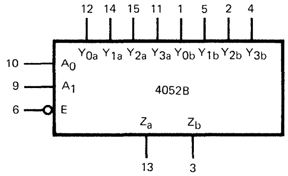
L = LOW Level, H = HIGH Level, X = Don't care

4052B FUNCTIONAL LOGIC DIAGRAM



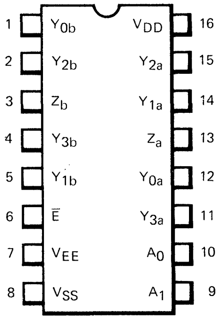
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7
○ = Pin Number

LOGIC SYMBOL



V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		95	900		55	380		35	210	Ω	MIN	V_{is} = V_{DD} to V_{EE} Note 2
				100	1000		65	500		40	280		25°C	
				125	1100		100	600		65	340		MAX	
		XM		90	850		50	340		30	190	Ω	MIN	
				100	1000		65	500		40	280		25°C	
				150	1150		110	660		70	370		MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels			25			10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	$\overline{E}$ = V_{DD}, V_{SS} = $V_{DD}/2$ V_{is} = V_{DD} or V_{EE} V_{os} = V_{EE} or V_{DD}
		XM						80						
	Any Channel OFF	XC						100						$\overline{E}$ = V_{SS} = $V_{DD}/2$ V_{is} = V_{DD} or V_{EE} V_{os} = V_{EE} or V_{DD}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40			80	µA	MIN, 25°C	V_{SS} = V_{EE} All inputs at V_{DD} or V_{EE}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		25			10			6		ns	C_L = 50 pF, R_L = 200 kΩ
t_{PHL}	Input to Output		10			6			4			$\overline{E}$ = V_{SS} = V_{EE},
t_{PLH}	Propagation Delay,		170			95			80		ns	A_n or V_{is} = V_{DD} or V_{EE}
t_{PHL}	Address to Output		210			125			95			Note 5
t_{PZL}	Output Enable Time		185			95			75		ns	C_L = 50 pF, R_L = 1 kΩ
t_{PZH}			205			105			85			$\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ}	Output Disable Time		1250			1130			1080		ns	V_{is} = V_{DD} or V_{EE}
t_{PHZ}			1240			1120			1070			Note 5
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	R_L = 10 kΩ V_{SS} = V_{DD}/2, $\overline{E}$ = V_{EE}, V_{is} = V_{DD}/2 (sine wave) p-p f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ, $\overline{E}$ = V_{EE} V_{is} = V_{DD}/2 (sine wave) p-p at −40 dB V_{SS} = V_{DD}/2, 20 Log_{10} (V_{os}/V_{is}) = −40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ, V_{SS} = V_{DD}/2 $\overline{E}$ = V_{DD} V_{is} = V_{DD}/2 (sine wave) p-p 20 Log_{10} (V_{os}/V_{is}) = −40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ, $\overline{E}$ = V_{SS} V_{is} = V_{DD}/2 (sine wave) p-p V_{SS} = V_{DD}/2 20 Log_{10} (V_{os}/V_{os} @ 1 kHz = −3 dB

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. $\overline{E}$ = V_{SS}, R_L = 10 kΩ, any channel selected and V_{SS} = V_{EE} or V_{DD}/2.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
5. V_{IN} = V_{DD} (Square Wave), Input transition times ≤ 20 ns
6. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 2, 4, 5, 11, 12, 14, or 15 the voltage drop across the bidirectional switch must not exceed 0.5 V at $T_A \leqslant 25°C$, or 0.3 V at $T_A > 25°C$. No V_{DD} current will flow through R_L if the switch current flows into terminals 3 or 13.

4053B
TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The 4053B is a Triple 2-Channel Analog Multiplexer/Demultiplexer with a common Enable Input ($\overline{E}$). Each Multiplexer/Demultiplexer has two Independent Inputs/Outputs (Y_0,Y_1), a Common Input/Output (Z), and a Select Input (S). Each multiplexer/demultiplexer contains two bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0,Y_1) and the other side connected to a Common Input/Output (Z). With the Enable Input ($\overline{E}$) LOW, one of the two switches is selected (low impedance, ON state) by the Select Input (S). With the Enable Input ($\overline{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Select Inputs (S_a-S_c).

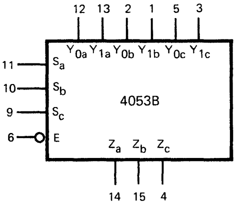
V_{DD} and V_{SS} are the two supply voltage connections for the Digital Control Inputs (S_a-S_c,$\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog Inputs/Outputs (Y_0,Y_1,Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}-V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

PIN NAMES

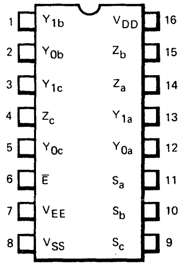
Y_{0a}-Y_{0c}, Y_{1a}-Y_{1c}	Independent Input/Outputs
S_a-S_c	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
Z_a-Z_c	Common Input/Outputs

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



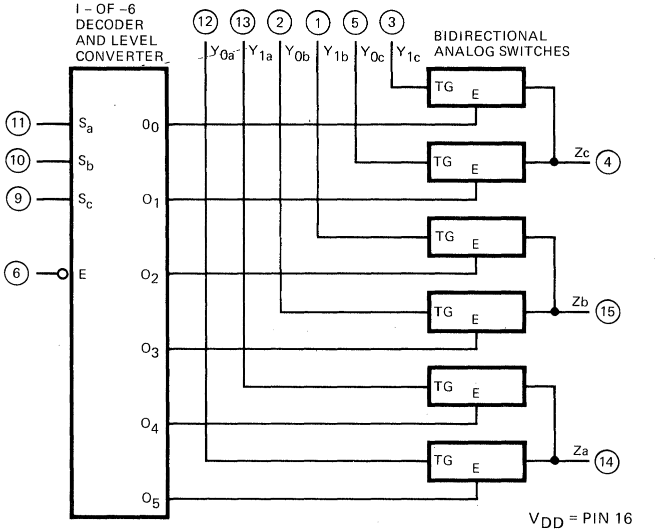
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

INPUTS		CHANNELS	
$\overline{E}$	S	Y_0-Z	Y_1-Z
L	L	ON	OFF
L	H	OFF	ON
H	X	OFF	OFF

H = HIGH Level
L = LOW Level
X = Don't Care

FUNCTIONAL LOGIC DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7
○ =PIN NUMBER

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		95	900		55	380		35	210		MIN	V_{is} = V_{DD} to V_{EE} Note 2
				100	1000		65	500		40	280	Ω	25°C	
				125	1100		100	600		65	340		MAX	
		XM		90	850		50	340		30	190		MIN	
				100	1000		65	500		40	280	Ω	25°C	
				150	1150		110	660		70	370		MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels			25			10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	$\overline{E}$ = V_{DD}, V_{SS} = $V_{DD}/2$ V_{is} = V_{DD} or V_{EE} V_{os} = V_{EE} or V_{DD}
		XM						80						
	Any Channel OFF	XC						100						$\overline{E}$ = V_{SS} = $V_{DD}/2$ V_{is} = V_{DD} or V_{EE} V_{os} = V_{EE} or V_{DD}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40			80	µA	MIN, 25°C	V_{SS} = V_{EE} All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20		MIN, 25°C	
					150			300			600		MAX	

Notes are on the following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		25 10			10 6			6 4		ns	C_L = 50 pF R_L =200 kΩ $\overline{E}$ = V_{SS} = V_{EE}, S_n or V_{is} = V_{DD} or V_{EE} Note 5
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		170 210			95 125			80 95		ns	
t_{PZL} t_{PZH}	Output Enable Time		185 205			95 105			75 85		ns	C_L = 50 pF , R_L = 1 kΩ $\overline{E}$ or S_n = V_{SS} = V_{EE} V_{is} = V_{DD} or V_{EE} Note 5
t_{PLZ} t_{PHZ}	Output Disable Time		1250 1240			1130 1120			1080 1070		ns	
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	R_L = 10 kΩ V_{SS} = $V_{DD}/2$, $\overline{E}$ = V_{EE}, V_{is} = $V_{DD}/2$ (sine wave)p-p f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ $\overline{E}$ = V_{EE} V_{is} = $V_{DD}/2$ (sine wave) p-p at -40 dB V_{SS} = $V_{DD}/2$, 20 Log_{10} (V_{os}/V_{is}) = -40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ, V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{DD} V_{is} = $V_{DD}/2$ (sine wave)p-p 20 Log_{10} (V_{os}/V_{is}) = -40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ, $\overline{E}$ = V_{SS} V_{is} = $V_{DD}/2$ (sine wave)p-p V_{SS} = $V_{DD}/2$ 20 Log_{10} (V_{os}/V_{os} @ 1 kHz) = -3 dB

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. $\overline{E}$ = V_{SS}, R_L = 10 kΩ, any channel selected and V_{SS} = V_{EE} or $V_{DD}/2$.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
5. V_{IN} = V_{DD} (Square Wave), Input transition times ≤ 20 ns,
6. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 2, 3, 5, 12, or 13 the voltage drop across the bidirectional switch must not exceed 0.5 V at $T_A \leq 25°C$, or 0.3 V at $T_A > 25°C$. No V_{DD} current will flow through R_L if the switch current flows into terminals 4, 14, or 15.

4066B

QUAD BILATERAL SWITCHES

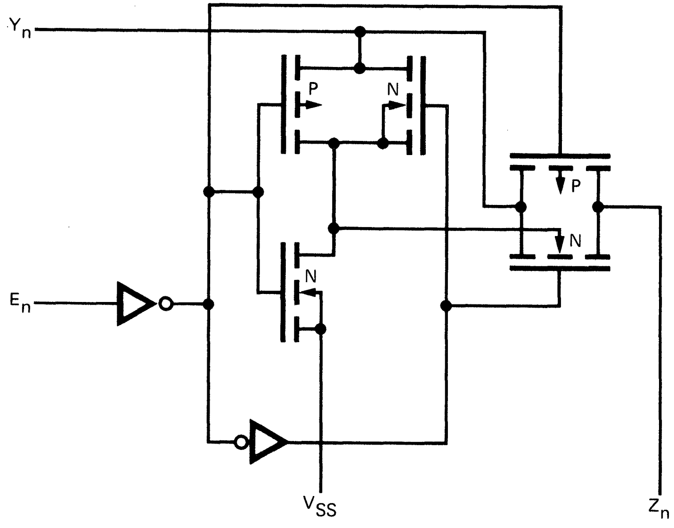
DESCRIPTION – The 4066B has four independent bilateral analog switches (transmission gates). Each switch has two Input/Output Terminals (Y_n, Z_n) and an active HIGH Enable Input (E_n). A HIGH on the Enable Input establishes a low impedance bidirectional path between Y_n and Z_n (ON condition). A LOW on the Enable Input disables the switch; high impedance between Y_n and Z_n (OFF condition).

- **DIGITAL OR ANALOG SIGNAL SWITCHING**
- **INDIVIDUAL ENABLE INPUTS (ACTIVE HIGH)**

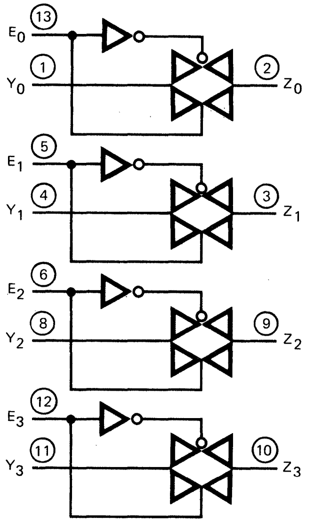
PIN NAMES

E_0–E_3	Enable Inputs
Y_0–Y_3	Input/Output Terminals
Z_0–Z_3	Input/Output Terminals

LOGIC DIAGRAM (1/4 OF A 4066B)

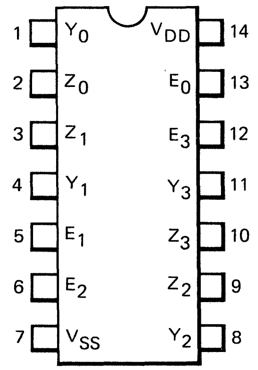


LOGIC SYMBOL



V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		190	900		100	450		80	250	Ω	MIN	$E_n = V_{DD}$ R_L = 10 kΩ to $V_{DD}/2$ $V_{is} = V_{DD}$ to V_{SS}
				270	1000		120	500		80	280		25°C	
				330	1090		170	520		130	300		MAX	
		XM		160	850		85	400		60	220	Ω	MIN.	
				270	1000		120	500		80	280		25°C	
				360	1150		190	550		145	320		MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels			25			10			5		Ω	25°C	$E_n = V_{DD}$ R_L = 10 kΩ to $V_{DD}/2$ $V_{is} = V_{DD}$ or V_{SS}
I_Z	OFF State Leakage Current	XC									±300	nA	MIN, 25°C	$E_n = V_{SS}$ $V_{is} = V_{DD}$ or V_{SS} $V_{os} = V_{SS}$ or V_{DD}
											±1000		MAX	
		XM									±100		MIN, 25°C	
											±1000		MAX	
I_{DD}	Quiescent Power Supply Dissipation	XC			1			2			4	μA	MIN, 25°C	All inputs at V_{DD} or V_{SS}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		8	45		3	30		2	20	ns	C_L = 50 pF, R_L = 200 Ω to V_{SS} Input Transition Times ≤ 20 ns E_n = V_{DD} V_{is} = V_{DD} (square wave)
t_{PHL}			8	45		4	30		2	20		
t_{PZL}	Output Enable Time		32	125		16	60		13	50	ns	C_L = 50 pF, R_L = 1 kΩ to V_{SS} or V_{DD} E_n = V_{DD} (square wave) Input Transition Times ≤ 20 ns V_{is} = V_{DD} or V_{SS}
t_{PZH}			32	125		16	60		13	50		
t_{PLZ}	Output Disable Time		380			380			400		ns	
t_{PHZ}			380			380			400			
	Distortion, Sine Wave Response		0.4			0.4			0.4		%	R_L = 10 kΩ Input Frequency = 1 kHz E_n = V_{DD} V_{is} = $V_{DD}/2$ (sine wave) p-p
	Crosstalk Between Any Two Switches					0.9					MHz	R_L = 1 kΩ E_A = V_{DD}, E_B = V_{SS} V_{is} = $V_{DD}/2$ (sine wave) p-p 20 Log_{10} $[V_{os}(B)/V_{is}(A)]$ = -50 dB
	Crosstalk, Enable Input to Output					50					mV	Input Transition Times ≤ 20 ns $R_{L(OUT)}$ = 1 kΩ $R_{L(IN)}$ = 50 Ω E_n = V_{DD} (square wave)
	OFF State Feedthrough					1.25					MHz	R_L = 1 kΩ, E_n = V_{SS} V_{is} = $V_{DD}/2$ (sine wave) p-p 20 Log_{10} (V_{os}/V_{is}) = -50 dB
	ON State Frequency Response					40					MHz	R_L = 1 kΩ V_{is} = $V_{DD}/2$ (sine wave) p-p E_n = V_{DD}, 20 Log_{10} $(V_{os}/V_{os}$ @ 1 kHz) = -3 dB
f_{MAX}	Enable Input Frequency (Note 4)					10					MHz	C_L = 50 pF, R_L = 1 kΩ Input Transition Times ≤ 20 ns E_n = V_{DD} (square wave) V_{os} = $V_{is}/2$ at DC V_{is} = V_{DD}
C_{is}	Input Switch Capacitance					4					pF	V_{DD} = 10 V E_n = V_{SS} V_{is} = Open 100 kHz or 1 MHz Bridge
C_{os}	Output Switch Capacitance					4					pF	
C_{ios}	Feedthrough Switch Capacitance					0.2					pF	

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11 the voltage drop across the bidirectional switch must not exceed 0.5 V at $T_A \leq 25°C$, or 0.3 V at $T_A > 25°C$. No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.

4067B

16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

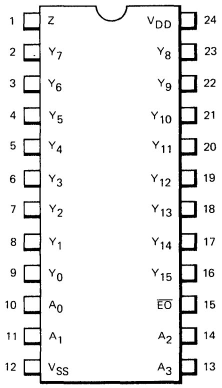
DESCRIPTION – The 4067B is a 16-Channel Analog Multiplexer/Demultiplexer with four Address Inputs (A_0-A_3), 16 Independent Inputs/Outputs (Y_0-Y_{15}), an active LOW Output Enable input ($\overline{EO}$), and a Common Input/Output (Z). The 4067B contains 16 bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0-Y_{15}) and the other side connected to a Common Input/Output (Z). One of the 16 switches is selected (low impedance, ON state) by the four Address Inputs (A_0-A_3) when the Output Enable input ($\overline{EO}$) is LOW. All unselected switches are in the high impedance OFF state. With the Output Enable input ($\overline{EO}$) HIGH, all 16 switches are in the high impedance OFF state. The Analog Input/Outputs (Y_0-Y_{15},Z) can swing between V_{DD} and V_{SS}. V_{DD}-V_{SS} may not exceed 15 V.

- **ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER**
- **24-PIN PACKAGE**
- **SINGLE POWER SUPPLY**

PIN NAMES

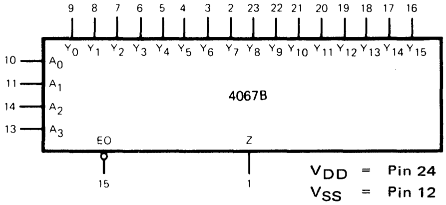
Y_0–Y_{15}	Independent Inputs/Outputs
A_0–A_3	Address Inputs
Z	Common Input/Output
$\overline{EO}$	Output Enable Input (Active LOW)

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC SYMBOL



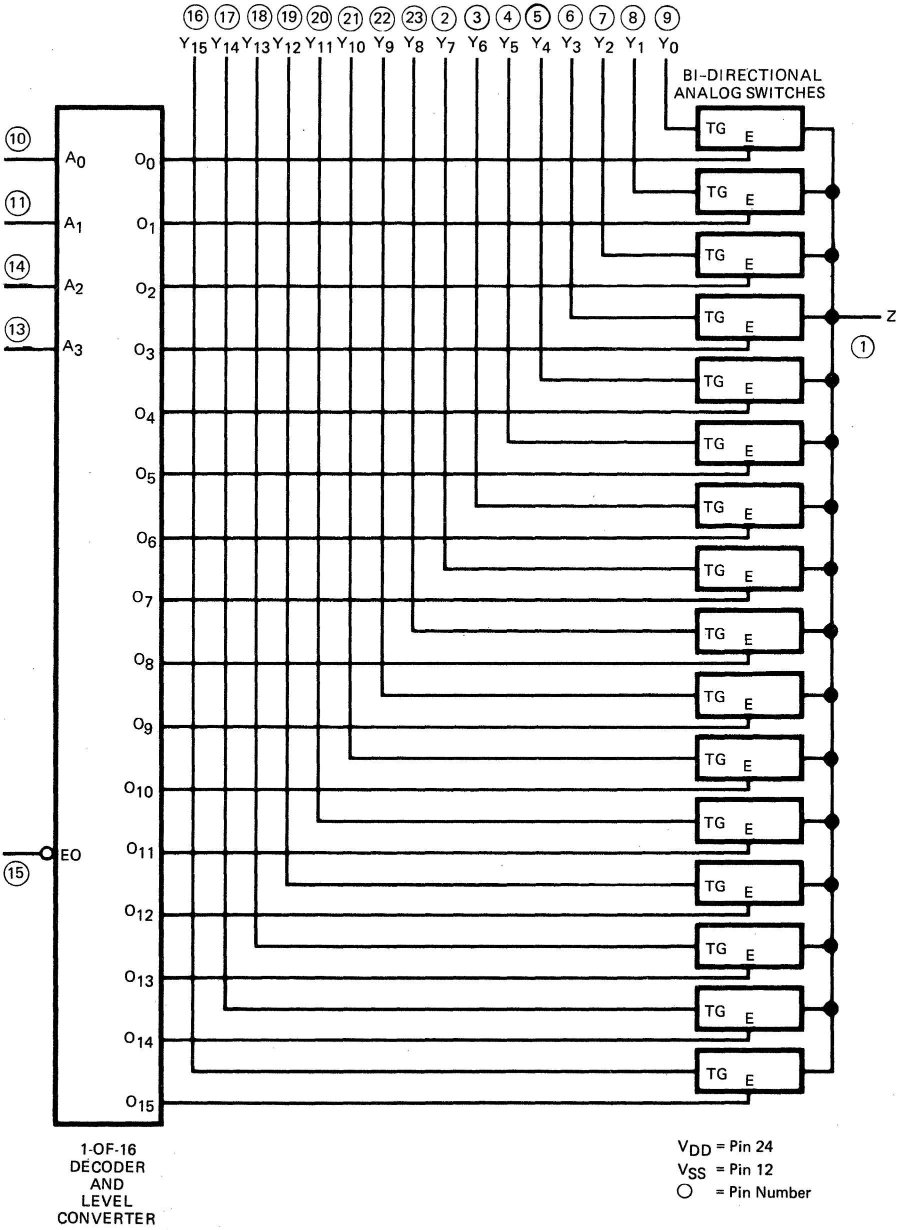
V_{DD} = Pin 24
V_{SS} = Pin 12

TRUTH TABLE

INPUTS				CHANNEL															
A_3	A_2	A_1	A_0	Y_0-Z	Y_1-Z	Y_2-Z	Y_3-Z	Y_4-Z	Y_5-Z	Y_6-Z	Y_7-Z	Y_8-Z	Y_9-Z	Y_{10}-Z	Y_{11}-Z	Y_{12}-Z	Y_{13}-Z	Y_{14}-Z	Y_{15}-Z
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
H	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
H	L	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
H	L	H	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
H	L	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
H	H	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
H	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
H	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

L = LOW Level H = HIGH Level $\overline{EO}$ = LOW Level

FUNCTIONAL LOGIC DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	V_{DD} = 15 V MIN	V_{DD} = 15 V TYP	V_{DD} = 15 V MAX	UNITS	TEMP	TEST CONDITIONS
R_{ON}	ON Resistance	XC		95	900		55	380		35	210	Ω	MIN	V_{is} = V_{DD} to V_{SS} Note 2
				100	1000		65	500		40	280		25°C	
				125	1100		100	600		65	340		MAX	
		XM		90	850		50	340		30	190	Ω	MIN	
				100	1000		65	500		40	280		25°C	
				150	1150		110	660		70	370		MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels			25			10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	$\overline{EO}$ = V_{DD} V_{is}= V_{DD} or V_{SS} V_{os} = V_{SS} or V_{DD}
		XM						80						
	Any Channel OFF	XC						100						$\overline{EO}$ = V_{SS} V_{is} = V_{DD} or V_{SS} V_{os} = V_{SS} or V_{DD}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40			80	µA	MIN, 25°C	All Inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25°C$ (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		25			10			6		ns	$C_L = 50$ pF, $R_L = 200$ kΩ
t_{PHL}	Input to Output		10			6			4			$\overline{EO} = V_{SS}$
t_{PLH}	Propagation Delay,		170			95			80		ns	A_n or $V_{is} = V_{DD}$ or V_{SS}
t_{PHL}	Address to Output		210			125			95			Note 5
t_{PZL}	Output Enable Time		185			95			75		ns	$C_L = 50$ pF, R_L @ 1 kΩ
t_{PZH}			205			105			85			$\overline{EO}$ or $A_n = V_{SS}$
t_{PLZ}	Output Disable Time		1250			1130			1080		ns	$V_{is} = V_{DD}$ or V_{SS}
t_{PHZ}			1240			1120			1070			Note 5
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	$R_L = 10$ kΩ, $\overline{EO} = V_{SS}$ $V_{is} = V_{DD}/2$ (sine wave) p-p $f_{is} = 1$ kHz
	Crosstalk Between Any Two Channels					1					MHz	$R_L = 1$ kΩ, $\overline{EO} = V_{SS}$ $V_{is} = V_{DD}/2$ (sine wave) p-p at –40 dB 20 Log_{10} $(V_{os}/V_{is}) = -40$ dB
	OFF State Feedthrough					1					MHz	$R_L = 1$ kΩ, $\overline{EO} = V_{DD}$ $V_{is} = V_{DD}/2$ (sine wave) p-p 20 Log_{10} $(V_{os}/V_{is}) = -40$ dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	$R_L = 1$ kΩ, $\overline{EO} = V_{SS}$ $V_{is} = V_{DD}/2$ (sine wave) p-p 20 Log_{10} (V_{os}/V_{os} @ 1 kHz) = –3 dB

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. $\overline{EO} = V_{SS}$, $R_L = 10$ kΩ, any channel selected.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
5. $V_{IN} = V_{DD}$ (Square Wave), Input transition times $\leqslant 20$ ns.
6. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 2, 3, 4, 5, 6, 7, 8, 9, 16, 17, 18, 19, 20, 21, 22, or 23 the voltage drop across the bidirectional switch must not exceed 0.5 V at $T_A \leqslant 25°C$, or 0.3 V at $T_A > 25°C$. No V_{DD} current will flow through R_L if the switch current flows into terminal 1.

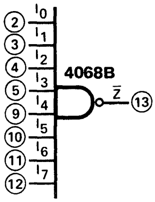
4068B

8-INPUT NAND GATE

DESCRIPTION — This CMOS logic element provides the positive 8-Input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

4068B LOGIC SYMBOL

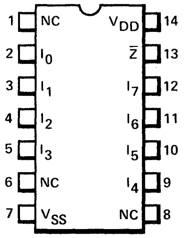
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 1, 6, 8



PIN NAMES

I_0–I_7	NAND Gate Inputs
$\overline{Z}$	Output (Active LOW)

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

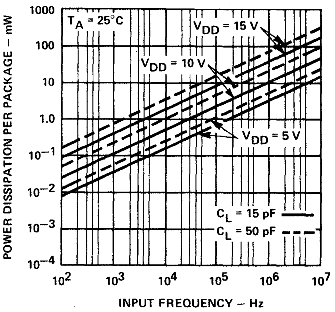
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		82	200		40	85		29	68	ns	C_L = 50 pF,
t_{PHL}			88	200		40	85		28	68	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		64	135		32	70		24	45	ns	Input Transition
t_{THL}			55	135		23	70		16	45		Times ≤ 20 ns

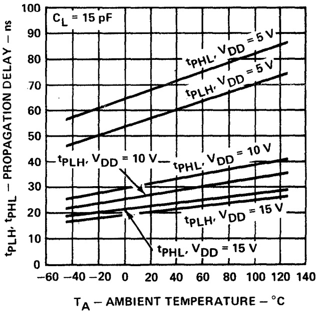
NOTE:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

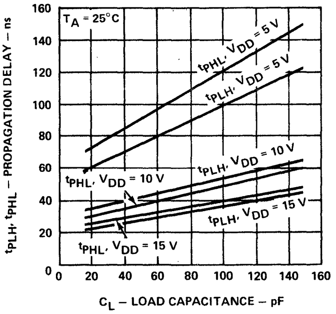
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

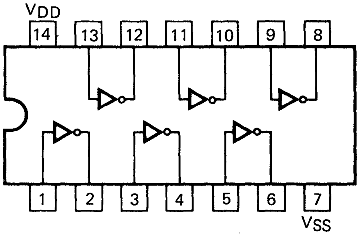


4069UB/74C04/54C04

HEX INVERTER

DESCRIPTION – The 4069UB is a general purpose Hex Inverter which has standard Fairchild input and output characteristics. A single-stage design has been used since the output impedance of a single-input gate is not pattern sensitive. The 4096UB is a Direct Replacement for the 74C04/54C04.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent	XC			1			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
	Power				7.5			15			30		MAX	
	Supply	XM			0.25			0.5			1	μA	MIN, 25°C	
	Current				7.5			15			30		MAX	

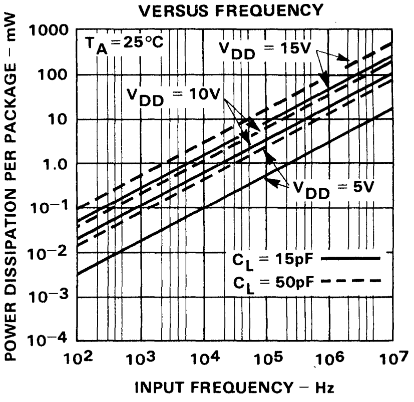
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		32	64		16	32		13	26	ns	C_L = 50 pF,
t_{PHL}			32	64		16	32		13	26		R_L = 200 kΩ
t_{TLH}	Output Transition Time		45	135		23	70		18	45	ns	Input Transition
t_{THL}			45	135		23	70		18	45		Times ≤ 20 ns

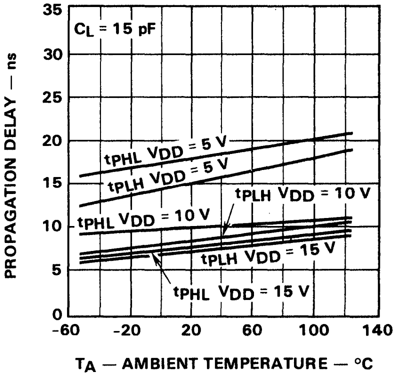
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

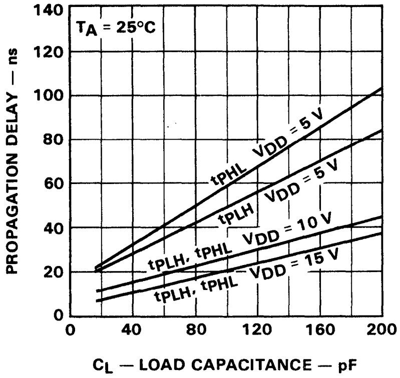
TYPICAL POWER DISSIPATION VERSUS FREQUENCY



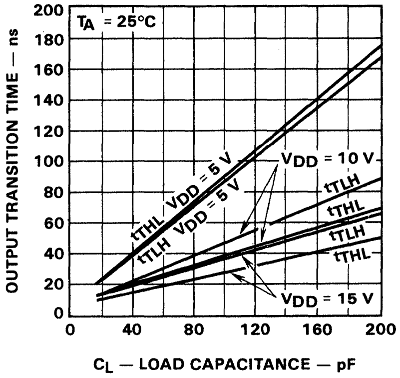
PROPAGATION DELAY VERSUS TEMPERATURE



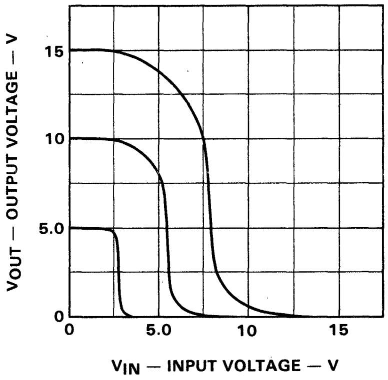
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



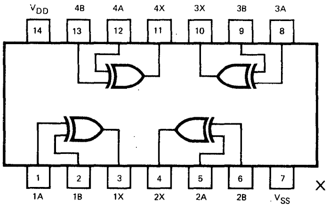
TYPICAL VOLTAGE TRANSFER CHARACTERISTICS



4070B/74C86/54C86

QUAD EXCLUSIVE-OR GATE

DESCRIPTION — The 4070B CMOS logic element provides the Exclusive-OR function. The outputs are fully buffered for best performance. The 4070B is a direct replacement for the 74C86/54C86.



$X = \bar{A}B + A\bar{B}$

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)

NOTE:
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

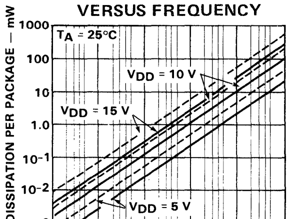
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

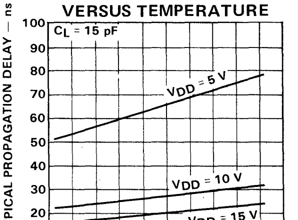
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

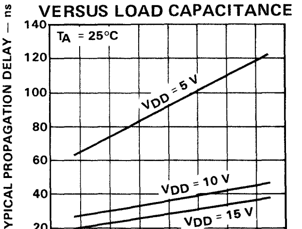
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		85	170		45	90		27	72	ns	C_L = 50 pF,
t_{PHL}	A or B to X		85	170		45	90		27	72	ns	R_L = 200 kΩ
t_{TLH}	Output Transition		50	100		23	50		17	35	ns	Input Transition
t_{THL}	Time		50	100		23	50		17	35	ns	Times ≤ 20 ns

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS


POWER DISSIPATION VERSUS FREQUENCY


PROPAGATION DELAY VERSUS TEMPERATURE

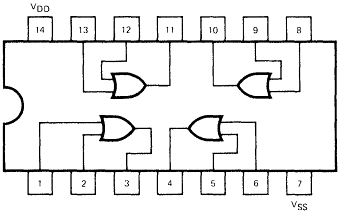

PROPAGATION DELAY VERSUS LOAD CAPACITANCE

4071B

QUAD 2-INPUT OR GATE

DESCRIPTION – The 4071B is a positive logic Quad 2-Input OR Gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

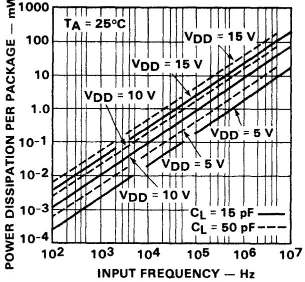
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		43	85		22	40		17	32	ns	C_L = 50 pF,
t_{PHL}			52	100		23	40		15	32	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		45	135		24	70		18	45	ns	Input Transition
t_{THL}			54	135		21	70		15	45	ns	Times ≤ 20 ns

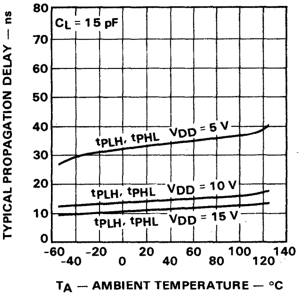
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

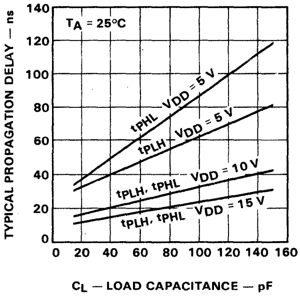
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

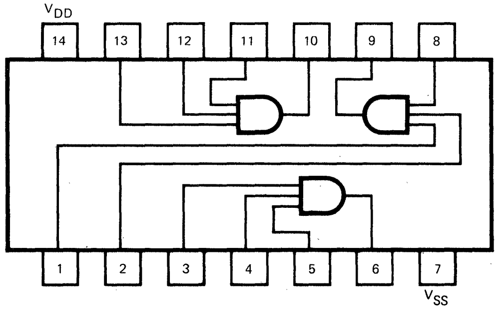


4073B

TRIPLE 3-INPUT AND GATE

DESCRIPTION — This CMOS logic element provides the positive Triple 3-Input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		40	110		19	55		14	44	ns	C_L = 50 pF,
t_{PHL}			44	110		26	55		21	44		R_L = 200 kΩ
t_{TLH}	Output Transition Time		70	135		35	75		25	45	ns	Input Transition
t_{THL}			70	135		35	75		25	45		Times ≤ 20 ns

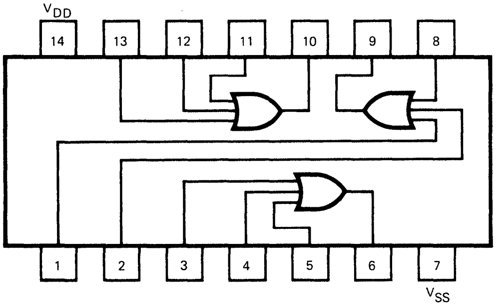
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

4075B

TRIPLE 3-INPUT OR GATE

DESCRIPTION – This CMOS logic element provides the positive Triple 3-Input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		59	130		34	65		28	50	ns	C_L = 50 pF,
t_{PHL}			62	130		30	65		24	50		R_L = 200 kΩ
t_{TLH}	Output Transition Time		70	135		35	75		25	35	ns	Input Transition
t_{THL}			70	135		35	75		25	35		Times ≤ 20 ns

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

4076B/74C173/54C173

QUAD D FLIP-FLOP WITH 3-STATE OUTPUT

DESCRIPTION – The 4076B is a Quad Edge-Triggered D Flip-Flop with four Data Inputs (D_0-D_3), two active LOW Data Enable Inputs ($\overline{ED}_0$-$\overline{ED}_1$), an edge-triggered Clock Input (CP), four 3-State Outputs (Q_0-Q_3), two active LOW Output Enable inputs ($\overline{EO}_0$, $\overline{EO}_1$), and an overriding asynchronous Master Reset Input (MR).

Information on the Data Inputs (D_0-D_3) is stored in the four flip-flops on the LOW-to-HIGH transition of the Clock Input (CP) if both Data Enable Inputs ($\overline{ED}_0$-$\overline{ED}_1$) are LOW. A HIGH on either Data Enable Input ($\overline{ED}_0$-$\overline{ED}_1$) prevents the flip-flops from changing on the LOW-to-HIGH transition of the Clock Input (CP), independent of the information on the Data Inputs (D_0-D_3).

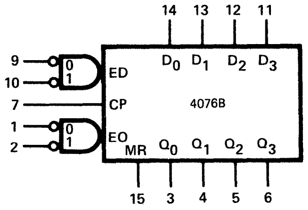
When both Output Enable inputs ($\overline{EO}_0$-$\overline{EO}_1$) are LOW, the contents of the four flip-flops are available at the outputs (Q_0-Q_3). A HIGH on either Output Enable input ($\overline{EO}_0$, $\overline{EO}_1$) forces the outputs (Q_0-Q_3) into the high impedance OFF state.

A HIGH on the overriding asynchronous Master Reset Input (MR) resets all four flip-flops, indepedent of all other input conditions.

The 4076B is a direct replacement for the 54C173/74C173.

- **FULLY INDEPENDENT CLOCK**
- **3-STATE OUTPUTS**
- **CLOCK IS L → H EDGE-TRIGGERED**
- **ACTIVE LOW DATA ENABLE INPUTS**
- **ACTIVE LOW OUTPUT ENABLE INPUTS**
- **ASYNCHRONOUS MASTER RESET**

LOGIC SYMBOL

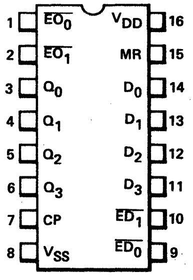


V_{DD} = Pin 16
V_{SS} = Pin 8

PIN NAMES

D_0-D_3	Data Inputs
$\overline{ED}_0$-$\overline{ED}_1$	Data Enable Inputs (Active LOW)
$\overline{EO}_0$, $\overline{EO}_1$	Output Enable Inputs (Active LOW)
CP	Clock Input (L → H Edge-Triggered)
MR	Master Reset Input
Q_0-Q_3	Data Outputs

CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

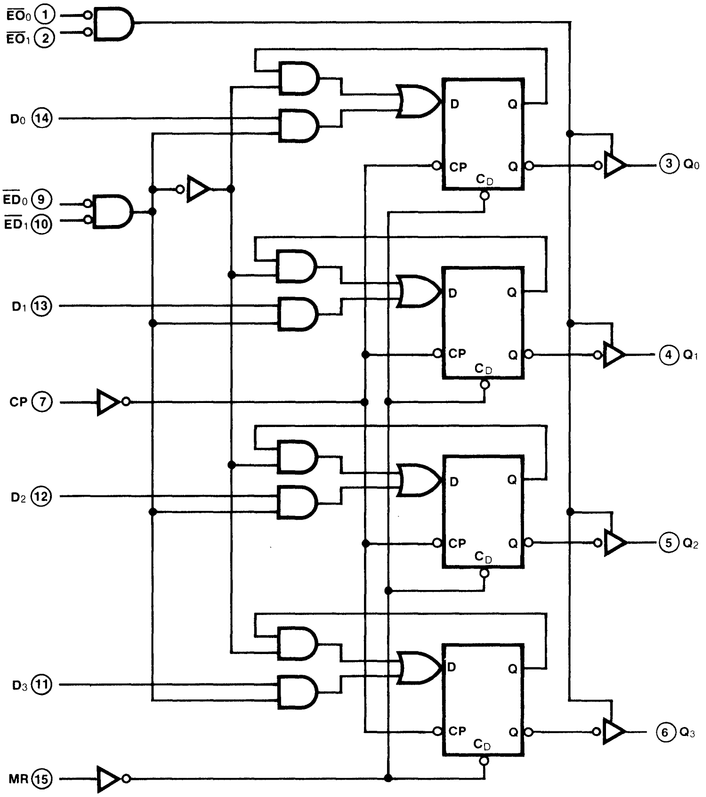
INPUTS			OUTPUTS
$\overline{ED}_0$	$\overline{ED}_1$	D_n	Q_{n+1}
H	X	X	Q_n
X	H	X	Q_n
L	L	L	L
L	L	H	H

CONDITIONS:

MR = $\overline{EO}_0$ = $\overline{EO}_1$ = LOW
L = LOW Level
H = HIGH Level
X = Don't Care
Q_{n+1} = State After Positive Clock Transition

NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current High	XC									1.6	µA	MIN, 25°C	Output returned to V_{DD}. $\overline{EO}_1$ = $\overline{EO}_0$ = V_{DD}
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	µA	MIN, 25°C	Output returned to V_{SS}. $\overline{EO}_1$ = $\overline{EO}_0$ = V_{DD}
											-12		MAX	
		XM									-0.4		MIN, 25°C	
											-12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			10	µA	MIN, 25°C	
					150			300			600		MAX	

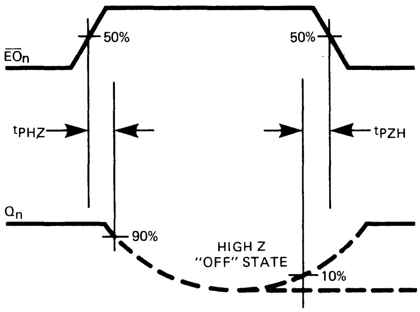
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		70	210		35	105		25	75	ns	C_L = 50 pF,
t_{PHL}	CP to O_n		70	210		35	105		25	75	ns	R_L = 200 kΩ
t_{PHL}	Propagation Delay MR to O_n		80	240		40	120		25	75	ns	Input Transition Times ≤20 ns
t_{PZH}	Output Enable		95	290		50	150		35	105	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}	Time		95	290		50	150		35	105	ns	(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable		95	290		50	150		35	105	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}	Time		95	290		50	150		35	105	ns	(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition		65	160		40	90		15	35	ns	
t_{THL}	Time		65	160		40	90		15	35	ns	
t_wCP(L)	Minimum Clock Pulse Width	80	25		45	10		36	8		ns	
t_wMR(H)	Minimum MR Pulse Width	60	35		30	20		24	15		ns	
t_{rec}	MR Recovery Time		6			5			2		ns	
t_s	Set-Up Time, D_n to CP	15	1		5	1		2	0		ns	
t_h	Hold-Time, D_n to CP	45	10		20	2		10	2		ns	
t_s	Set-Up Time, $\overline{ED}_n$ to CP	100	50		40	20		30	15		ns	
t_h	Hold-Time, $\overline{ED}_n$ to CP	20	2		12	1		8	1		ns	
f_{MAX}	Maximum Clock Frequency (Note 3)	4	9		10	16		12	19		MHz	

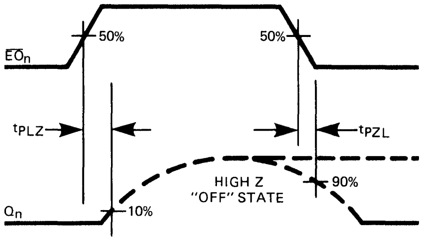
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 20 V, and 3 µs at V_{DD} = 15 V.

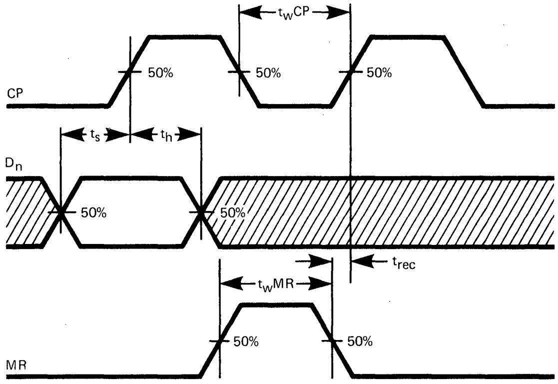
SWITCHING WAVEFORMS



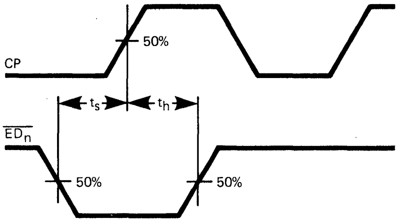
OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})



MINIMUM PULSE WIDTHS FOR CP AND MR, MR RECOVERY TIME, AND SET-UP AND HOLD-TIMES, D_N TO CP



SET-UP AND HOLD-TIMES $\overline{ED_N}$ TO CP

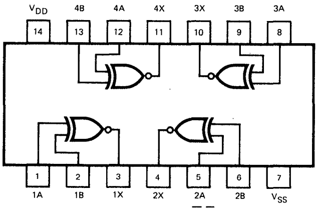
NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

4077B

QUAD EXCLUSIVE-NOR GATE

DESCRIPTION – The 4077B CMOS logic element provides the Exclusive-NOR function. The outputs are fully buffered for best performance. The 4077B may be used interchangeably for the 4811.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



$X = AB + \overline{A}\,\overline{B}$

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			5			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

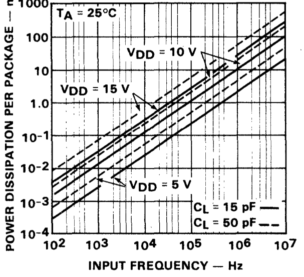
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5V			V_{DD} = 10V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		55	110		27	55		17	44	ns	C_L = 50 pF,
t_{PHL}	A or B to X		65	130		27	55		20	44	ns	R_L = 200 kΩ
t_{TLH}	Output Transition		53	100		20	50		15	35	ns	Input Transition
t_{THL}	Time		53	100		20	50		15	35	ns	Times ≤ 20 ns

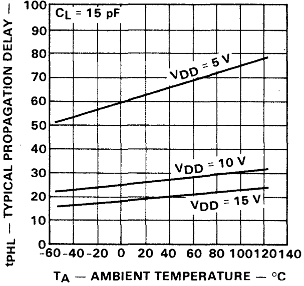
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

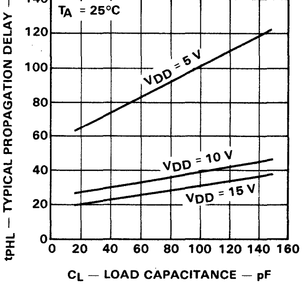
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

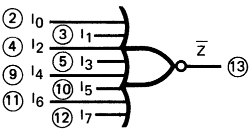


4078B

8-INPUT NOR GATE

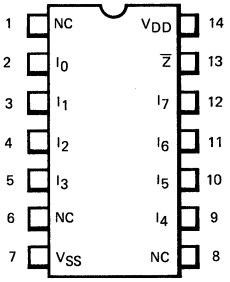
DESCRIPTION – This CMOS logic element provides the positive 8-Input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

4078B LOGIC SYMBOL



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 1, 6, 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

I_0–I_7	NOR Gate Inputs
$\overline{Z}$	Output (Active LOW)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

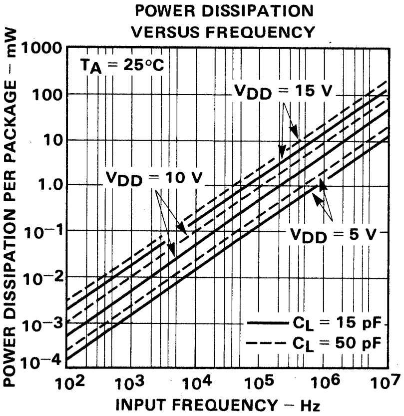
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	µA	MIN, 25°C	
					7.5			15			30		MAX	

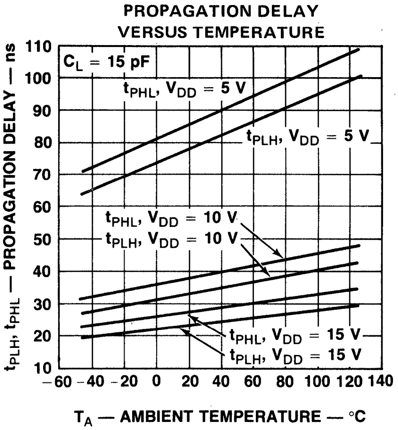
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

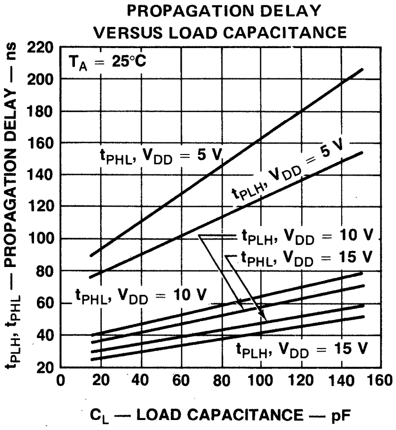
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		108	200		46	85		34	68	ns	C_L = 50 pF,
t_{PHL}			129	200		50	85		35	68	ns	R_L = 200 kΩ
t_{TLH}	Output Transition		76	135		39	70		30	45	ns	Input Transition
t_{THL}	Time		80	135		32	70		24	45	ns	Times ≤ 20 ns

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS





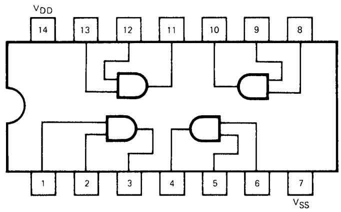


4081B

QUAD 2-INPUT AND GATE

DESCRIPTION — The 4081B is a positive logic Quad 2-Input AND Gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

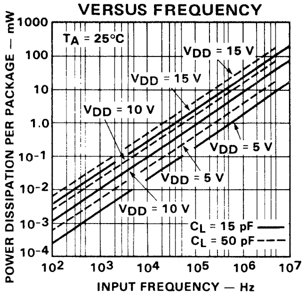
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	μA	MIN, 25°C	All inputs at 0V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

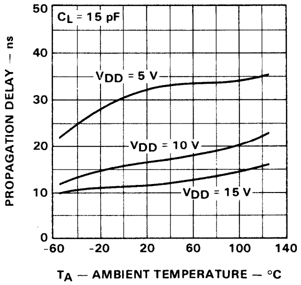
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

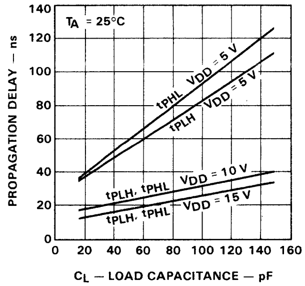
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		55	95		23	50		17	40	ns	C_L = 50 pF,
t_{PHL}			60	95		25	50		19	40	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		70	135		30	70		23	45	ns	Input Transiton
t_{THL}			57	135		23	70		16	45	ns	Times ⩽ 20 ns

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS


POWER DISSIPATION VERSUS FREQUENCY


PROPAGATION DELAY VERSUS TEMPERATURE


PROPAGATION DELAY VERSUS LOAD CAPACITANCE

4085B

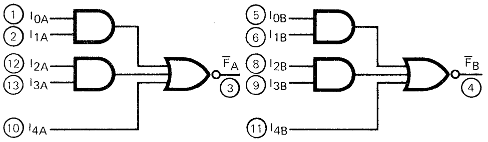
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

DESCRIPTION — The 4085B is a Dual 2-Wide 2-Input AND-OR-Invert (AOI) Gate, each with an additional input (I_{4A} or I_{4B}) which can be used as either an Expander Input or an Inhibit Input by connecting it to any standard CMOS output. A HIGH on this Input (I_4) forces the Output ($\overline{F}$) LOW independent of the other four inputs (I_0-I_3). The Outputs ($\overline{F_A}$ and $\overline{F_B}$) are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

PIN NAMES

I_{0A}-I_{4A}, I_{0B}-I_{4B}	Gate Inputs
$\overline{F}_A$, $\overline{F}_B$	Outputs (Active LOW)

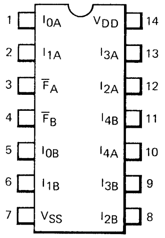
LOGIC DIAGRAM



$\overline{F} = \overline{I_0 \bullet I_1 + I_2 \bullet I_3 + I_4}$

V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	µA	MIN, 25°C	
					7.5			15			30		MAX	

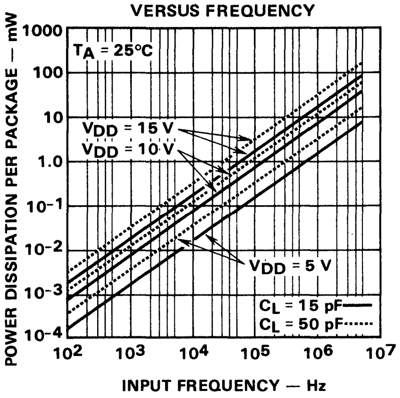
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		56	115		25	55		17	44	ns	C_L = 50 pF,
t_{PHL}	Any I to $\overline{F}$		74	135		30	65		20	52	ns	R_L = 200 kΩ
t_{TLH}	Output Transition		45	100		22	50		15	35	ns	Input Transition
t_{THL}	Time		45	100		22	50		15	35	ns	Times ≤ 20 ns

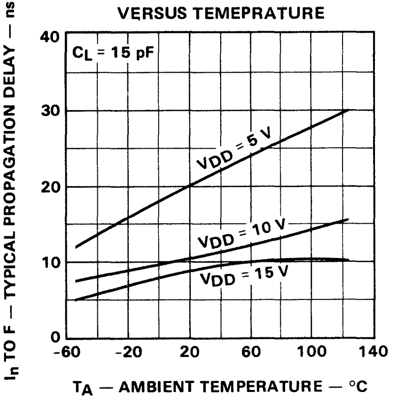
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

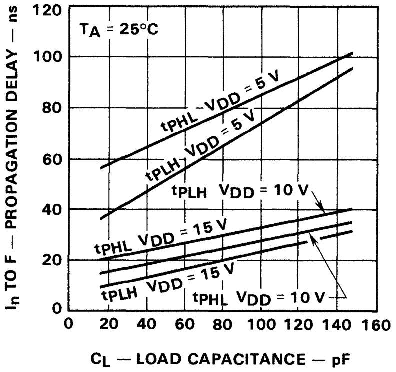
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMEPRATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



4086B

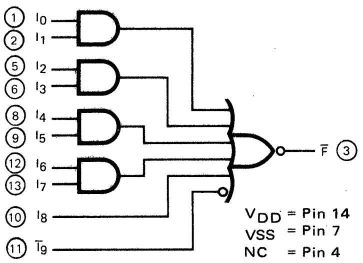
4-WIDE 2-INPUT AND-OR-INVERT GATE

DESCRIPTION – The 4086B is a 4-Wide 2-Input AND-OR-Invert (AOI) Gate with two additional inputs (I_8 and $\overline{I}_9$) which can be used as either expander inputs or inhibit inputs by connecting them to any standard CMOS output. A HIGH on I_8 or a LOW on $\overline{I}_9$ forces the Output ($\overline{F}$) LOW independent of the other eight inputs (I_0–I_7). The Output (F) is fully buffered for highest noise immunity and pattern insensitivity of output impedance.

PIN NAMES

I_0–I_8	Gate Inputs
$\overline{I}_9$	Gate Input (Active LOW)
$\overline{F}$	Output (Active LOW)

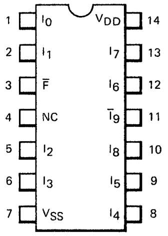
LOGIC DIAGRAM



$$\overline{F} = \overline{I_0 \bullet I_1 + I_2 \bullet I_3 + I_4 \bullet I_5 + I_6 \bullet I_7 + I_8 + I_9}$$

NOTE:
A HIGH on I_8 or a LOW on $\overline{I}_9$ forces the output ($\overline{F}$) LOW.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	µA	MIN, 25°C	
					7.5			15			30		MAX	

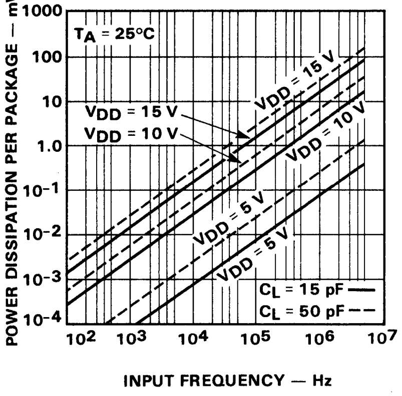
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, I_0 through I_8 to $\overline{F}$		100 100	180 180		40 40	80 80		25 25	64 64	ns ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{I}_9$ to $\overline{F}$		65 65	100 100		35 35	50 50		20 20	40 40	ns ns	
t_{TLH} t_{THL}	Output Transition Time		55 55	100 100		25 25	50 50		18 18	35 35	ns ns	

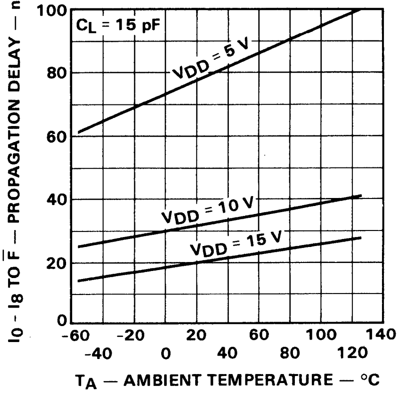
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

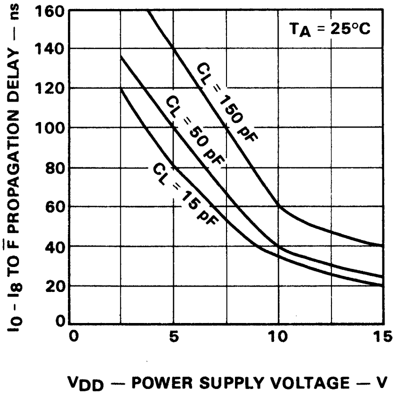
POWER DISSIPATION VERSUS FREQUENCY



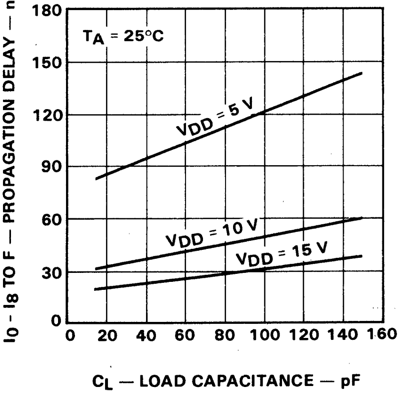
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



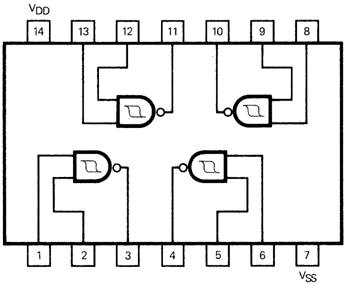
7

4093B

QUAD 2-INPUT NAND SCHMITT TRIGGER

GENERAL DESCRIPTION — The 4093B is a Quad 2-Input NAND Schmitt Trigger offering positive and negative threshold voltages, V_{T+} and V_{T-} which show very low variation with temperature (typically 0.0005 V/°C at V_{DD} = 10 V) and typical hysteresis, V_{T+} to $V_{T-} \geq 0.33\ V_{DD}$. Outputs are fully buffered for highest noise immunity.

LOGIC AND CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

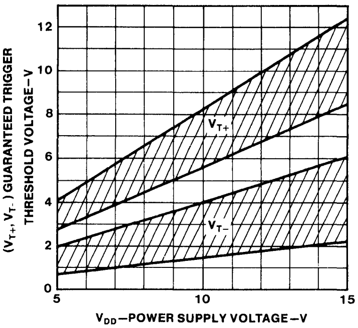
DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
V_{T+}	Positive-Going Threshold Voltage		2.9	3.6	4.3	6.0	6.8	8.6	9	10	12.9	V	ALL	$V_{IN} = V_{SS}$ to V_{DD}
V_{T-}	Negative-Going Threshold Voltage		0.7	1.4	1.9	1.4	3.2	4.0	2.1	5	6	V	ALL	$V_{IN} = V_{DD}$ to V_{SS}
V_{T+} to V_{T-}	Hysteresis		1.0	2.2	3.6	2.0	3.6	7.2	3	5	8	V	ALL	Guaranteed Hysteresis = V_{T+} Minus V_{T-}
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	μA	MIN, 25°C	All Inputs at OV or V_{DD}.
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

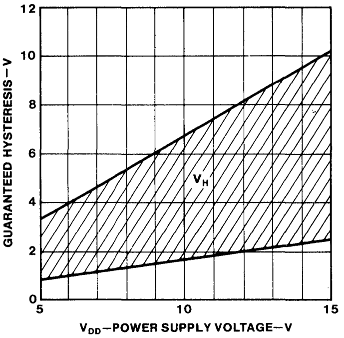
NOTES:

1. Additional dc characteristics are listed in this section under Fairchild 4000B series CMOS family characteristics.

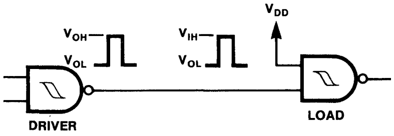
GUARANTEED TRIGGER THRESHOLD VERSUS V_{DD}

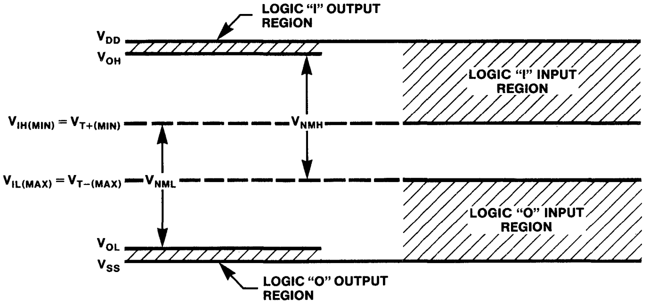


GUARANTEED HYSTERESIS VERSUS V_{DD}



INPUT AND OUTPUT CHARACTERISTICS

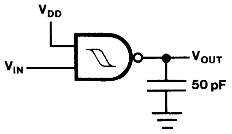


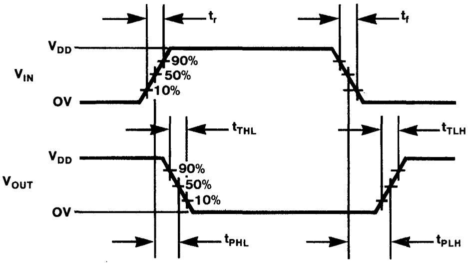


$$V_{NML} = V_{IH(MIN)} - V_{OL} \simeq V_{IH(MIN)} = V_{T+(MIN)}$$

$$V_{NMH} = V_{OH} - V_{IL(MAX)} \simeq V_{DD} - V_{IL(MAX)} = V_{DD} - V_{T-(MAX)}$$

AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS





AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS See Note 2
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		60	110		25	60		20	48	ns	C_L = 50 pF,
t_{PHL}			60	110		25	60		20	48	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		60	135		30	70		20	45	ns	Input Transition
t_{THL}			60	135		30	70		20	45	ns	Times ≤ 20 ns

NOTE:
Propagation Delays and Output Transitions Times are Grahically Described in Section Under Series CMOS Family Characteristics.

4104B

QUAD LOW VOLTAGE TO HIGH VOLTAGE TRANSLATOR WITH 3-STATE OUTPUTS

DESCRIPTION – The 4104B Quad Low Voltage to High Voltage Translator with 3-State Outputs provides the capability of interfacing low voltage circuits to high voltage circuits, such as low voltage CMOS and TTL to high voltage CMOS. It has four Data Inputs (I_0-I_3), an active HIGH Output Enable input (EO), four Data Outputs (Z_0-Z_3) and their Complements ($\overline{Z}_0$-$\overline{Z}_3$). With the Output Enable input HIGH, the Outputs (Z_0-Z_3, $\overline{Z}_0$-$\overline{Z}_3$) are in the low impedance "ON" state, either HIGH or LOW as determined by the Data Inputs; with the Output Enable input LOW, the Outputs are in the high impedance "OFF" state. The voltage level on the Output Enable input may swing between V_{DDI} and V_{SS}.

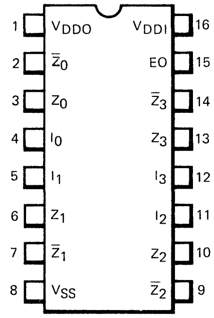
The device uses a common negative supply (V_{SS}) and separate positive supplies for inputs (V_{DDI}) and outputs (V_{DDO}). V_{DDI} must always be less than or equal to V_{DDO}, even during power turn-on and turn-off. For the allowable operating range of V_{DDI} and V_{DDO} see Figure 1. Each input protection circuit is terminated between V_{DDO} and V_{SS}. This allows the input signals to be driven from any potential between V_{DDO} and V_{SS}, without regard to current limiting. When driving from potentials greater than V_{DDO} or less than V_{SS}, the current at each input must be limited to 10 mA.

When used in a bus organized system, all 4104B devices on the same bus line should be connected to the same V_{DDO} and V_{SS} supplies. Otherwise, parasitic diodes from the output to V_{DDO} and V_{SS} can become forward biased, even while the device is in the OFF state, causing catastrophic failure if the current is not limited to 10 mA.

- **3-STATE FULLY BUFFERED OUTPUTS**
- **OUTPUT ENABLE INPUT (ACTIVE HIGH)**
- **DUAL POWER SUPPLY**

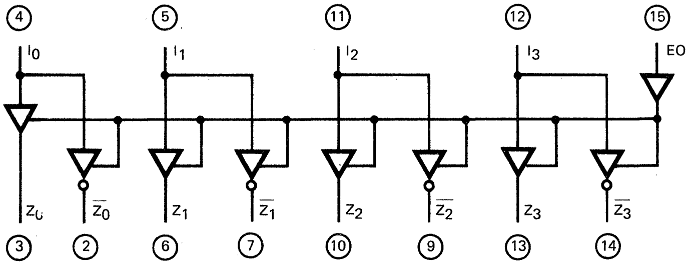
PIN NAMES	FUNCTION
I_0-I_3	Data Inputs
EO	Output Enable Input
Z_0-Z_3	Data Outputs
$\overline{Z_0}$-$\overline{Z_3}$	Complimentary Data Outputs

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC SYMBOL



V_{DDO} = Pin 1
V_{DDI} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: $V_{DDO} = V_{DDI}$ as shown, $V_{SS} = 0$ V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DDO/I} = 5$ V			$V_{DDO/I} = 10$ V			$V_{DDO/I} = 15$ V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		3.5		Note 1	7		Note 1	11		Note 1	V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage		Note 2		1.5	Note 2		3	Note 2		4	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		4.95			9.95			14.95			V	MIN, 25°C	$I_{OH} < 1$ µA Note 3
			4.95			9.95			14.95				MAX	
			4.5			9.0			13.5				All	$I_{OL} < 1$ µA Note 4
V_{OL}	Output LOW Voltage				0.05			0.05			0.05	V	MIN, 25°C	$I_{OL} < 1$ µA Note 3
					0.05			0.05			0.05		MAX	
					0.5			1.0			1.5		All	$I_{OH} < 1$ µA Note 4
I_{IN}	Input Current	XC									0.3	µA	MIN, 25°C	Lead Under Test at 0 V or V_{DDO}. All Other Inputs Simultaneously at 0 V or V_{DDO}
											1.0		MAX	
		XM									0.1	µA	MIN, 25°C	
											1.0		MAX	
I_{OH}	Output HIGH Current		-1.5									mA	MIN, 25°C	$V_{OUT} = 2.5$ V for $V_{DDO} = 5$ V Note 3
			-1.0										MAX	
			-0.7			-1.4			-2.2				MIN, 25°C	$V_{OUT} = V_{DDO}$ -0.5 V Note 3
			-0.4			-0.8			-1.4				MAX	
I_{OL}	Output LOW Current		1.0 0.8 0.4			2.6 2.0 1.2			3.6 3.6 2.0			mA	MIN, 25°C MAX	$V_{OUT} = 0.4$ V for $V_{DDO} = 5$ V $V_{OUT} = 0.5$ V for $V_{DDO} = 10$ V $V_{OUT} = 0.5$ V for $V_{DDO} = 15$ V Note 3
I_{OZH}	Output OFF Current HIGH	XC									1.6	µA	MIN, 25°C	Output Returned to V_{DDO}, EO = V_{SS}
											12		MAX	
		XM									0.4	µA	MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	µA	MIN, 25°C	Output Returned to V_{SS}, EO = V_{SS}
											-12		MAX	
		XM									-0.4	µA	MIN, 25°C	
											-12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All Inputs at 0 V or $V_{DDI} = V_{DDO}$
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

NOTES:

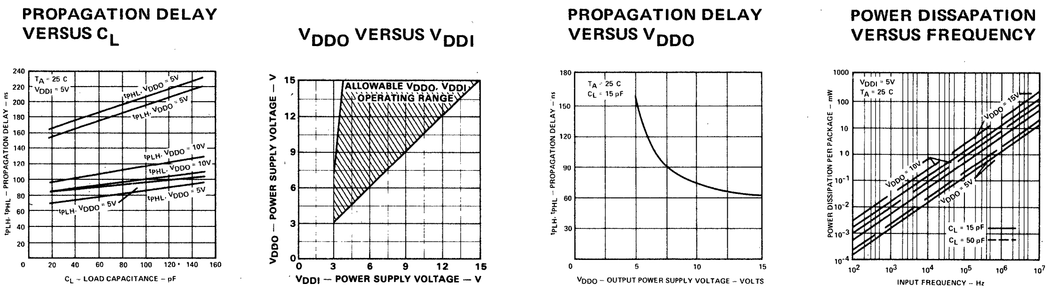
1. V_{IH} must be less than or equal to V_{DDO}. If V_{IH} is greater than V_{DDO}, current at each input must be limited to 10 mA.
2. V_{IL} must be greater than or equal to V_{SS}, if V_{IL} is less than V_{SS}, current at each input must be limited to 10 mA.
3. Inputs at 0 V or V_{DDO} per function.
4. Inputs at minimum V_{IH} or maximum V_{IL} per function.
5. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DDI} = 5 V, V_{DDO} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 5)

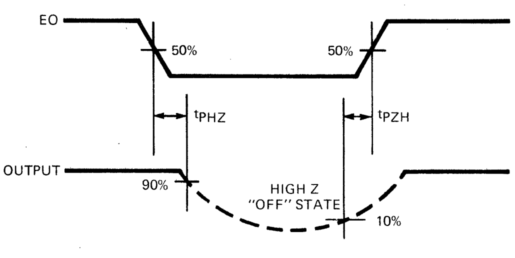
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DDO} = 5 V			V_{DDO} = 10 V			V_{DDO} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, I_n to Z_n or $\overline{Z}_n$		160 160	375 375		85 85	180 180		75 75	144 144	ns	C_L = 50 pF, R_L = 200 kΩ
t_{PZH} t_{PZL}	Output Enable Time		200 200	450 450		80 100	110 170		70 80	88 136	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DDO})
t_{PHZ} t_{PLZ}	Output Disable Time		75 50	165 115		90 80	170 110		75 70	136 88	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DDO})
t_{TLH} t_{THL}	Output Transition Time		60 60	135 135		30 30	70 70		25 25	45 45	ns	Input Transition Times ⩽ 20 ns

Notes on previous page.

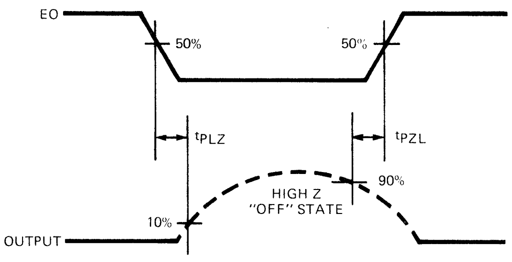
Fig. 1 TYPICAL ELECTRICAL CHARACTERISTICS



SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

4510B

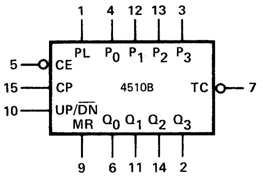
UP/DOWN DECADE COUNTER

DESCRIPTION – The 4510B is an Edge-Triggered Synchronous Up/Down BCD Counter with a Clock Input (CP), an active HIGH Up/Down Count Control Input (Up/$\overline{\text{Dn}}$), an active LOW Count Enable Input ($\overline{\text{CE}}$), an asynchronous active HIGH Parallel Load Input (PL), four Parallel Inputs (P_0-P_3), four Parallel Outputs (Q_0-Q_3), an active LOW Terminal Count Output ($\overline{\text{TC}}$) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except the Master Reset Input (MR) which must be LOW. With the Parallel Load Input (PL) LOW, the counter changes on the LOW-to-HIGH transition of the Clock Input (CP) if the Count Enable Input ($\overline{\text{CE}}$) is LOW. The Up/Down Count Control Input (Up/$\overline{\text{Dn}}$) determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, the Terminal Count Output ($\overline{\text{TC}}$) is LOW when the Parallel Outputs $Q_0 \cdot Q_3$ are HIGH and the Count Enable ($\overline{\text{CE}}$) is LOW. When counting down, the Terminal Count Output ($\overline{\text{TC}}$) is LOW when all the Parallel Outputs (Q_0-Q_3) and the Count Enable Input ($\overline{\text{CE}}$) are LOW. A HIGH on the Master Reset Input resets the counter (Q_0-Q_3 = LOW) independent of all other input conditions.

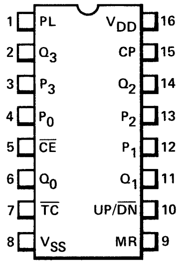
- **UP/DOWN COUNT CONTROL**
- **SINGLE CLOCK INPUT (L→H EDGE-TRIGGERED)**
- **ASYNCHRONOUS PARALLEL LOAD INPUT**
- **ASYNCHRONOUS MASTER RESET**
- **EASILY CASCADABLE**

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



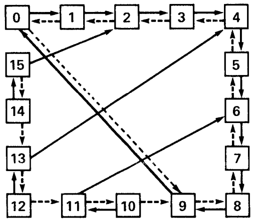
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

MODE SELECTION TABLE

PL	UP/$\overline{\text{DN}}$	$\overline{\text{CE}}$	CP	MODE
H	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	H	X	No Change
L	L	L	↑	Count Down, Decade
L	H	L	↑	Count Up, Decade

MR = LOW
H = HIGH Level
L = LOW Level
X = Don't Care
↑ = Positive-Going Transition

4510B STATE DIAGRAM



Count Up ————
Count Down – – – – –

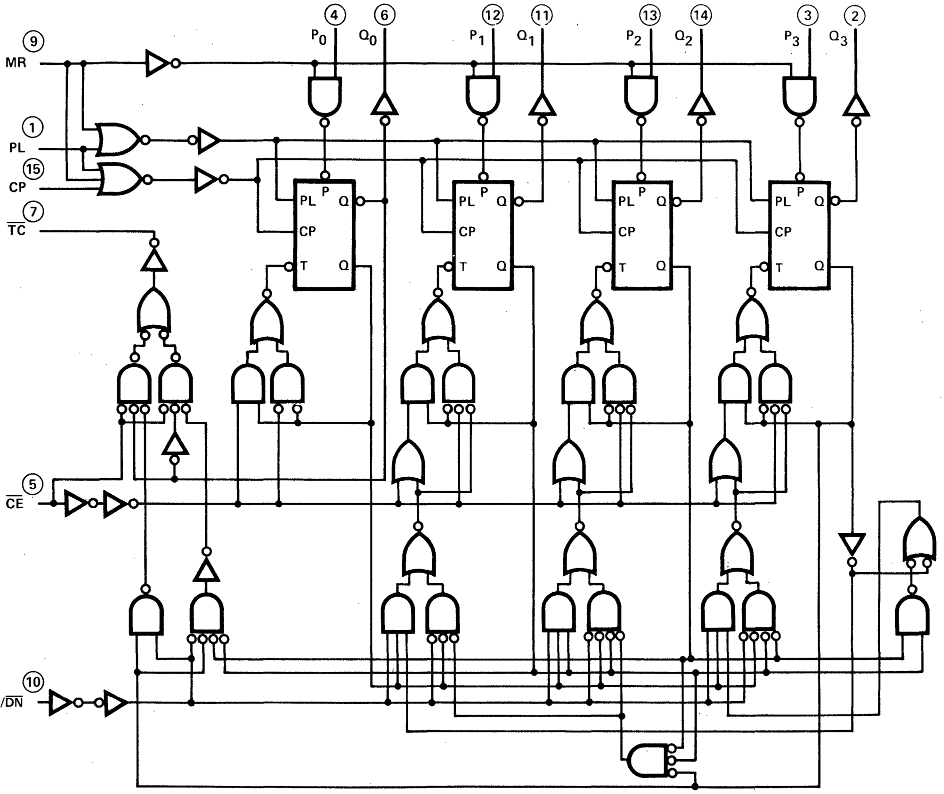
LOGIC EQUATION FOR TERMINAL COUNT

$$TC = CE \bullet [(UP \bullet Q_0 \bullet Q_3) + (\overline{UP} \bullet \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3)]$$

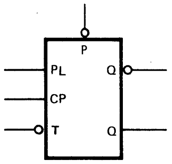
PIN NAMES

PL	Parallel Load Input (Active HIGH)
P_0-P_3	Parallel Inputs
$\overline{\text{CE}}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (L → H Edge-Triggered)
Up/$\overline{\text{Dn}}$	Up/Down Count Control Input
MR	Master Reset Input
$\overline{\text{TC}}$	Terminal Count Output (Active LOW)
Q_0-Q_3	Parallel Outputs

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number



PL (Parallel Load Input) — Asynchronously Loads P into Q, Overriding all Other Inputs
P (Parallel Input) — Data on this Pin is Asynchronously Loaded into Q, when PL is HIGH Overriding all Other Inputs
CP (Clock Pulse Input)
Q, $\overline{Q}$ (True and Complimentary Outputs)
T (Toggle Input) — Forces the Q output to synchronously toggle when a HIGH is placed on this input.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

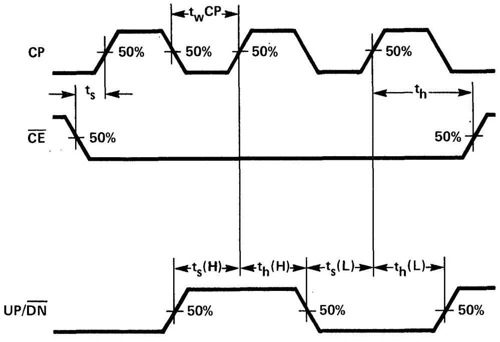
Notes on folowing page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25°C$ (See Note 2)

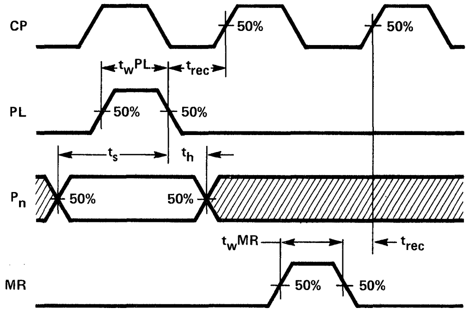
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		150	350		62	160		41	128	ns	$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ≤ 20 ns
t_{PHL}			150	350		59	160		39	128		
t_{PLH}	Propagation Delay, CP to $\overline{TC}$		167	450		71	180		48	144	ns	
t_{PHL}			252	650		100	245		66	196		
t_{PLH}	Propagation Delay, PL to Q_n		170	325		70	150		45	120	ns	
t_{PHL}			220	425		90	195		62	156		
t_{PLH}	Propagation Delay, MR to Q_n, $\overline{TC}$		225	500		170	210		105	168	ns	
t_{PHL}			205	450		120	190		80	152		
t_{TLH}	Output Transition Time		60	135		31	75		23	45	ns	
t_{THL}			65	135		25	75		18	45		
t_wCP	CP Minimum Pulse Width	125	50		60	21		48	14		ns	
t_wPL	PL Minimum Pulse Width	150	60		60	21		48	16		ns	
t_wMR	MR Minimum Pulse Width	150	60		60	30		48	20		ns	
t_{rec}	MR Recovery Time	175	75		70	30		56	20		ns	
t_{rec}	PL Recovery Time	150	62		60	24		48	17		ns	
t_s	Set-Up Time, UP/$\overline{DN}$ to CP	325	145		140	55		110	38		ns	
t_h	Hold Time, UP/$\overline{DN}$ to CP	0	-90		0	-35		0	-25			
t_s	Set-Up Time, $\overline{CE}$ to CP	275	118		120	49		96	33		ns	
t_h	Hold Time, $\overline{CE}$ to CP	0	-40		0	-15		0	-10			
t_s	Set-Up Time, P_n to PL	70	29		30	11		24	8		ns	
t_h	Hold Time, P_n to PL	0	-40		0	-20		0	-20			
f_{MAX}	Input Clock Frequency (Note 3)	2	5		5	12		6	15		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at $V_{DD} = 5$ V, 4 µs at $V_{DD} = 10$ V, and 3 µs at $V_{DD} = 15$ V.

SWITCHING WAVEFORMS



MINIMUM CP WIDTH, SET-UP AND HOLD TIMES, $\overline{CE}$ TO CP AND UP/$\overline{DN}$ TO CP



MINIMUM PL AND MR PULSE WIDTH, RECOVERY TIME FOR PL AND MR, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

4511B

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

GENERAL DESCRIPTION – The 4511B is a BCD to 7-Segment Latch/Decoder/Driver with four Address Inputs (A_0-A_3), an active LOW Latch Enable Input ($\overline{EL}$), an active Low Blanking Input ($\overline{I_B}$), an active LOW Lamp Test Input ($\overline{I_{LT}}$) and seven active HIGH npn bipolar segment outputs (a-g).

When the Latch Enable Input ($\overline{EL}$) is LOW, the state of the Segment Outputs (a-g) is determined by the data on the Address Inputs (A_0-A_3). When the Latch Enable Input ($\overline{EL}$) goes HIGH, the last data present at the Address Inputs (A_0-A_3) is stored in the latches and the Segment Outputs (a-g) remain stable.

When the Lamp Test Input ($\overline{I_{LT}}$) is LOW, all the Segment Outputs (a-g) are HIGH independent of all other input conditions. With the Lamp Test Input ($\overline{I_{LT}}$) HIGH, a LOW on the Blanking Input ($\overline{I_B}$) forces all Outputs (a-g) LOW. The Lamp Test Input ($\overline{I_{LT}}$) and the Blanking Input ($\overline{I_B}$) do not affect the latch circuit.

- **HIGH CURRENT SOURCING OUTPUTS (UP TO 25 mA)**
- **BLANKING INPUT (ACTIVE LOW)**
- **LAMP TEST INPUT (ACTIVE LOW)**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **MULTIPLEXING CAPABILITY**
- **LOW POWER DISSIPATION**

PIN NAMES

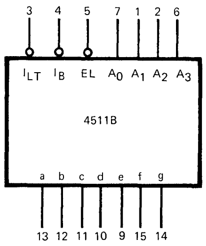
A_0- A_3	Address (Data) Inputs
$\overline{EL}$	Latch Enable (Active LOW) Input
$\overline{I_B}$	Blanking (Active LOW) Input
$\overline{I_{LT}}$	Lamp Test (Active LOW) Input
a-g	Segment Outputs

TRUTH TABLE

INPUTS							OUTPUTS							
$\overline{EL}$	$\overline{I_B}$	$\overline{I_{LT}}$	A_3	A_2	A_1	A_0	a	b	c	d	e	f	g	DISPLAY
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	L	H	H	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	H	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	H	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X				●				●

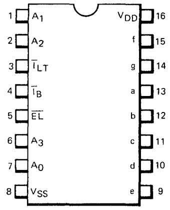
H = HIGH Level
L = LOW Level
X = Don't Care
● = Depends upon the BCD code applied during the LOW-to-HIGH transition of $\overline{EL}$

LOGIC SYMBOL



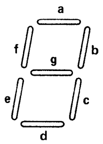
V_{DD} = Pin 16
V_{SS} = Pin 8

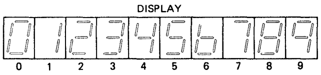
CONNECTION DIAGRAM DIP (TOP VIEW)



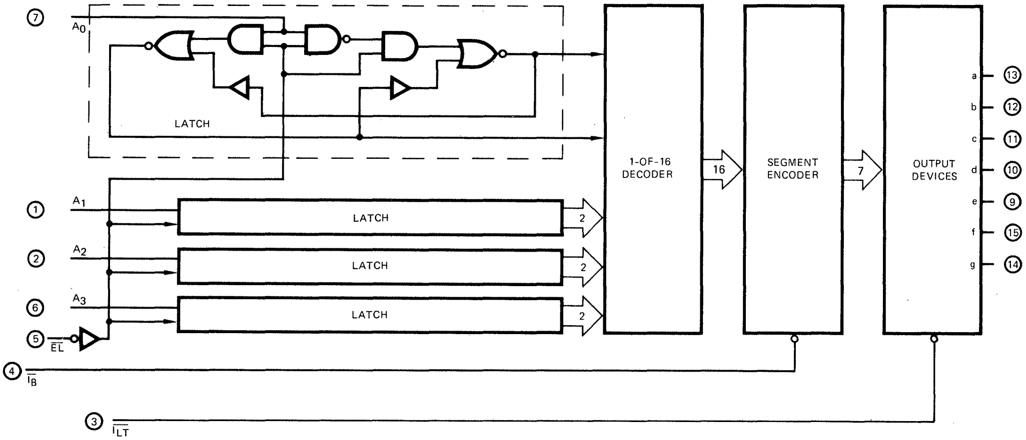
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Packages.

NUMERICAL DESIGNATIONS





BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8
○ = PIN NUMBER

DC CHARACTERISTICS: V_{DD} = 5 V, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		3.5			V	All	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				1.5	V	All	Guaranteed Input LOW Voltage	
V_{OH}	Output HIGH Voltage	XC or XM	4.1	4.57		V	25°C	I_{OH}<1 µA	Inputs at 0 V or V_{DD} per the Truth Table
		XC		4.24		V	25°C	I_{OH}=5 mA	
			3.60	4.22				I_{OH}=10 mA	
				4.16				I_{OH}=15 mA	
			.2.80	4.12				I_{OH}=20 mA	
				4.05				I_{OH}=25 mA	
		XM		4.24		V	25°C	I_{OH}=5 mA	
			3.90	4.22				I_{OH}=10 mA	
				4.16				I_{OH}=15 mA	
			3.40	4.12				I_{OH}=20 mA	
				4.05				I_{OH}=25 mA	
V_{OL}	Output LOW Voltage				0.05		MIN, 25°C	I_{OL} < 1 µA, Inputs at 0 V or V_{DD} per the Truth Table	
					0.05	V	MAX		
					0.5	V	All	I_{OL} < 1 µA, Inputs at 1.5 or 3.5 V	
I_{OL}	Output LOW Current		1				MIN	V_{OUT} = 0.4 V	Inputs at 0 V or V_{DD} per the Truth Table
			0.8			mA	25°C		
			0.4				MAX		
I_{DD}	Quiescent Power Supply Current	XC			20	µA	MIN, 25°C	All Inputs at 0 V or V_{DD} and all Outputs Open	
					150		MAX		
		XM			5		MIN, 25°C		
					150		MAX		

DC CHARACTERISTICS: $V_{DD} = 10\ V$, $V_{SS} = 0\ V$ (Note 1)

SYMBOL	PARAMETER		LIMITS			UNITS	TEMP	TEST CONDITIONS	
			MIN	TYP	MAX				
V_{IH}	Input HIGH Voltage		7			V	All	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				3	V	All	Guaranteed Input LOW Voltage	
V_{OH}	Output HIGH Voltage	XC or XM	9.1	9.58		V	25° C	$I_{OH} < 1\ \mu A$	Inputs at 0 V or V_{DD} per the Truth Table
		XC		9.26		V	25° C	$I_{OH} = 5\ mA$	
			8.75	9.21				$I_{OH} = 10\ mA$	
				9.17				$I_{OH} = 15\ mA$	
			8.10	9.14				$I_{OH} = 20\ mA$	
				9.10				$I_{OH} = 25\ mA$	
		XM		9.26		V	25° C	$I_{OH} = 5\ mA$	
			9.00	9.21				$I_{OH} = 10\ mA$	
				9.17				$I_{OH} = 15\ mA$	
			8.60	9.14				$I_{OH} = 20\ mA$	
				9.10				$I_{OH} = 25\ mA$	
V_{OL}	Output LOW Voltage				0.05	V	MIN, 25° C	$I_{OL} < 1\ \mu A$, Inputs at 0 V or V_{DD} per the Truth Table	
					0.05		MAX		
					1	V	All	$I_{OL} < 1\ \mu A$, Inputs at 3 or 7 V	
I_{OL}	Output LOW Current		2.6			mA	MIN	$V_{OUT} = 0.5\ V$	Inputs at 0 V or V_{DD} per the Truth Table
			2				25° C		
			1.2				MAX		
I_{DD}	Quiescent Power Supply Current	XC			40	µA	MIN, 25° C	All Inputs at 0 V or V_{DD} and all Outputs Open	
					300		MAX		
		XM			10		MIN, 25° C		
					300		MAX		

DC CHARACTERISTICS: $V_{DD} = 15$ V, $V_{SS} = 0$ V (Note 1)

SYMBOL	PARAMETER		LIMITS			UNITS	TEMP	TEST CONDITIONS	
			MIN	TYP	MAX				
V_{IH}	Input HIGH Voltage		11			V	All	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				4	V	All	Guaranteed Input LOW Voltage	
V_{OH}	Output HIGH Voltage	XC or XM	14.10	14.59		V	25°C	$I_{OH} < 1$ µA	Inputs at 0 V or V_{DD} per the Truth Table
		XC		14.27			25°C	I_{OH}=5 mA	
			13.75	14.23				I_{OH}=10 mA	
				14.20				I_{OH}=15 mA	
			13.10	14.17				I_{OH}=20 mA	
				14.13				I_{OH}=25 mA	
		XM		14.27			25°C	I_{OH}=5 mA	
			14.00	14.23				I_{OH}=10 mA	
				14.20				I_{OH}=15 mA	
			13.60	14.17				I_{OH}=20 mA	
				14.13				I_{OH}=25 mA	
V_{OL}	Output LOW Voltage				0.05	V	MIN, 25°C	$I_{OL} < 1$ µA, Inputs at 0 V or V_{DD} per the Logic Function or Truth Table	
					0.05		MAX		
					2	V	All	$I_{OL} < 1$ µA, Inputs at 4 or 11 V	
I_{IN}	Input Current	XC			1	µA	All	Lead under test at 0 V or V_{DD} All other Inputs simultaneously at 0 V or V_{DD}	
		XM			1				
I_{OL}	Output LOW Current		7.5			mA	MIN, 25°C	V_{OUT} = 1.5 V	Inputs at 0 V or V_{DD} per the Truth Table
			4.5				MAX		
I_{DD}	Quiescent Power Supply Current	XC			80	µA	MIN, 25°C	All Inputs at 0 V or V_{DD} and all Outputs Open	
					600		MAX		
		XM			20		MIN, 25°C		
					600		MAX		

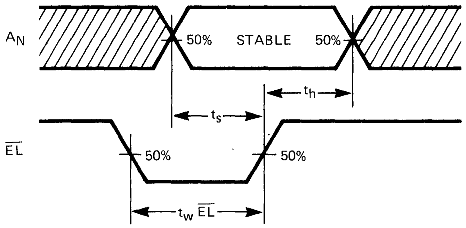
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25°C$ (see Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, A_N to a-g		212	480		90	190		68	152	ns	$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ≤20 ns
t_{PHL}			238	480		88	190		60	152	ns	
t_{PLH}	Propagation Delay, $\overline{I_{LT}}$ to a-g		82	180		38	80		30	64	ns	
t_{PHL}			85	180		34	80		24	64	ns	
t_{PLH}	Propagation Delay, $\overline{I_B}$ to a-g		147	330		60	135		42	108	ns	
t_{PHL}			164	330		65	135		46	108	ns	
t_{PLH}	Propagation Delay, $\overline{E_L}$ to a-g		230	550		90	210		63	168	ns	
t_{PHL}			275	550		98	210		66	168	ns	
t_{TLH}	Output Transition		25	55		18	40		16	40	ns	
t_{THL}	Time		75	135		26	75		17	45	ns	
$t_W\overline{EL}$	$\overline{EL}$ Minimum Pulse Width	85	34		35	14		28	10		ns	
t_s	Set-Up Time, A_N to $\overline{EL}$	55	20		25	7		20	4		ns	
t_h	Hold-Time, A_N to $\overline{EL}$	55	19		25	6		20	4		ns	

NOTES:
1. Additional dc characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

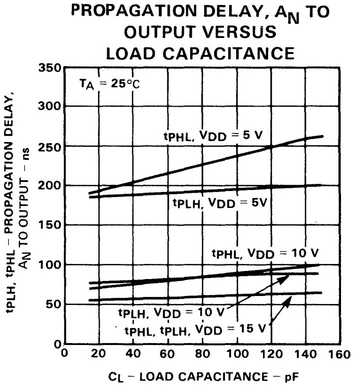
AC WAVEFORMS

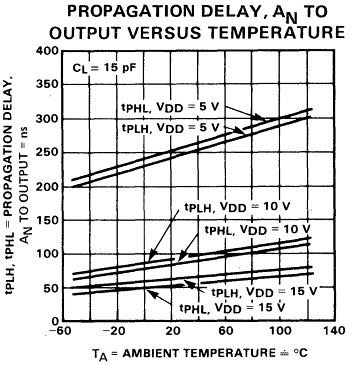
SET-UP AND HOLD-TIMES, A_N TO $\overline{EL}$ AND MINIMUM $\overline{EL}$ PULSE WIDTH

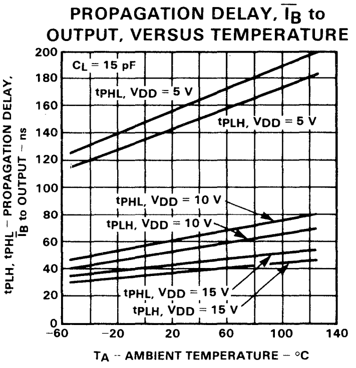


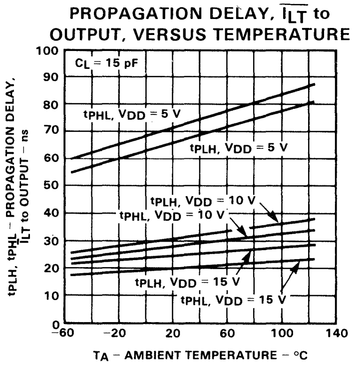
NOTE: Set-up and hold-times are shown as positive values but may be specified as negative values

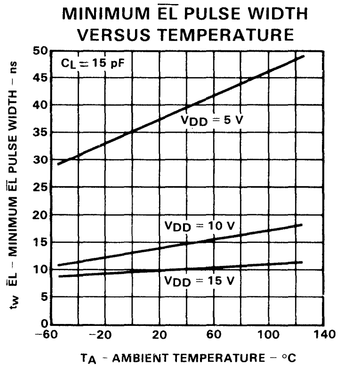
TYPICAL ELECTRICAL CHARACTERISTICS

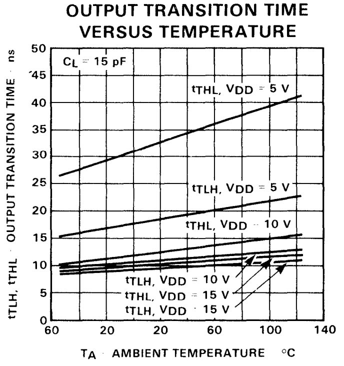

PROPAGATION DELAY, A_N TO OUTPUT VERSUS LOAD CAPACITANCE

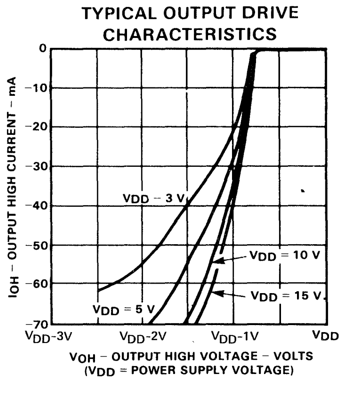

PROPAGATION DELAY, A_N TO OUTPUT VERSUS TEMPERATURE


PROPAGATION DELAY, $\overline{I_B}$ to OUTPUT, VERSUS TEMPERATURE


PROPAGATION DELAY, $\overline{I_{LT}}$ to OUTPUT, VERSUS TEMPERATURE

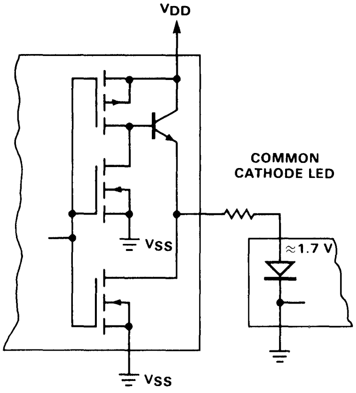

MINIMUM $\overline{EL}$ PULSE WIDTH VERSUS TEMPERATURE

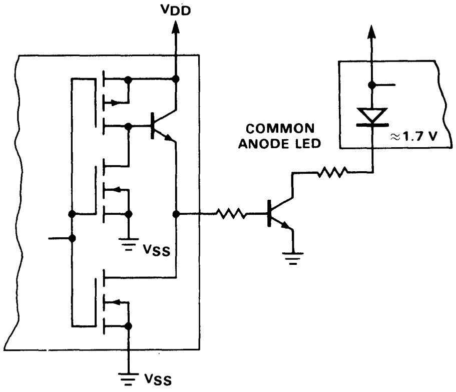

OUTPUT TRANSITION TIME VERSUS TEMPERATURE


TYPICAL OUTPUT DRIVE CHARACTERISTICS

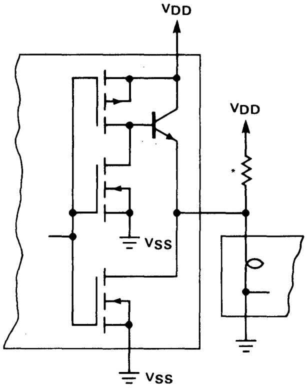
TYPICAL APPLICATIONS

LIGHT EMITTING DIODE (LED) READOUT



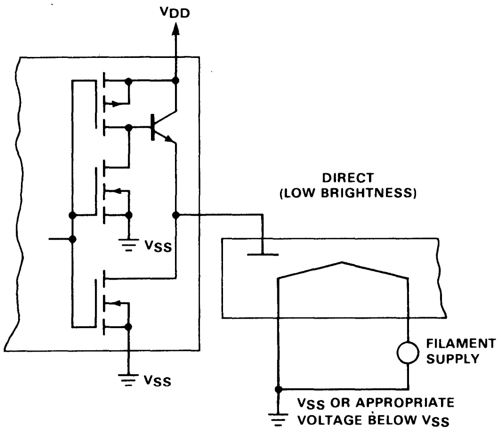


INCANDESCENT READOUT

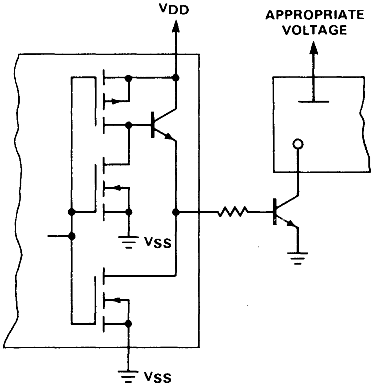


*A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

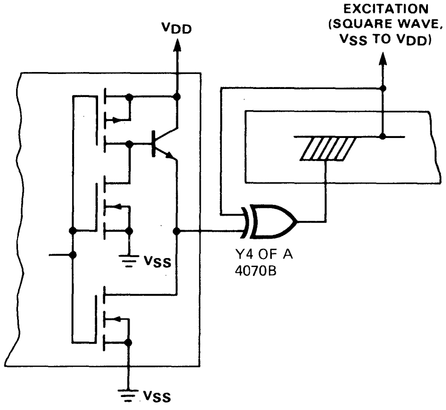
FLUORESCENT READOUT



GAS DISCHARGE READOUT



LIQUID CRYSTAL (LCD) READOUT**



**Direct dc drive of LCD not recommended for life of LCD readouts.

4512B

8-INPUT MULTIPLEXER WITH 3-STATE OUTPUT

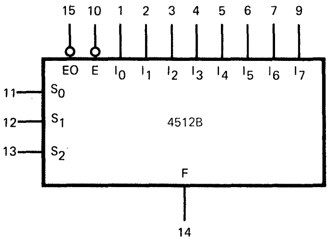
DESCRIPTION – The 4512B is an 8-Input Multiplexer with Active LOW logic and output enables ($\overline{E}$, $\overline{EO}$). One of eight binary inputs is selected by Select Inputs S_0, S_1 and S_2 and is routed to the output F. A HIGH on the Output Enable ($\overline{EO}$) causes the F output to assume a high impedance or "OFF" state, regardless of other input conditions. This allows the output to interface directly with bus oriented systems (3-state). When the active LOW Enable ($\overline{E}$) is HIGH, it forces the output LOW provided the Output Enable ($\overline{EO}$) is LOW. By proper manipulation of the inputs, the 4512B can provide any logic functions of four variables. The 4512B cannot be used to multiplex analog signals.

- **SELECTS ONE-OF-EIGHT DATA SOURCES**
- **PERFORMS PARALLEL-TO-SERIAL CONVERSION**
- **3-STATE OUTPUTS WITH ACTIVE LOW OUTPUT ENABLE**
- **ACTIVE LOW LOGIC ENABLE**

PIN NAMES

S_0, S_1, S_2	Select Inputs
$\overline{EO}$	Output Enable (Active LOW)
$\overline{E}$	Enable (Active LOW)
I_0 to I_7	Multiplexer Inputs
F	Multiplexer Output

LOGIC SYMBOL



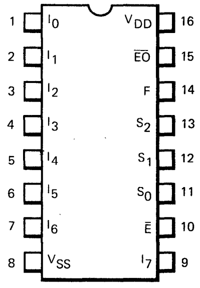
V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUTS													OUTPUT
$\overline{EO}$	$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	F
L	H	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	L	H	X	X	X	X	X	X	X	H
L	L	L	L	H	X	L	X	X	X	X	X	X	L
L	L	L	L	H	X	H	X	X	X	X	X	X	H
L	L	L	H	L	X	X	L	X	X	X	X	X	L
L	L	L	H	L	X	X	H	X	X	X	X	X	H
L	L	L	H	H	X	X	X	L	X	X	X	X	L
L	L	L	H	H	X	X	X	H	X	X	X	X	H
L	L	H	L	L	X	X	X	X	L	X	X	X	L
L	L	H	L	L	X	X	X	X	H	X	X	X	H
L	L	H	L	H	X	X	X	X	X	L	X	X	L
L	L	H	L	H	X	X	X	X	X	H	X	X	H
L	L	H	H	L	X	X	X	X	X	X	L	X	L
L	L	H	H	L	X	X	X	X	X	X	H	X	H
L	L	H	H	H	X	X	X	X	X	X	X	L	L
L	L	H	H	H	X	X	X	X	X	X	X	H	H
H	X	X	X	X	X	X	X	X	X	X	X	X	Z

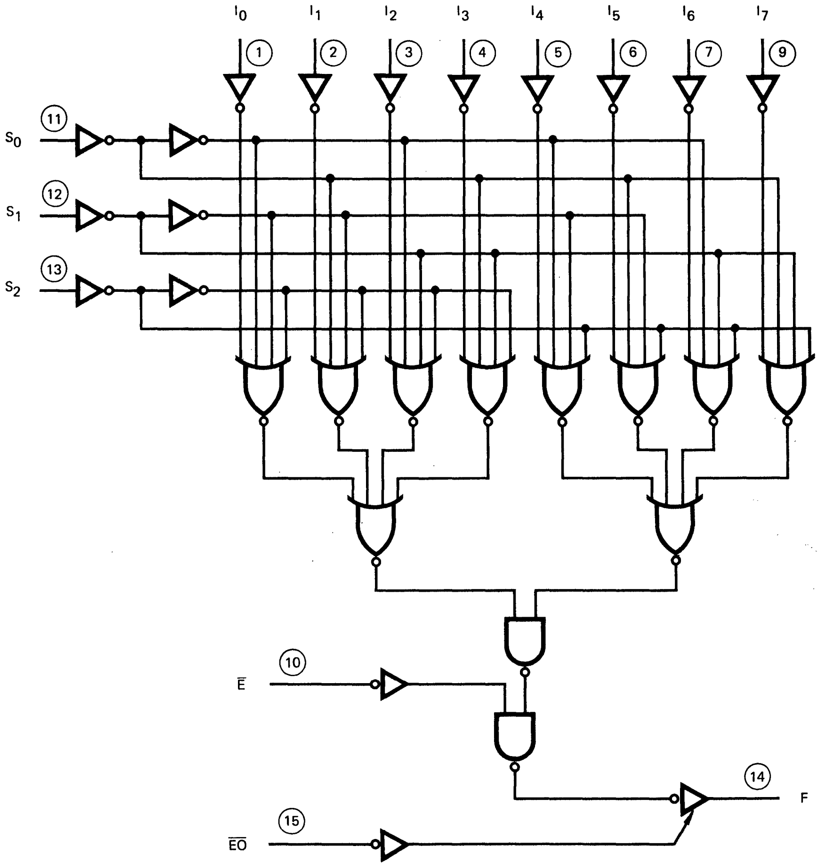
L = LOW Level
H = HIGH Level
X = Don't Care
Z = High Impedance State

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDTIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC									1.6 12	µA	MIN, 25°C MAX	Output returned to V_{DD}, $\overline{EO}$ = V_{DD}
		XM									0.4 12		MIN, 25°C MAX	
I_{OZL}	Output OFF Current LOW	XC									– 1.6 –12	µA	MIN, 25°C MAX	Output returned to V_{SS}, $\overline{EO}$ = V_{DD}
		XM									– 0.4 –12		MIN, 25°C MAX	
I_{DD}	Quiescent Power Supply Current	XC			20 150			40 300			80 600	µA	MIN, 25°C MAX	All inputs at 0 V or V_{DD}
		XM			5 150			10 300			20 600	µA	MIN, 25°C MAX	

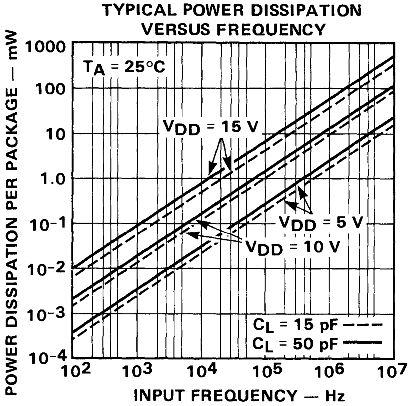
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

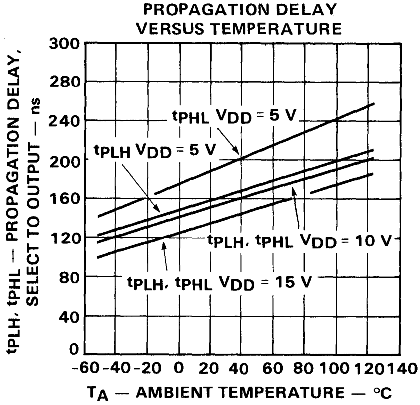
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		150	300		75	150		52	120	ns	C_L = 50 pF,
t_{PHL}	Data to Output		150	300		75	150		52	120	ns	R_L = 200 kΩ
t_{PLH}	Propagation Delay,		175	350		85	170		60	136	ns	Input Transition
t_{PHL}	Select to Output		175	350		85	170		65	136	ns	Times ≤ 20 ns
t_{PLH}	Propagation Delay,		90	175		45	90		30	72	ns	
t_{PHL}	$\overline{E}$ to Output		90	175		45	90		32	72	ns	
t_{PZH}	Output Enable		33	85		20	45		18	36	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}	Time		30	85		22	45		20	36	ns	(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable		39	100		20	50		15	40	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}	Time		40	100		20	50		15	40	ns	(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition		90	200		40	100		33	65	ns	
t_{THL}	Time		100	200		40	100		30	65	ns	

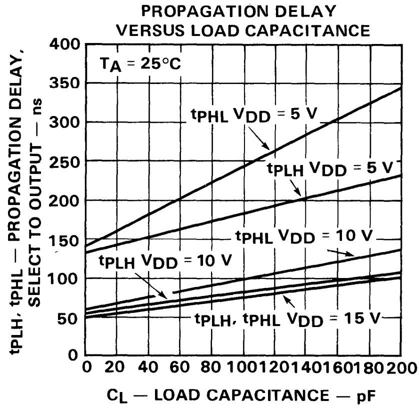
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characterisitcs.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

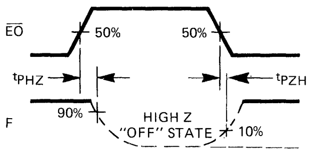
TYPICAL ELECTRICAL CHARACTERISTICS


TYPICAL POWER DISSIPATION VERSUS FREQUENCY

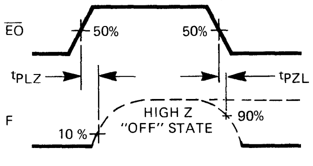

PROPAGATION DELAY VERSUS TEMPERATURE


PROPAGATION DELAY VERSUS LOAD CAPACITANCE

SWITCHING WAVEFORMS



OUTPUT ENABLE TIME
(tPZH) AND OUTPUT DISABLE TIME (tPHZ)



OUTPUT ENABLE TIME
(tPZL) AND OUTPUT DISABLE TIME (tPLZ)

APPLICATIONS

MULTIPLEXER AS A FUNCTION GENERATOR – In most digital systems there are areas, usually in the control section, where a number of inputs generate an output in a highly irregular way. In other words, an unusual function must be generated which is apparently not available as an MSI building block. In such cases, many designers tend to return to classical methods of logic design with NAND and NOR gates using Boolean Algebra, Karnaugh maps and Veitch diagrams for logic minimization. Surprisingly enough, multiplexers can simplify these designs.

The 4512B 8-Input multiplexer can generate any one of the 65,536 different functions of four variables. An example will illustrate the technique. Assume four binary inputs are A, B, C and D and F is the desired function (See Fig. 1). If C is connected to S_0, B to S_1 and A to S_2, any combination of A, B and C will select an input (assuming the output is enabled). For each combination of A, B and C, the required output, as a function of the fourth variable D, is either H or L the same as D or the opposite of D. Therefore, the truth table may be examined and each input of the 4512B is connected to V_{DD} V_{SS}, D or $\overline{D}$ as required and in such fashion the function is generated.

In the example shown, (Fig. 1) the first two outputs are the opposite of D, so I_0 is connected to D. The second two are HIGH, so I_1 is connected to V_{DD}, etc.

32-INPUT MULTIPLEXER – The 3-State Output Enable can be used to expand the 4512B. A 32-Input Multiplexer utilizing four 4512B's and a 4011B is shown in Fig. 2.

INPUT VARIABLES				REQUIRED FUNCTION
A	B	C	D	F
L	L	L	L	H
L	L	L	H	L
L	L	H	L	H
L	L	H	H	H
L	H	L	L	L
L	H	L	H	H
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
•	•	•	•	•
•	•	•	•	•
		•	•	•

H = HIGH Level
L = LOW Level

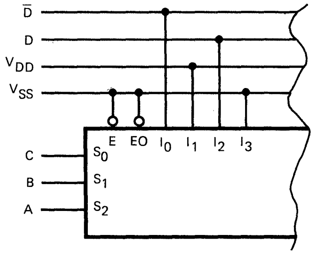
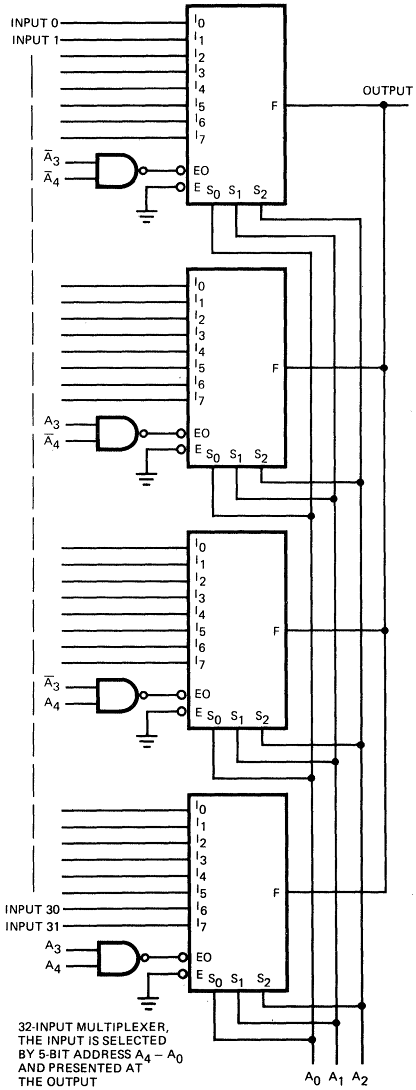


Fig. 1



32-INPUT MULTIPLEXER,
THE INPUT IS SELECTED
BY 5-BIT ADDRESS $A_4 - A_0$
AND PRESENTED AT
THE OUTPUT

Fig. 2

4514B

1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCH

DESCRIPTION – The 4514B is a 1-of-16 Decoder/Demultiplexer with four binary weighted Address Inputs (A_0-A_3), a Latch Enable Input (EL), an active LOW Enable Input ($\overline{E}$) and sixteen mutually exclusive active HIGH Outputs (O_0-O_{15}).

When the Latch Enable Input (EL) is HIGH, the selected Output (O_0-O_{15}) is determined by the data on the Address Inputs (A_0-A_3). When the Latch Enable Input (EL) goes LOW, the last data present at the Address inputs (A_0-A_3) is stored in the latches and the Outputs (O_0-O_{15}) remain stable. When the Enable Input ($\overline{E}$) is LOW, the selected Output (O_0-O_{15}), determined by the contents of the latch, is HIGH. When the Enable Input ($\overline{E}$) is HIGH, all Outputs (O_0-O_{15}) are LOW. The Enable Input ($\overline{E}$) does not affect the state of the latch.

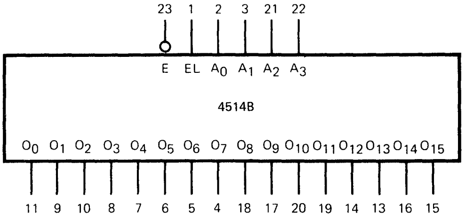
With the Latch Enable Input (EL) HIGH, 16-channel demultiplexing results when data is applied to the Enable Input ($\overline{E}$) and the desired output is selected by A_0-A_3. The selected output (O_0-O_{15}) will follow as the inverse of the data. All unselected outputs (O_0-O_{15}) are LOW.

- **LATCH ENABLE INPUT (ACTIVE HIGH)**
- **ENABLE INPUT (ACTIVE LOW)**
- **SELECTED BUFFERED OUTPUTS (ACTIVE HIGH) COMPLEMENT OF THE INPUT**

PIN NAMES

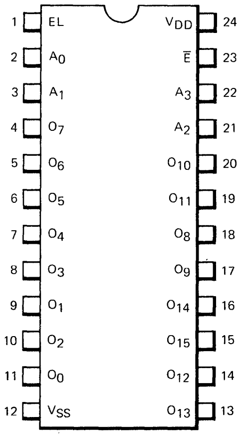
A_0-A_3	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
EL	Latch Enable Input
O_0-O_{15}	Outputs

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



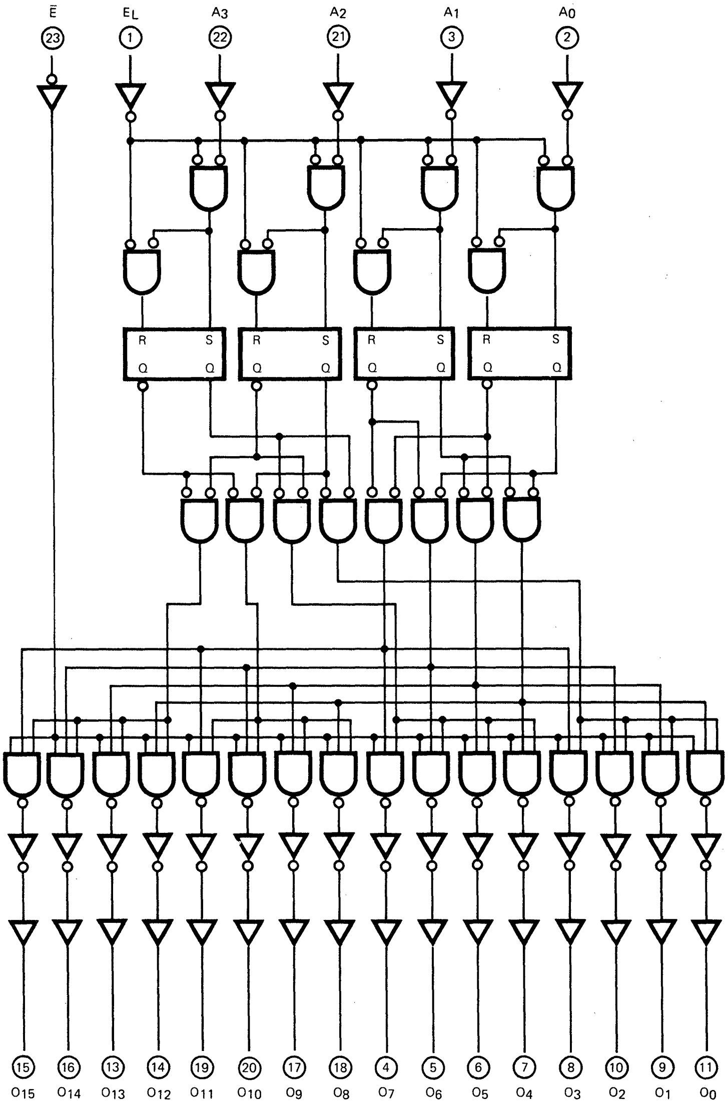
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

INPUTS					OUTPUTS															
$\overline{E}$	A_0	A_1	A_2	A_3	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}	O_{11}	O_{12}	O_{13}	O_{14}	O_{15}
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

H = HIGH Level
L = LOW Level
EL = HIGH

LOGIC DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

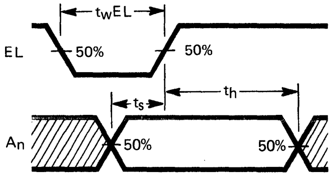
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, A_n to O_n		260			95			65		ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			260			95			65			
t_{PLH}	Propagation Delay, EL to O_n		260			95			65		ns	
t_{PHL}			260			95			65			
t_{PLH}	Propagation Delay, $\overline{E}$ to O_n		200			70			50		ns	
t_{PHL}			200			70			50			
t_{TLH}	Output Transition Time		135			75			45		ns	
t_{THL}			135			75			45			
t_s	Set-Up Time, A_n to EL		60			20			15		ns	
t_h	Hold Time, A_n to EL		60			20			15			
t_wEL	Minimum EL Pulse Width		60			20			15		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

SWITCHING WAVEFORMS



MINIMUM EL PULSE WIDTH AND SET-UP AND HOLD TIMES, A_n TO EL

NOTE:
Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

4515B

1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCH

DESCRIPTION – The 4515B is a 1-of-16 Decoder/Demultiplexer with four binary weighted Address Inputs (A_0–A_3), a Latch Enable Input (EL), an active LOW Enable Input ($\overline{E}$) and sixteen mutually exclusive active LOW Outputs ($\overline{O_0}$–$\overline{O_{15}}$).

When the Latch Enable Input (EL) is HIGH, the selected Output ($\overline{O_0}$–$\overline{O_{15}}$) is determined by the data on the Address Inputs (A_0–A_3). When the Latch Enable Input (EL) goes LOW, the last data present at the Address Inputs (A_0–A_3) is stored in the latches and the Outputs ($\overline{O_0}$–$\overline{O_{15}}$) remain stable. When the Enable Input ($\overline{E}$) is LOW, the selected Output ($\overline{O_0}$–$\overline{O_{15}}$), determined by the contents of the latch, is LOW. When the Enable Input ($\overline{E}$) is HIGH, all Outputs ($\overline{O_0}$–$\overline{O_{15}}$) are HIGH. The Enable Input ($\overline{E}$) does not affect the state of the latch.

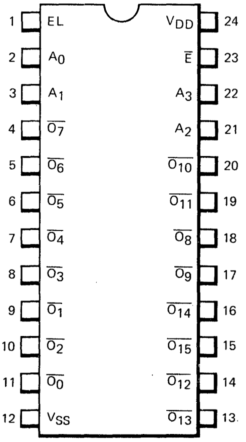
With the Latch Enable Input (EL) HIGH, 16-channel demultiplexing results when data is applied to the Enable Input ($\overline{E}$) and the desired output is selected by A_0–A_3. The selected Output ($\overline{O_0}$–$\overline{O_{15}}$) will follow the data at the Enable Input ($\overline{E}$). All unselected outputs ($\overline{O_0}$–$\overline{O_{15}}$) are HIGH.

- **LATCH ENABLE INPUT (ACTIVE HIGH)**
- **ENABLE INPUT (ACTIVE LOW)**
- **BUFFERED OUTPUTS (ACTIVE LOW)**

PIN NAMES

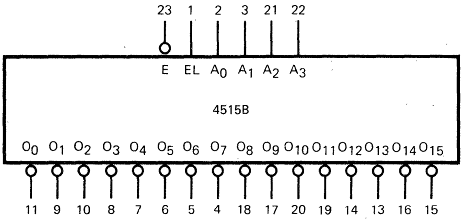
A_0–A_3	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
EL	Latch Enable Input
$\overline{O_0}$–$\overline{O_{15}}$	Outputs (Active LOW)

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC SYMBOL



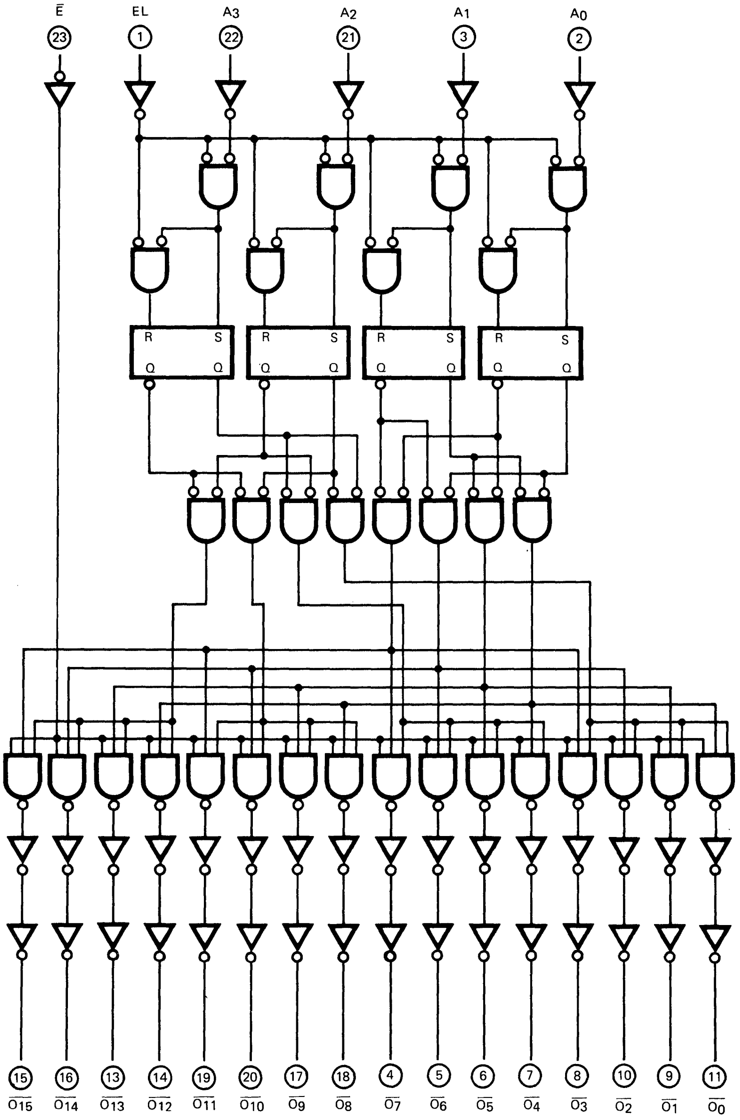
V_{DD} = Pin 24
V_{SS} = Pin 12

TRUTH TABLE

INPUTS					OUTPUTS															
$\overline{E}$	A_0	A_1	A_2	A_3	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$	$\overline{O_4}$	$\overline{O_5}$	$\overline{O_6}$	$\overline{O_7}$	$\overline{O_8}$	$\overline{O_9}$	$\overline{O_{10}}$	$\overline{O_{11}}$	$\overline{O_{12}}$	$\overline{O_{13}}$	$\overline{O_{14}}$	$\overline{O_{15}}$
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Level
L = LOW Level
EL = HIGH

LOGIC DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

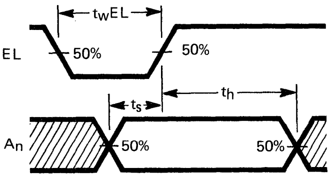
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, A_n to $\overline{O}_n$		260 260			95 95			65 65		ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, EL to $\overline{O}_n$		260 260			95 95			65 65		ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}$ to $\overline{O}_n$		200 200			70 70			50 50		ns	
t_{TLH} t_{THL}	Output Transition Time		135 135			75 75			45 45		ns	
t_s t_h	Set-Up Time, A_n to EL Hold Time, A_n to EL		60 60			20 20			15 15		ns	
t_wEL	Minimum EL Pulse Width		60			20			15		ns	

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

SWITCHING WAVEFORMS



MINIMUM EL PULSE WIDTH AND SET-UP AND HOLD TIMES, A_n TO EL

NOTE:
Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

4516B

UP/DOWN COUNTER

DESCRIPTION — The 4516B is an edge-triggered synchronous Up/Down 4-Bit Binary Counter with a Clock Input (CP), an active HIGH Count Up/Down Control Input (Up/$\overline{Dn}$), an active LOW count Enable Input ($\overline{CE}$), an asynchronous active HIGH Parallel Load Input (PL), four Parallel Inputs (P_0-P_3), four parallel Outputs (Q_0-Q_3), an active LOW Terminal Count Output ($\overline{TC}$) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except the Master Reset Input (MR) which must be LOW. When the Parallel Load Input (PL) and the Count Enable Input ($\overline{CE}$) are LOW, the counter changes on the LOW-to-HIGH transition of the Clock Input (CP). The Count Up/Down Control Input (Up/$\overline{Dn}$) determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, the Terminal Count Output ($\overline{TC}$) is LOW when $Q_0 = Q_1 = Q_2 = Q_3 =$ HIGH and $\overline{CE}$ = LOW. When counting down the Terminal Count Output ($\overline{TC}$) is LOW when $Q_0 = Q_1 = Q_2 = Q_3 =$ LOW and the $\overline{CE}$ = LOW. A HIGH on the Master Reset Input (MR) resets the counter ($Q_0 = Q_1 = Q_2 = Q_3 =$ LOW) independent of all other input conditions.

- **UP/DOWN COUNT CONTROL**
- **SINGLE CLOCK INPUT (L→H EDGE-TRIGGERED)**
- **ASYNCHRONOUS PARALLEL LOAD INPUT**
- **ASYNCHRONOUS MASTER RESET**

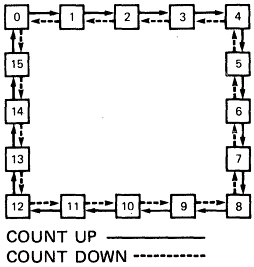
MODE SELECTION TABLE

PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
H	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	H	X	No Change
L	L	L	⎍	Count Down, Binary
L	H	L	⎍	Count Up, Binary

MR = LOW
H = HIGH Level
L = LOW Level

X = Don't Care
⎍ = Positive-Going Transition

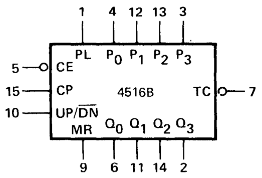
STATE DIAGRAM



LOGIC EQUATION FOR TERMINAL COUNT

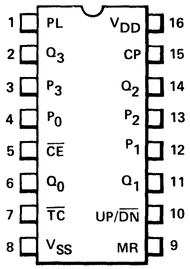
$$\overline{TC} = \overline{CE} \bullet [(UP/\overline{DN}) \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3] + [(UP/\overline{DN}) \bullet \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3]$$

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

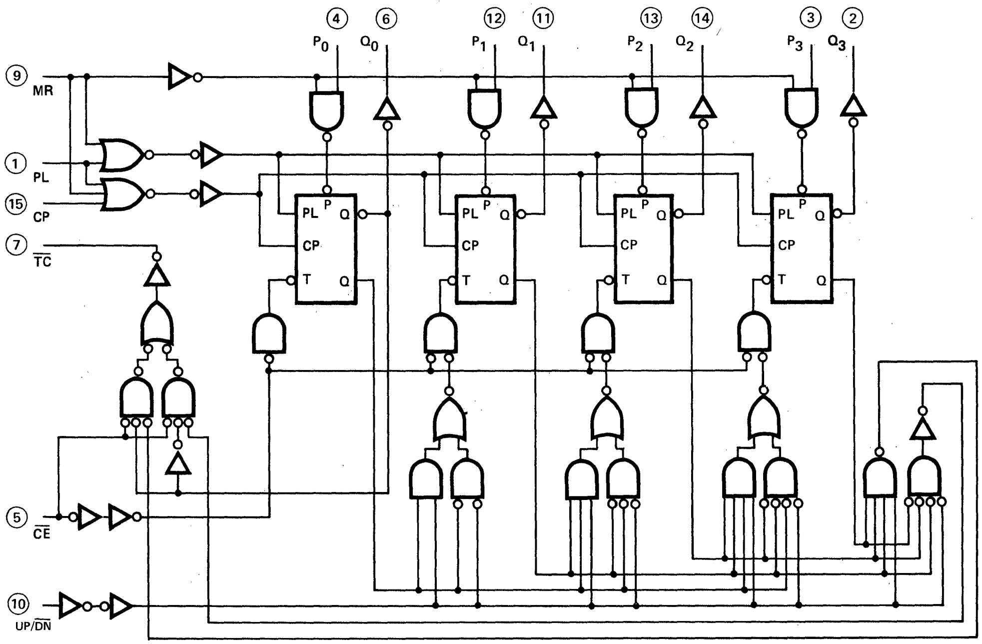


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package,

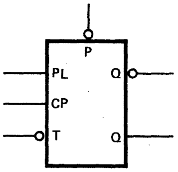
PIN NAMES

PL	Parallel Load Input (Active HIGH)
P_0-P_3	Parallel Inputs
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (L→H Edge-Triggered)
Up/$\overline{Dn}$	Up/Down Count Control Input
MR	Master Reset Input
$\overline{TC}$	Terminal Count Output (Active LOW)
Q_0-Q_3	Parallel Outputs

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number



PL (Parallel Load Input) — Asynchronously Loads P into Q, Overriding all Other Inputs
$\overline{P}$ (Parallel Input) — Data on this Pin is Asynchronously Loaded into Q, when PL is HIGH Overriding all Other Inputs
$\overline{T}$ (Toggle Input) — Forces the Q Output to Synchronously Toggle when a HIGH is placed on this Input
CP (Clock Pulse Input)
Q, $\overline{Q}$ (True and Complementary Outputs)

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

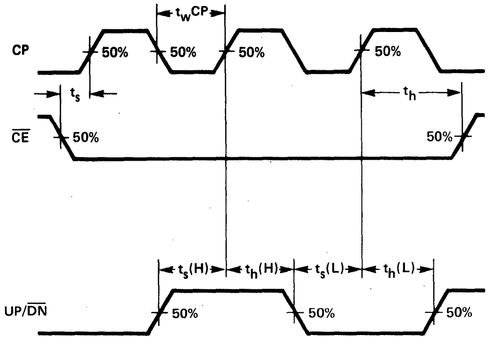
Notes on following page

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

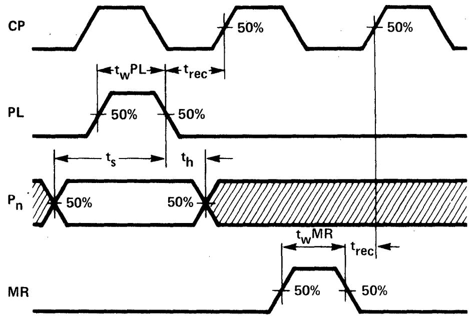
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		150	350		62	160		41	128	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			150	350		59	160		39	128		
t_{PLH}	Propagation Delay, CP to $\overline{TC}$		167	450		71	180		48	144	ns	
t_{PHL}			252	650		100	245		66	196		
t_{PLH}	Propagation Delay, PL to Q_n		170	325		70	150		45	120	ns	
t_{PHL}			220	425		90	195		62	156		
t_{PLH}	Propagation Delay, MR to Q_n, $\overline{TC}$		225	500		170	210		105	168	ns	
t_{PHL}			205	450		120	190		80	152		
t_{TLH}	Output Transition Time		60	135		31	75		23	45	ns	
t_{THL}			65	135		25	75		18	45		
t_WCP	CP Minimum Pulse Width	125	50		60	21		48	14		ns	
t_WPL	PL Minimum Pulse Width	150	60		60	21		48	16		ns	
t_WMR	MR Minimum Pulse Width	150	60		60	30		48	20		ns	
t_{rec}	MR Recovery Time	175	75		70	30		56	20		ns	
t_{rec}	PL Recovery Time	150	62		60	24		48	17		ns	
t_s	Set-Up Time, UP/$\overline{DN}$ to CP	325	145		140	55		110	38		ns	
t_h	Hold Time, UP/$\overline{DN}$ to CP	0	-90		0	-35		0	-25			
t_s	Set-Up Time, $\overline{CE}$ to CP	275	118		120	49		96	33		ns	
t_h	Hold Time, $\overline{CE}$ to CP	0	-40		0	-15		0	-10			
t_s	Set-Up Time, P_n to PL	70	29		30	11		24	8		ns	
t_h	Hold Time, P_n to PL	0	-40		0	-20		0	-20			
f_{MAX}	Input Clock Frequency (Note 3)	2	5		5	12		6	15		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



MINIMUM CP WIDTH, SET-UP AND HOLD TIMES, $\overline{CE}$ TO CP AND UP/$\overline{DN}$ TO CP



MINIMUM PL AND MR PULSE WIDTH, RECOVERY TIME FOR PL AND MR, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

4518B

DUAL 4-BIT DECADE COUNTER

DESCRIPTION – The 4518B is a Dual 4-Bit Internally Synchronous BCD Counter. Each counter has both an active HIGH Clock Input (CP_0) and an active LOW Clock Input ($\overline{CP}_1$), buffered Outputs from all four bit positions (Q_0-Q_3) and an active HIGH overriding asynchronous Master Reset Input (MR).

The counter advances on either the LOW-to-HIGH transition of the CP_0 Input if $\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of the $\overline{CP}_1$ Input if CP_0 is LOW (see the Truth Table). Either Clock Input (CP_0, $\overline{CP}_1$) may be used as the Clock Input to the counter and the other Clock Input may be used as a Clock Inhibit Input.

A HIGH on the Master Reset Input (MR) resets the counter (Q_0-Q_3 = LOW) independent of the Clock Inputs (CP_0, $\overline{CP}_1$).

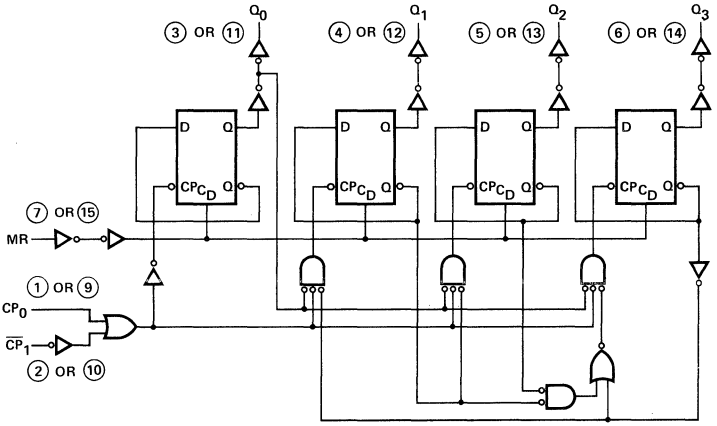
- **TYPICAL COUNT FREQUENCY OF 10 MHz AT V_{DD} = 10 V**
- **TRIGGERED ON EITHER A LOW-TO-HIGH OR A HIGH-TO-LOW TRANSITION**
- **ASYNCHRONOUS ACTIVE HIGH MASTER RESET**
- **BUFFERED OUTPUTS FROM ALL FOUR BIT POSITIONS**
- **FULLY SYNCHRONOUS COUNTING**

TRUTH TABLE

CP_0	$\overline{CP}_1$	MR	MODE
_/‾	H	L	Counter Advances
L	‾_	L	Counter Advances
‾_	X	L	No Change
X	_/‾	L	No Change
_/‾	L	L	No Change
H	‾_	L	No Change
X	X	H	Reset (Asynchronous)

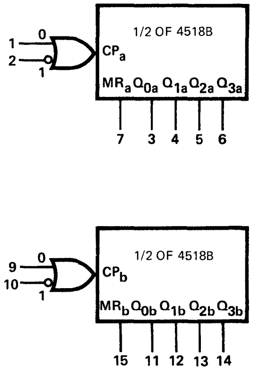
X = Don't Care
L = LOW Level
H = HIGH Level
_/‾ = Positive-Going Transition
‾_ = Negative-Going Transition

1/2 OF A 4518B LOGIC DIAGRAM



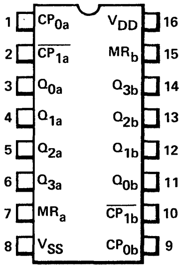
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

LOGIC SYMBOLS



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

CP_{0a}, CP_{0b}	Clock Input (L → H Triggered)
$\overline{CP}_{1a}$, $\overline{CP}_{1b}$	Clock Input (H → L Triggered)
MR_a, MR_b	Master Reset Inputs
Q_{0a}–Q_{3a}	Outputs
Q_{0b}–Q_{3b}	Outputs

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

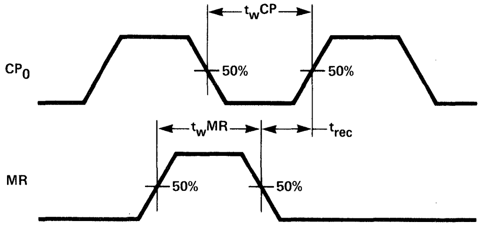
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, F_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PLH}	Propagation Delay, CP_0 or $\overline{CP_1}$ to Q_n		220 220	480 480		95 95	210 210		60 60	168 168	ns	CL = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}	Propagation Delay, MR to Q_n		220	480		90	210		60	168	ns	
t_{TLH} t_{THL}	Output Transition Time		65 65	135 135		35 35	70 70		25 25	45 45	ns	
t_wMR	MR Minimum Pulse Width	180	70		70	30		56	20		ns	
t_wCP	CP_0 or $\overline{CP_1}$ Minimum Pulse Width	275	120		120	50		96	35		ns	
t_{rec}	MR Recovery Time	40	15		25	5		20	0		ns	
t_s	Set-Up Time, CP_0 to $\overline{CP_1}$	275	130		125	57		100	40		ns	
t_s	Set-Up Time, $\overline{CP_1}$ to CP_0	275	130		125	57		100	40		ns	
f_{MAX}	Input Count Frequency (Note 3)	2	4		4	10		5	12		MHz	

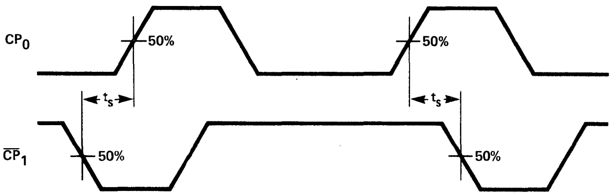
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTHS FOR CP_0, $\overline{CP_1}$ AND MR AND MR RECOVERY TIME

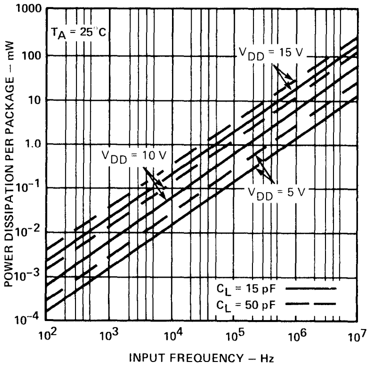
CONDITIONS: $\overline{CP_1}$ = HIGH and the device triggers on a LOW-to-HIGH transition at CP_0. The timing also applies when CP_0 = LOW and the device triggers on a HIGH-to-LOW transition at $\overline{CP_1}$.



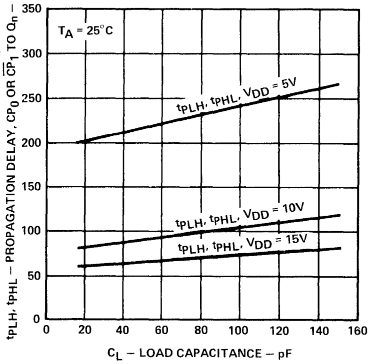
SET-UP TIMES, CP_0 TO $\overline{CP_1}$ AND $\overline{CP_1}$ TO CP_0

NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

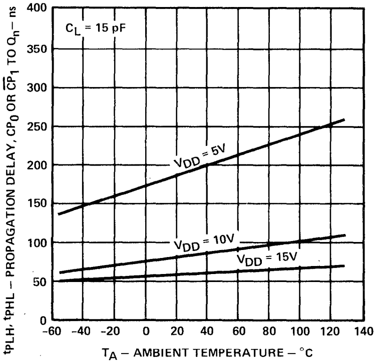
TYPICAL ELECTRICAL CHARACTERISTICS



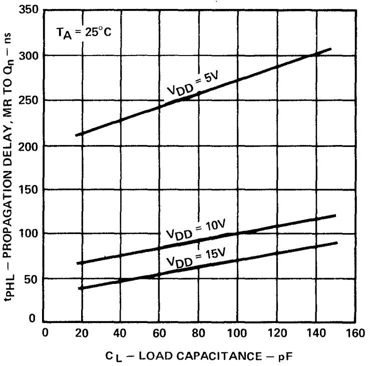
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY, CP0 OR $\overline{CP1}$ TO Q_n, VERSUS LOAD CAPACITANCE



PROPAGATION DELAY, CP0 OR $\overline{CP1}$ TO Q_n, VERSUS TEMPERATURE



PROPAGATION DELAY, MR TO Q_n, VERSUS LOAD CAPACITANCE

4520B

DUAL 4-BIT BINARY COUNTER

DESCRIPTION — The 4520B is a Dual 4-Bit Internally Synchronous Binary Counter. Each counter has both an active HIGH Clock Input (CP_0) and an active LOW Clock Input ($\overline{CP}_1$), buffered Outputs from all four bit positions (Q_0-Q_3) and an active HIGH overriding asynchronous Master Reset Input (MR).

The counter advances on either the LOW-to-HIGH transition of the CP_0 Input if $\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of the $\overline{CP}_1$ Input if CP_0 is LOW (see the Truth Table). Either Clock Input (CP_0, $\overline{CP}_1$) may be used as the Clock Input to the counter and the other Clock Input may be used as a Clock Inhibit Input.

A HIGH on the Master Reset Input (MR) resets the counter (Q_0-Q_3 = LOW) independent of the Clock Inputs (CP_0, $\overline{CP}_1$).

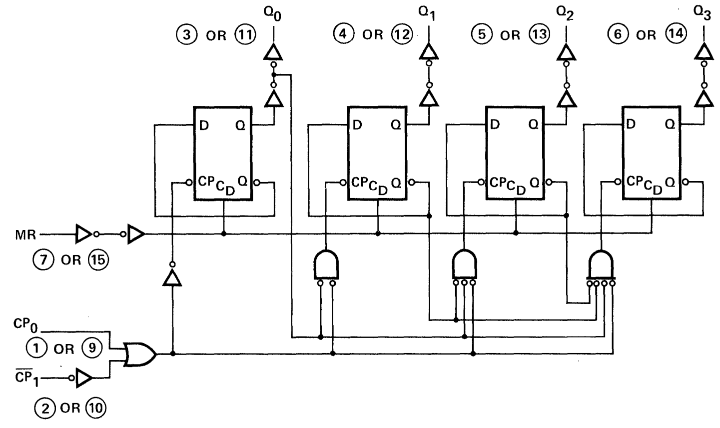
- TYPICAL COUNT FREQUENCY OF 10 MHz AT V_{DD} = 10 V
- TRIGGERED ON EITHER A LOW-TO-HIGH OR A HIGH-TO-LOW TRANSITION
- ASYNCHRONOUS ACTIVE HIGH MASTER RESET
- BUFFERED OUTPUTS FROM ALL FOUR BIT POSITIONS
- FULLY SYNCHRONOUS COUNTING

TRUTH TABLE

CP_0	$\overline{CP}_1$	MR	MODE
↑	H	L	Counter Advances
L	↓	L	Counter Advances
↓	X	L	No Change
X	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
X	X	H	Reset (Asynchronous)

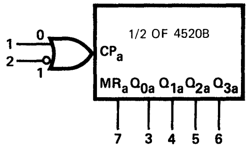
X = Don't Care
L = LOW Level
H = HIGH Level
↑ = Positive-Going Transition
↓ = Negative-Going Transition

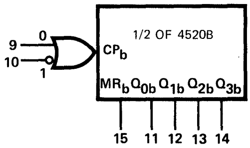
1/2 OF A 4520B LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

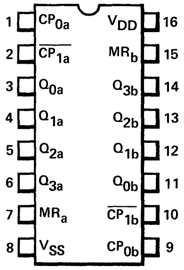
LOGIC SYMBOLS





V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

CP_{0a}, CP_{0b}	Clock Input (L → H Triggered)
$\overline{CP}_{1a}$, $\overline{CP}_{1b}$	Clock Input (H → L Triggered)
MR_a, MR_b	Master Reset Inputs
Q_{0a}–Q_{3a}	Outputs
Q_{0b}–Q_{3b}	Outputs

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

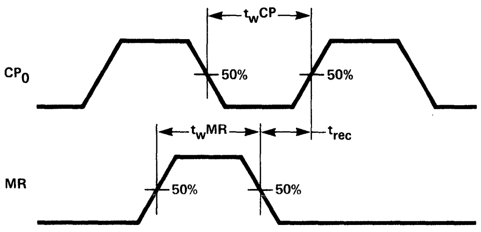
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP_0 or $\overline{CP}_1$ to Q_n		220 220	480 480		95 95	210 210		60 60	168 168	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}	Propagation Delay, MR to Q_n		220	480		90	210		60	168	ns	
t_{RLH} t_{THL}	Output Transition Time		65 65	135 135		35 35	70 70		25 25	45 45	ns	
t_wMR	MR Minimum Pulse Width	180	70		70	30		56	20		ns	
t_wCP	CP_0 or $\overline{CP_1}$ Minimum Pulse Width	275	120		120	50		96	35		ns	
t_{rec}	MR Recovery Time	40	15		25	5		20	0		ns	
t_s	Set-Up Time, CP_0 to $\overline{CP_1}$	275	130		125	57		100	40		ns	
t_s	Set-Up Time, $\overline{CP_1}$ to CP_0	275	130		125	57		100	40		ns	
f_{MAX}	Input Count Frequency (Note 3)	2	4		4	10		5	12		MHz	

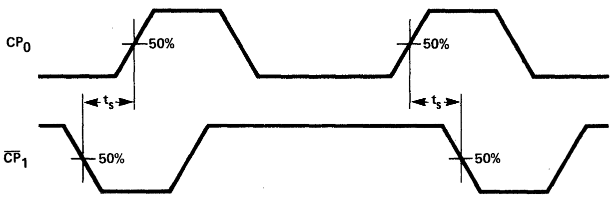
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTHS FOR CP_0, $\overline{CP_1}$ AND MR AND MR RECOVERY TIME



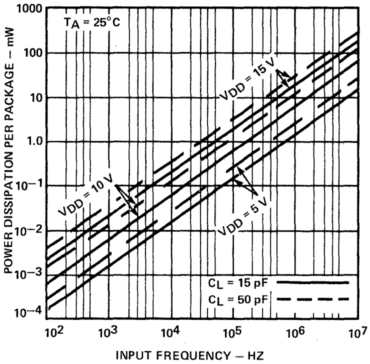
SET-UP AND HOLD TIMES, CP_0 TO $\overline{CP_1}$ AND $\overline{CP_1}$ TO CP_0

CONDITIONS: $\overline{CP_1}$ = HIGH and the device triggers on a LOW-to-HIGH transition at CP_0. The timing also applies when CP_0 = LOW and the device triggers on a HIGH-to-LOW transition at $\overline{CP_1}$.

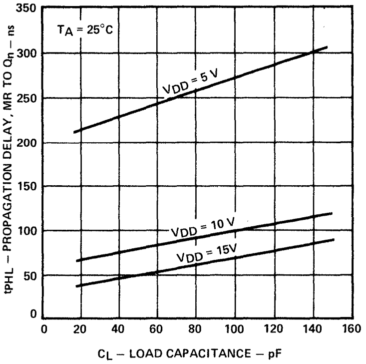
NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

TYPICAL ELECTRICAL CHARACTERISTICS

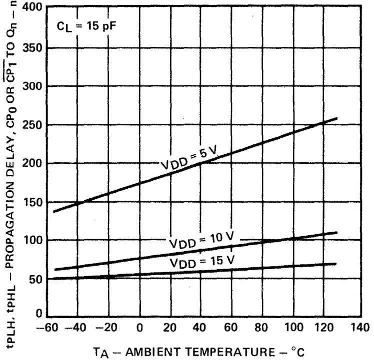
POWER DISSIPATION VERSUS FREQUENCY



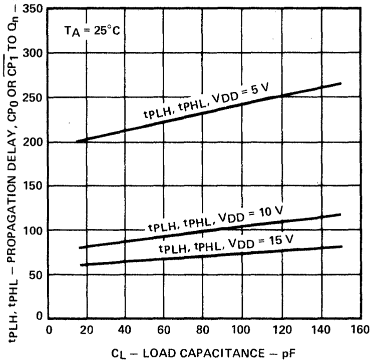
PROPAGATION DELAY, MR TO Q_n, VERSUS LOAD CAPACITANCE



PROPAGATION DELAY, CP_0 OR $\overline{CP_1}$ TO Q_n, VERSUS TEMPERATURE



PROPAGATION DELAY, CP_0 OR $\overline{CP_1}$ TO Q_n, VERSUS LOAD CAPACITANCE



4521B

24-STAGE BINARY COUNTER

GENERAL DESCRIPTION – The 4521B is a timing circuit consisting of an on-chip oscillator circuit and a 24-stage binary ripple counter. The device has two Oscillator Inputs (I_1 and I_2) and two Oscillator Outputs (O_1 and O_2), Source Connections to the n-channel and p-channel transistors of the oscillator circuit (S_N and S_P), a Master Reset Input (MR) and Data Outputs from the last seven stages of the 24-stage Ripple Counter (Q_{17}-Q_{23}).

The 4521B, as shown in the Block Diagram, may be used with either an external crystal oscillator circuit, an external RC oscillator circuit, or external clock input. Oscillator Output, O_2, is available for driving additional external loads. The oscillator circuit may be made less sensitive to variations in the power supply voltage by adding external resistors R_1 and R_2 (See Block Diagram). If these external resistors are not required, Source Connection S_P must be tied to V_{DD} and Source Connection S_N must be tied to V_{SS}.

The 24-Stage Ripple Counter advances on the HIGH-to-LOW transition of the clock input with parallel Data Outputs (Q_{17}-Q_{23}) from the last seven stages available.

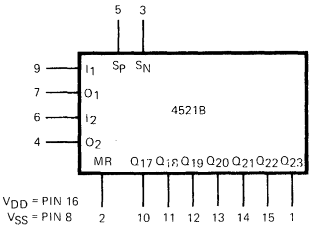
A HIGH on the Master Reset Input (MR) clears all counter stages, forcing all Parallel Data Outputs (Q_{17}-Q_{23}) LOW and disables the oscillator circuit, independent of all other inputs. This allows for very low standby power dissipation.

- **ON-CHIP CRYSTAL OSCILLATOR CIRCUIT OR ON-CHIP RC OSCILLATOR CIRCUIT OR EXTERNAL CLOCK INPUT**
- **MASTER RESET INPUT CLEARS ALL COUNTER STAGES AND DISABLES OSCILLATOR CIRCUIT FOR LOW STANDBY POWER**
- **EXTERNAL SOURCE CONNECTIONS FOR IMPROVED TIMING STABILITY**
- **OSCILLATOR OUTPUT AVAILABLE FOR DRIVING EXTERNAL LOADS**
- **MASTER RESET INPUT FACILITATES DIAGNOSTICS**

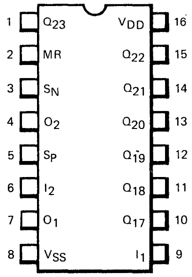
PIN NAMES

I_1, I_2	Oscillator Inputs
S_P	Source Connection-to-p-channel transistor
S_N	Source Connection-to-n-channel transistor
MR	Master Reset Input
O_1, O_2	Oscillator Outputs
Q_{17}-Q_{23}	Data Outputs

LOGIC SYMBOL

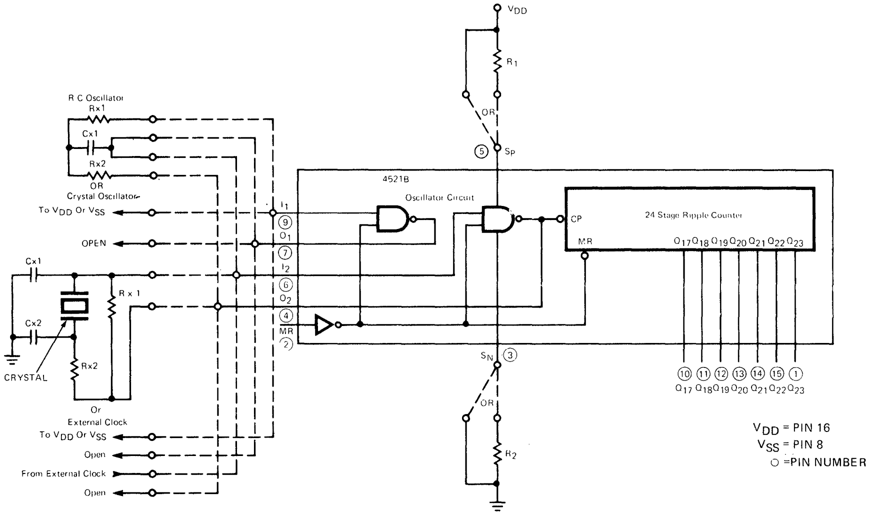


CONNECTION DIAGRAM
DIP (TOP View)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



4522B • 4526B

PROGRAMMABLE 4-BIT BCD/BINARY DOWN COUNTER

GENERAL DESCRIPTION — The 4522B/4526B is a synchronous Programmable 4-Bit BCD/Binary Down Counter with an active HIGH and an active LOW Clock Input (CP_0, $\overline{CP_1}$), an asynchronous Parallel Load Input (PL), four Parallel Inputs (P_0-P_3), a Carry Forward Input (CF), four buffered Parallel Outputs (Q_0-Q_3), a Terminal Count Output (TC) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except Master Reset Input (MR) which must be LOW. When the Parallel Load Input (PL) and the active LOW Clock Input ($\overline{CP_1}$) are LOW, the counter advances on a LOW-to-HIGH transition of the active HIGH Clock Input (CP_0). When the Parallel Load Input (PL) is LOW and the active HIGH Clock Input (CP_0) is HIGH, the counter advances on a HIGH-to-LOW transition of the $\overline{CP_1}$ Input. The Terminal Count Output (TC) is HIGH when the counter is in the zero state ($Q_0 = Q_1 = Q_2 = Q_3$ = LOW) and the Carry Forward Input (CF) is HIGH. A HIGH on the Master Reset Input (MR) resets the counter (Q_0-Q_3 = LOW) independent of other input conditions.

- **FULLY SYNCHRONOUS PROGRAMMABLE BCD/BINARY DOWN COUNTER**
- **CLOCK INPUT EITHER HIGH-TO-LOW OR LOW-TO-HIGH EDGE-TRIGGERED**
- **ASYNCHRONOUS MASTER RESET**
- **CASCADABLE**
- **ASYNCHRONOUS PARALLEL LOAD**

PIN NAMES

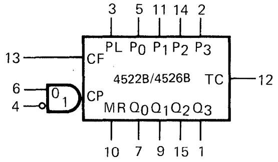
PL	Parallel Load Input
P_0-P_3	Parallel Inputs
CF	Carry Forward Input
CP_0	Clock Input (L→H Edge-Triggered)
$\overline{CP_1}$	Clock Input (H→L Edge-Triggered)
MR	Asynchronous Master Reset Input
TC	Terminal Count Output
Q_0-Q_3	Buffered Outputs

MODE SELECTION TABLE

MR	PL	CP_0	$\overline{CP_1}$	MODE
H	X	X	X	RESET (ASYNCHRONOUS)
L	H	X	X	PRESET (ASYNCHRONOUS)
L	L	↑	H	NO CHANGE
L	L	L	↓	NO CHANGE
L	L	↓	X	NO CHANGE
L	L	X	↑	NO CHANGE
L	L	↑	L	COUNTER ADVANCES
L	L	H	↓	COUNTER ADVANCES

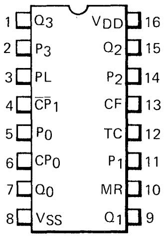
X = DON'T CARE
L = LOW LEVEL
H = HIGH LEVEL
↑ = POSITIVE - GOING TRANSITION
↓ = NEGATIVE - GOING TRANSITION

LOGIC SYMBOL



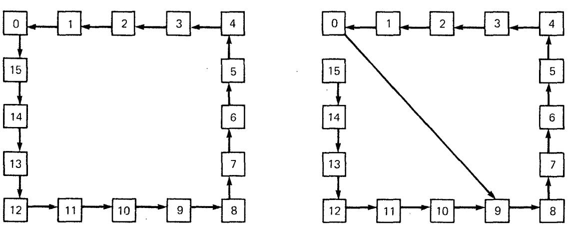
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

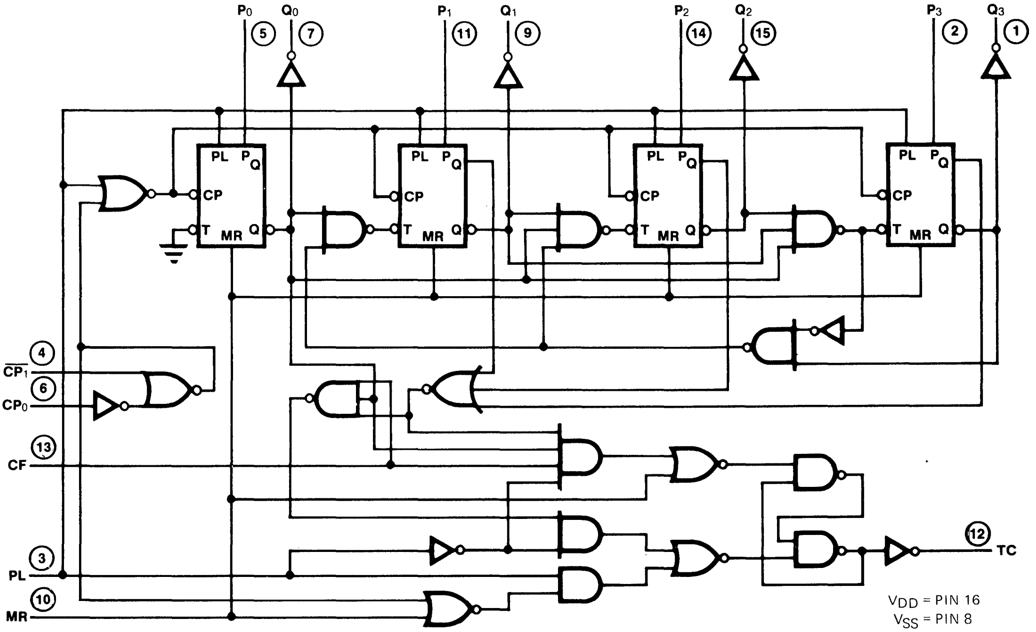
STATE DIAGRAM



LOGIC EQUATION FOR TERMINAL COUNT

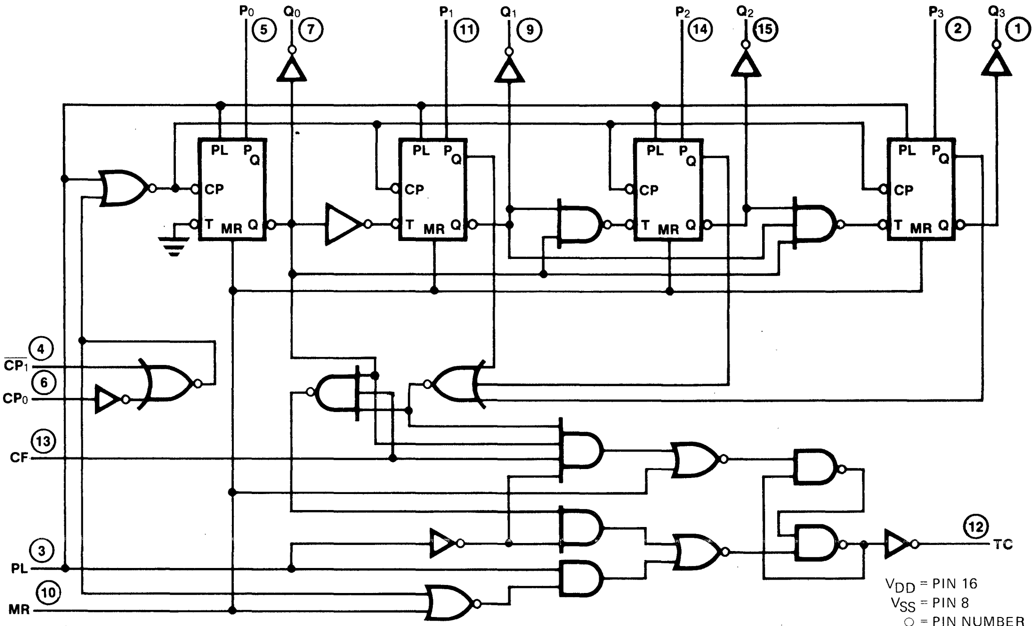
$TC = CF \bullet \overline{Q_0} \bullet \overline{(Q_1 + Q_2 + Q_3)}$

4522B LOGIC DIAGRAM

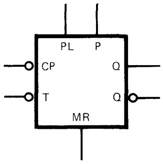


V_{DD} = PIN 16
V_{SS} = PIN 8
○ = PIN NUMBER

4526 LOGIC DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8
○ = PIN NUMBER



PL (Parallel Load Input) – Asynchronously Loads P into Q, Overriding all Other Inputs
P (Parallel Input) – Data on this Pin is Asynchronously Loaded into Q, when PL is HIGH Overriding all Other Inputs
$\overline{T}$ (Toggle Input) – Forces the Q Output to Synchronously Toggle when a LOW is Placed on this Input.
CP (Clock Pulse Input)
Q, $\overline{Q}$ (True and Complimentary Outputs)
MR (Master Reset Input)

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

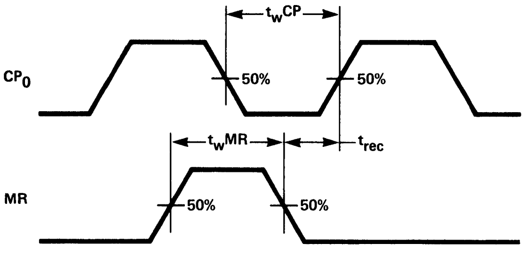
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP}_1$ to Q_n		220			95			60		ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			220			95			60		ns	
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP}_1$ to TC		240			105			66		ns	
t_{PHL}			240			105			66		ns	
t_{PLH}	Propagation Delay, CF to TC		200			85			53		ns	
t_{PHL}			200			85			53		ns	
t_{PLH}	Propagation Delay, PL to Q_n		220			90			65		ns	
t_{PHL}			220			90			65		ns	
t_{PHL}	Propagation Delay, MR to Q_n		220			95			60		ns	
t_{TLH}	Output Transition Time		65			25			18		ns	
t_{THL}			65			25			18		ns	
t_{rec}	MR Recovery Time		15			5			0		ns	
t_WMR	MR Minimum Pulse Width		70			30			20		ns	
t_{rec}	PL Recovery Time		15			5			0		ns	
t_WPL	PL Minimum Pulse Width		70			30			20		ns	
t_WCP	CP Minimum Pulse Width		120			50			35		ns	
t_s	Set-Up Time, CF to CLOCK		150			50			35		ns	
t_h	Hold Time, CF to CLOCK		100			40			25		ns	
t_s	Set-Up Time, P_n to PL		30			15			10		ns	
t_h	Hold Time, P_n to PL		25			10			5		ns	
t_h	Hold Time, CP_0 to $\overline{CP}_1$		130			57			40		ns	
t_h	Hold Time, $\overline{CP}_1$ to CP_0		130			57			40		ns	
f_{MAX}	Input Count Frequency (Note 3)		4			10			12		MHz	

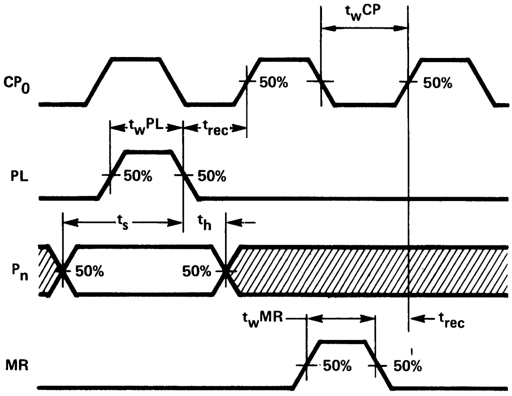
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS

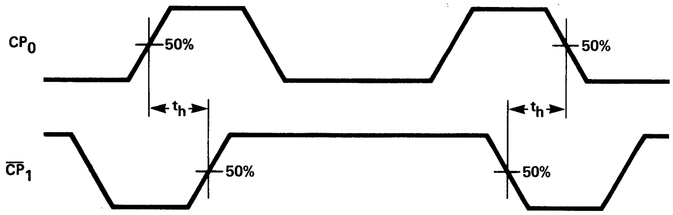


MINIMUM PULSE WIDTHS FOR
CP_0 AND MR AND MR RECOVERY TIME

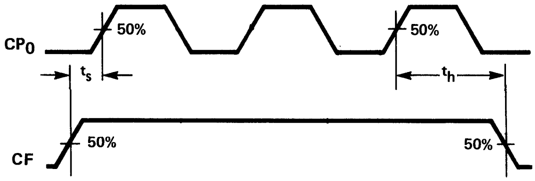


MIMIMUM CP_0, PL AND MR PULSE WIDTH,
RECOVERY TIME FOR PL AND MR, AND SET-UP
AND HOLD TIMES, P_n TO PL

CONDITIONS:$\overline{CP}_1$ = LOW and the device triggers on a LOW-to-HIGH transition at CP_0. The timing also applies when CP_0 = HIGH and the device triggers on a HIGH-to-LOW transition at $\overline{CP}_1$. MR = PL = LOW.



HOLD TIMES, CP_0 TO $\overline{CP_1}$ AND $\overline{CP_1}$ TO CP_0



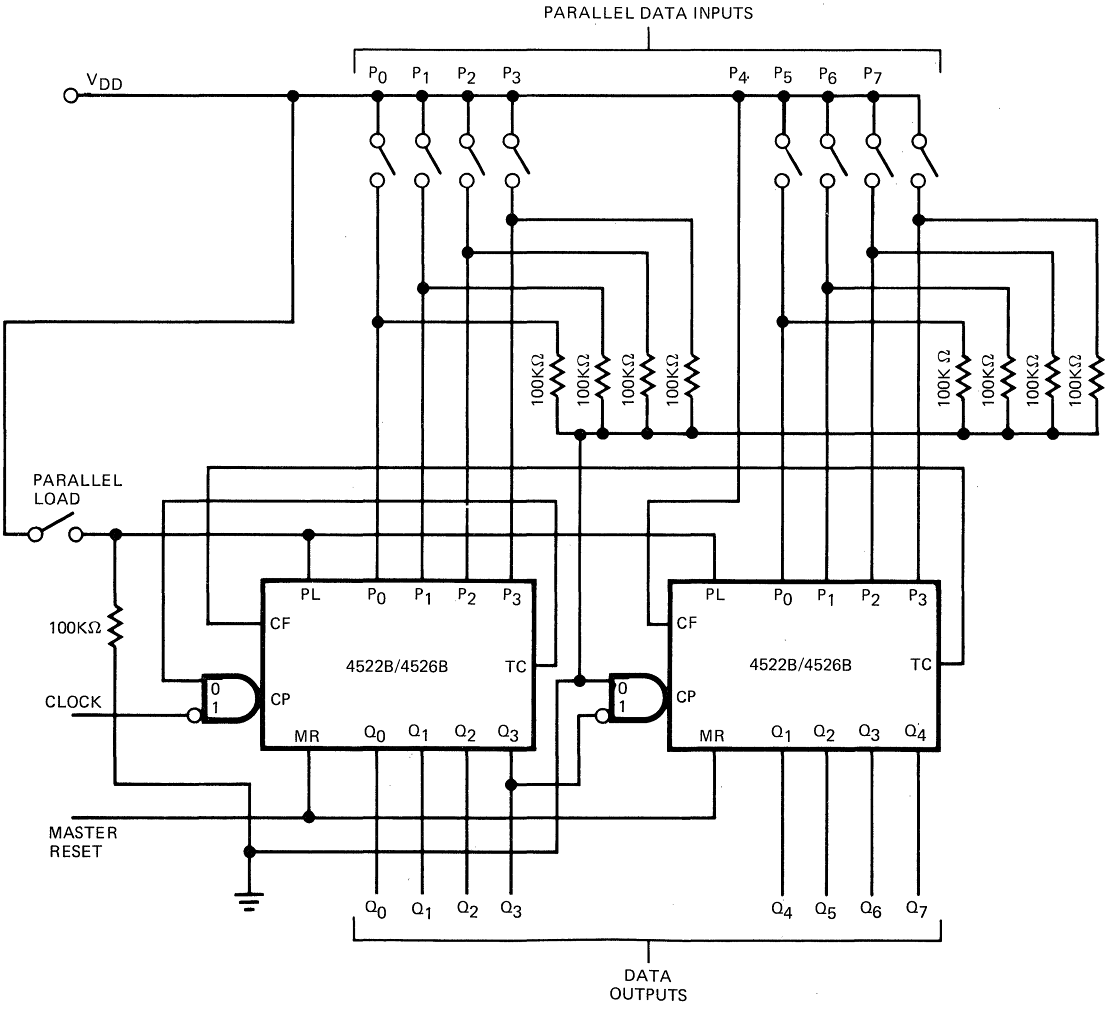
SET UP AND HOLD TIMES, CF TO CP_0

CONDITIONS:$\overline{CP}_1$ = LOW and the device triggers on a LOW-to-HIGH transition at CP_0. The timing also applies when CP_0 = HIGH and the device triggers on a HIGH-to-LOW transition at $\overline{CP}_1$.

NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

TYPICAL APPLICATIONS

2-STAGE PROGRAMMABLE DOWN COUNTER



4527B

BCD RATE MULTIPLIER

DESCRIPTION – The 4527B is a BCD Rate Multiplier with an active LOW Count Enable Input ($\overline{CE}$), and active LOW Q Output Enable Input ($\overline{E}_Q$), and active LOW Output Enable Input ($\overline{E}$), a Clock Input (CP), four Mode Select Inputs (S_0-S_3), a Preset to Nine Input (P_9), an asynchronous Master Reset Input (MR), an active LOW Count Enable Output ($\overline{O}_{CE}$), a Carry Output (Q_9) and True and Complementary Data Outputs (Q, $\overline{Q}$).

When the Master Reset (MR), the Preset to Nine (P_9) and the Count Enable ($\overline{CE}$) Inputs are LOW, the internal Synchronous 4-Bit Decade Counter triggers on a LOW-to-HIGH transition at the Clock Input (CP). As shown in the Truth Table, information present on the Mode Select Inputs (S_0-S_3) determines the output pulse rate at the Data Outputs (Q and $\overline{Q}$). For example, if S_3=S_0=LOW and S_1=S_2=HIGH, there will be output pulses at the Data Outputs (Q and $\overline{Q}$) for every ten input pulses at the Clock Input (CP). Data outputs (Q and $\overline{Q}$) are synchronized with the HIGH-to-LOW transition at the Clock Input (CP). When the Count Enable Input ($\overline{CE}$) is HIGH the internal BCD Decade Counter is disabled and no change occurs in the state of the counter.

With the Q Output Enable Input ($\overline{E}_Q$) LOW, a HIGH on the Output Enable Input ($\overline{E}$) forces Data Output Q LOW and Complementary Data Output $\overline{Q}$ HIGH, independent of all other input conditions. A HIGH on the Q Output Enable Input $\overline{E}_Q$ forces the Data Output Q HIGH, independent of all other input conditions.

The Carry Output (Q_9) goes HIGH when the two most significant bits of the internal BCD Counter are HIGH and provides one output pulse for every ten input pulses at the Clock Input (CP). The Count Enable Output ($\overline{O}_{CE}$) goes LOW when either the Count Enable Input ($\overline{CE}$) is HIGH or the Carry Output (Q_9) is LOW and provides one output pulse for every ten input pulses at the Clock Input (CP).

With Mode Select Input S_3 LOW, a HIGH on the Master Reset Input (MR) resets the two least significant bits of the internal BCD Counter and forces Data Output Q LOW, Complementary Data Output $\overline{Q}$ HIGH, Carry Output Q_9 HIGH and Count Enable Output $\overline{O}_{CE}$ LOW, independent of Clock Input, CP, Count Enable Input $\overline{CE}$ and Mode Select Inputs S_0-S_2. With Mode Select Input S_3 HIGH, a HIGH on the Master Reset Input (MR) resets the two least significant bits of the internal BCD Counter and forces Carry Output Q_9 HIGH and Count Enable Output $\overline{O}_{CE}$ LOW and provides 10 output pulses at the Data Outputs (Q and $\overline{Q}$) for every 10 input pulses at the Clock Input (CP) independent of Mode Select Inputs S_0-S_2.

A HIGH on the Preset to Nine Input (P_9) resets the two least significant bits and sets the two most significant bits of the internal BCD Counter and forces Data Output Q LOW, Complementary Data Output $\overline{Q}$ HIGH, Carry Output Q_9 LOW and Count Enable Output $\overline{O}_{CE}$ HIGH independent of the Clock (CP), Count Enable ($\overline{CE}$) and Master Reset (MR) inputs.

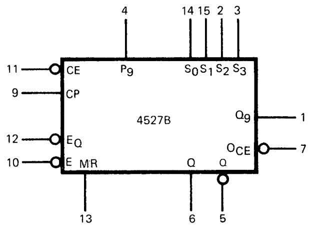
4527B applications include performance of arithmetic operations, solution of algebraic and differential equations, generation of logrithms and trigonometric functions A/D and D/A conversion, and frequency synthesis.

- **INTERNAL SYNCHRONOUS COUNTERS**
- **COUNT ENABLE AND OUTPUT ENABLE INPUTS**
- **TRUE AND COMPLEMENTARY OUTPUTS SYNCHRONIZED WITH THE HIGH-TO-LOW TRANSITION AT THE CLOCK INPUT**
- **EASY CASCADING**
- **MASTER RESET AND PRESET TO NINE INPUTS**

PIN NAMES

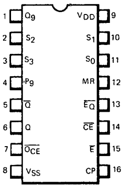
$\overline{CE}$	Count Enable Input (Active LOW)
$\overline{E}_Q$	Q Output Enable Input (Active LOW)
$\overline{E}$	Output Enable Input (Active LOW)
CP	Clock Input (L→H Triggered)
S_0-S_3	Mode Select Inputs
P_9	Preset to Nine Input
MR	Master Reset Input
$\overline{O}_{CE}$	Count Enable Output (Active LOW)
Q_9	Carry Output
Q	Data Output
$\overline{Q}$	Complementary Data Output (Active LOW)

LOGIC SYMBOL



V_{DD} = PIN 16
V_{SS} = PIN 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

INPUTS										OUTPUTS			
										OUTPUT LOGIC LEVEL OR NUMBER OF OUTPUT PULSES			
S_3	S_2	S_1	S_0	NUMBER OF CLOCK PULSES ON INPUT CP	$\overline{CE}$	$\overline{E}$	$\overline{E_Q}$	MR	P_9	Q	$\overline{Q}$	Q_9	$\overline{O_{CE}}$
L	L	L	L	10	L	L	L	L	L	L	H	1	1
L	L	L	H	10	L	L	L	L	L	1	1	1	1
L	L	H	L	10	L	L	L	L	L	2	2	1	1
L	L	H	H	10	L	L	L	L	L	3	3	1	1
L	H	L	L	10	L	L	L	L	L	4	4	1	1
L	H	L	H	10	L	L	L	L	L	5	5	1	1
L	H	H	L	10	L	L	L	L	L	6	6	1	1
L	H	H	H	10	L	L	L	L	L	7	7	1	1
H	L	L	L	10	L	L	L	L	L	8	8	1	1
H	L	L	H	10	L	L	L	L	L	9	9	1	1
H	L	H	L	10	L	L	L	L	L	8	8	1	1
H	L	H	H	10	L	L	L	L	L	9	9	1	1
H	H	L	L	10	L	L	L	L	L	8	8	1	1
H	H	L	H	10	L	L	L	L	L	9	9	1	1
H	H	H	L	10	L	L	L	L	L	8	8	1	1
H	H	H	H	10	L	L	L	L	L	9	9	1	1
X	X	X	X	10	H	L	L	L	L	*	*	*	*
X	X	X	X	10	L	H	L	L	L	L	H	1	1
X	X	X	X	10	L	L	H	L	L	H	**	1	1
H	X	X	X	10	L	L	L	H	L	10	10	H	L
L	X	X	X	10	L	L	L	H	L	L	H	H	L
X	X	X	X	10	L	L	L	L	H	L	H	L	H

L = LOW level
H = HIGH level
X = Don't Care

* Output Logic Level Depends upon the Internal State of the Counter

** Output is the same as the first 16 lines of the Truth Table with the number of Output pulses depending upon the logic levels at inputs S_0-S_3

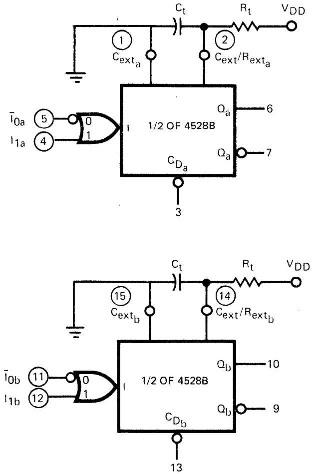
4528B

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION — The 4528B is a Dual Retriggerable Resettable Monostable Multivibrator. Each Multivibrator has an active LOW Input ($\overline{I_0}$), an active HIGH Input (I_1), an active LOW Clear Direct Input ($\overline{C_D}$), an Output (Q), its Complement ($\overline{Q}$) and two pins for connecting the external timing components (C_{ext}, C_{ext}/R_{ext}). An external timing capacitor must be connected between C_{ext} and C_{ext}/R_{ext} and an external resistor must be connected between C_{ext}/R_{ext} and V_{DD}.

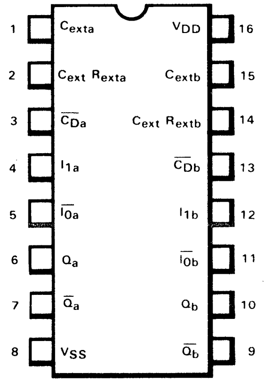
A HIGH-to-LOW transition on the $\overline{I_0}$ Input when the I_1 Input is LOW or a LOW-to-HIGH transition on the I_1 Input when the $\overline{I_0}$ Input is HIGH produces a positive pulse (L → H → L) on the Q Output and a negative pulse (H → L → H) on the $\overline{Q}$ Output if the Clear Direct Input ($\overline{C_D}$) is HIGH. A LOW on the Clear Direct Input ($\overline{C_D}$) forces the Q Output LOW, the $\overline{Q}$ Output HIGH and inhibits any further pulses until the Clear Direct Input ($\overline{C_D}$) is HIGH.

- **RECOMMENDED OPERATING VOLTAGE, V_{DD} = 4.5 TO 15 V**
- **TYPICAL OUTPUT PULSE WIDTH VARIATION ± 3% AT V_{DD} = 15 V FROM DEVICE TO DEVICE**
- **TYPICAL OUTPUT PULSE WIDTH STABILITY ± 1% OVER -40°C TO +85°C TEMPERATURE RANGE AT V_{DD} = 10 V**
- **TYPICAL OUTPUT PULSE WIDTH STABILITY ± 1% AT V_{DD} = 10 V ±0.25 V RESETTABLE**
- **TRIGGER ON EITHER A HIGH-TO-LOW TRANSITION ON $\overline{I_0}$ OR A LOW-TO-HIGH TRANSITION ON I_1**
- **COMPLEMENTARY OUTPUTS AVAILABLE**
- **BROAD TIMING RESISTOR RANGE, 5 kΩ TO 2 MΩ**
- **OUTPUT PULSE WIDTH INDEPENDENT OF DUTY CYCLE WITH A WIDE 26 ns TO ∞ RANGE**



V_{DD} = PIN 16
V_{SS} = PIN 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

$\overline{I}_{0a}$, $\overline{I}_{0b}$	Input (H→L Triggered)
I_{1a}, I_{1b}	Input (L→H Triggered)
$\overline{C_{Da}}$, $\overline{C_{Db}}$	Clear Direct (Active LOW) Input
Q_a, Q_b	Output
$\overline{Q}_a$, $\overline{Q}_b$	Complimentary (Active LOW) Output
C_{exta}, C_{extb}	External Capacitor Connections
C_{ext}/R_{exta}, C_{ext}/R_{extb}	External Capacitor/Resistor Connections

TRUTH TABLE

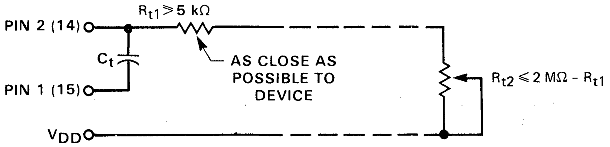
$\overline{I_0}$	I_1	$\overline{C_D}$	OPERATION
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Level
L = LOW Level
H→L = HIGH-to-LOW Transition
L→H = LOW-to-HIGH Transition
X = Don't Care

OPERATING RULES

Timing

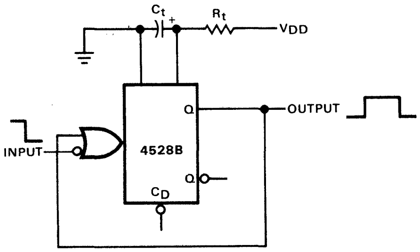
1. An external resistor (R_t) and external capacitor (C_t) are required as shown in the Logic Diagram. The value of R_t may vary from 5 kΩ to 2 MΩ.
2. The value of C_t may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{DD}/R_t the timing diagrams may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 2 (14) and the (-) terminal to pin 1 (15). Pin 2 (14) will remain positive with respect to pin 1 (15).
4. The output pulse width can be determined from the pulse width versus C_t or R_t graphs (Figures 1 and 2).
5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



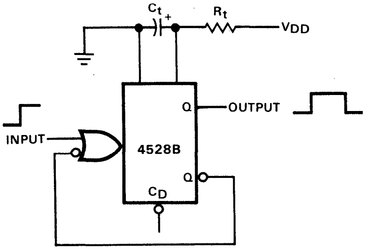
6. Under any operating condition, C_t and R_t (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. V_{DD} and ground wiring should conform to good high frequency standards so that switching transients on V_{DD} and ground pins do not cause interaction between one shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{DD} and ground located near the 4528B is recommended.
8. To minimize noise problems, it is recommended that pin 1 and pin 15 be tied externally to V_{SS}.

Triggering

1. The minimum negative pulse width into $\overline{I_0}$ is 32 ns at V_{DD} = 10 V and the minimum positive pulse width into I_1 is 32 ns at V_{DD} = 10 V.
2. When non-retriggerable operation is required, *i.e.,* when input triggers are to be ignored during a quasi-stable state, input latching is used to inhibit retriggering. The device does not retrigger if an additional trigger input occurs while the capacitor is discharging in response to the initial trigger input.



NEGATIVE EDGE-TRIGGER



POSITIVE EDGE-TRIGGER

3. An overriding active LOW level Clear Direct ($\overline{C_D}$) is provided on each multivibrator. By applying a LOW to the $\overline{C_D}$, any timing cycle can be terminated or any new cycle inhibited until the LOW Clear Input is removed. Trigger inputs will not produce spikes in the output when the Clear Direct Input is held LOW. A new cycle initiated less than 200 ns after removal of a Clear Direct Input ($\overline{C_D}$) will not have a standard output pulse width.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (see Note 4)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN. 25°C	Cext/Rext = V_{DD} All other inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN. 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{I}_0$ to Q		205	335		90	130		60	104	ns	C_L = 50 pF, R_L = 200 kΩ, Input Transition Times ≤ 20 ns R_t = 5 kΩ to 2 MΩ Any C_t
t_{PHL}	Propagation Delay, $\overline{I}_0$ to $\overline{Q}$		205	335		90	130		60	104		
t_{PLH}	Propagation Delay, I_1 to Q		205	335		90	130		60	104	ns	
t_{PHL}	Propagation Delay, I_1 to $\overline{Q}$		205	335		90	130		60	104		
t_{PLH}	Propagation Delay, $\overline{C}_D$ to Q		145	230		60	85		40	68	ns	
t_{PHL}	Propagation Delay, $\overline{C}_D$ to $\overline{Q}$		145	230		60	85		40	68		
t_{TLH}	Output Transition Time		70	135		32	70		22	45	ns	
t_{THL}			70	135		32	70		22	45		
t_{rec}	$\overline{C}_D$ Recovery Time (Note 1)	-50	–90		-20	–37		0	–25		ns	
$t_W\overline{I}_0$	$\overline{I}_0$ Minimum Pulse Width (LOW)	70	45		32	24		26	20		ns	
t_WI_1	I_1 Minimum Pulse Width (HIGH)	70	45		32	24		26	20		ns	
$t_W\overline{C}_D$	$\overline{C}_D$ Minimum Pulse Width	65	45		32	26		26	21		ns	
t_WQ	Q Minimum Output Pulse Width		300	500		200	400		150	300	ns	
		R_t = 5 kΩ, C_t = 15 pF										
t_WQ	Q Output Pulse Width	4.35	6.25	8	4	5.3	6.6	4	5	6	µs	
		R_t = 10 kΩ, C_t = 1000 pF										
Δt	Change in Q Output Pulse Width over Temperature		±2	±10		±1	±7		±1	±5	%	
		T_A = - 40°C to +85°C										
Δt	Change in Q Output Pulse Width over V_{DD}		±2	±4		±1	±2		±1	±2	%	
		V_{DD} = 5 V ±.25 V			V_{DD} = 10 V ±.25 V			V_{DD} = 15 V ± 25 V				
t_s	Set-Up Time, $\overline{C}_D$ to $\overline{I}_0$ or I_1 (To prevent change in output)	20	5		-25	- 45		-25	- 35		ns	
R_t	External Timing Resistor Any V_{DD}				5		2000				kΩ	
C_t	External Timing Capacitor	No Limits									µF	

Notes:

1. The 4528B device does not retrigger if an additional trigger input occurs while the capacitor is discharging in response to the initial trigger input.
2. A new cycle initiated less than 200 ns after removal of a Clear Direct Input ($\overline{C}_D$) will not have a standard output pulse width.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. Additional D. C. Characteristics are listed in this section under Fairchild 4000B Series CMOS Family Characteristics.
5. To minimize power dissipation unused multivibrators should have the Cextl Rext Connection tied to VDD, the Cext Connection tied to V_{SS} and all other inputs tied to either V_{DD} or V_{SS}.
6. It is recommended that Input Rise and Fall Times to inputs $\overline{I}_0$ and I_1 be less than 15 µs at V_{DD} = 5V, 4 µs at V_{DD} = 10V and 3 µs at V_{DD} = 15V.

TYPICAL ELECTRICAL CHARACTERISTICS

TYPICAL OUTPUT PULSE WIDTH VERSUS R_t AND C_t

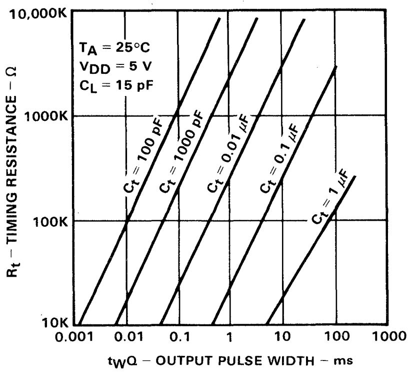


FIGURE 1.

TYPICAL OUTPUT PULSE WIDTH VERSUS R_t AND C_t

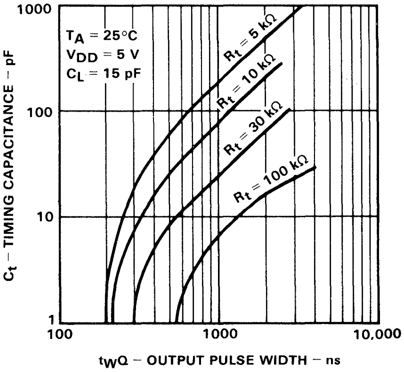
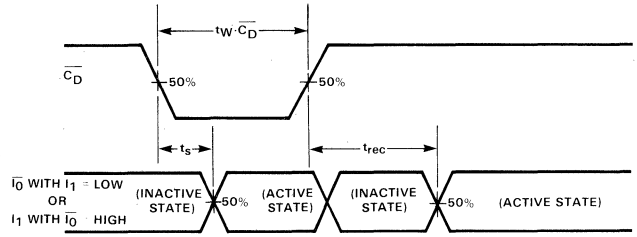
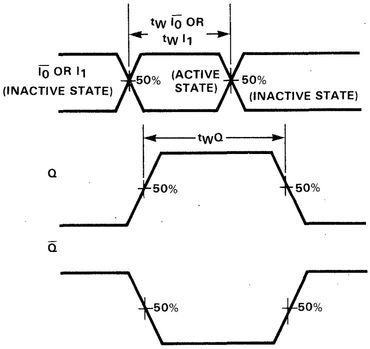


FIGURE 2.

AC WAVEFORMS



Set-up Time, $\overline{C_D}$ to $\overline{I_0}$ or I_1, Recovery Time for $\overline{C_D}$ and Minimum $\overline{C_D}$ Pulse Width.



Minimum $\overline{I_0}$ or I_1 Pulse Width and Minimum Output Pulse Width.

NOTE: Set-up Time and Recovery Time are shown as Positive values, but may specified as Negative values.

APPLICATIONS

The 4528B Monostable Multivibrator has its pulse width determined by an externally supplied Resistor-Capacitor network. A two step procedure is suggested for determing the proper R_tC_t combination (Equation 1) for a specific pulse width.

The first step is to choose a capacitor. Figure 1 shows pulse width versus resistor value with the capacitor value as the running parameter. A capacitor value is chosen so that the approximate resistor value is between 20 kΩ and 2 MΩ. Once the capacitor is determined, the timing constant (K) is found from Figure 3 for a specific V_{DD}. The resistor value is then determined from Equation 2. If the resistor value is less than 20 kΩ the timing constant should be increased by 20% and the resistor value re-calculated. The resistor must be larger than 5 kΩ.

No upper limit on the capacitor is required. If a large value of R_t and C_t are to be used the timing between pulses or duty cycle, must be sufficiently low that the capacitor fully charges to V_{DD}. Large capacitor values must be sufficiently low in leakage that the resistor value can supply the leakage of the capacitor and still charge the capacitor close to V_{DD}.

EXAMPLE:

Three pulse widths of 0.1, 1, and 10 ms are to be generated with the 4528B using a single capacitor.

From Figure 1 a capacitor value between 0.01 and .1 uF would be reasonable. A 0.022 μF capacitor is the only capacitor that is available.

The timing constant for a 0.022 μF at 10 V V_{DD} is found from Figure 3 to be approximately 0.3.

The resistor values are then calculated:

Pulse Width	R_t
0.1 ms	15.1 kΩ
1 ms	151.1 kΩ
10 ms	1.51 MΩ

The 15.1 kΩ is less than 20 kΩ so add 20% to the K value and recalculate

Pulse Width	R_t	
0.1 ms	12.5 kΩ	K = .36

Equation 1: $P.W. = KR_tC_t$

Equation 2: $P.W. = \frac{R_t}{KC_t}$

P.W. = Pulse Width (seconds)

K = Timing Constant

C_t = Capacitance (Farads)

R_t = Resistance (ohms)

TIMING CONSTANT VERSUS TIMING CAPACITANCE

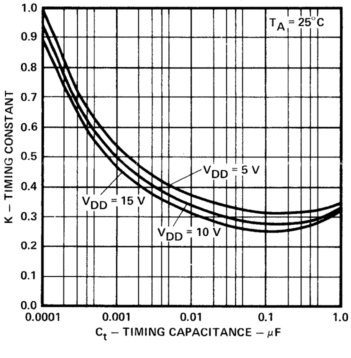


Fig. 3.

4531B

13-INPUT PARITY CHECKER GENERATOR

DESCRIPTION – The 4531B is a 13-Input Parity Checker/Generator with 13 Parity Inputs (I_0–I_{12}) and a Parity Output (Z). When the number of Parity Inputs that are HIGH is even, the Output (Z) is LOW. When the number of Parity Inputs that are HIGH is odd, the Output (Z) is HIGH. For words of 12 bits or less, the Output (Z) can be used to generate either odd or even parity by appropriate termination of the unused Parity Input (s). For words of 14 or more bits, the devices can be cascaded by connecting the output (Z) of one device to any Parity Input (I_0–I_{12}) of another device. When cascading devices, it is recommended that the Output (Z) of one device be connected to the I_{12} input of the other device since there is less delay to the Output (Z) from the I_{12} input than from any other Input (I_0-I_{11}).

- **VARIABLE WORD LENGTH**
- **FULLY BUFFERED OUTPUT (ACTIVE HIGH)**
- **PARITY INPUTS (ACTIVE HIGH)**

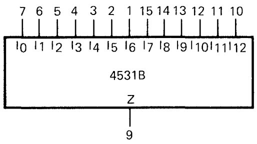
PIN NAMES	**FUNCTION**
I_0-I_{12}	Parity Inputs
Z	Buffered Output

TRUTH TABLE

INPUTS	OUTPUT
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7 I_8 I_9 I_{10} I_{11} I_{12}	Z
All Thirteen Inputs LOW	L
Any One Input HIGH	H
Any Two Inputs HIGH	L
Any Three Inputs HIGH	H
Any Four Inputs HIGH	L
Any Five Inputs HIGH	H
Any Six Inputs HIGH	L
Any Seven Inputs HIGH	H
Any Eight Inputs HIGH	L
Any Nine Inputs HIGH	H
Any Ten Inputs HIGH	L
Any Eleven Inputs HIGH	H
Any Twelve Inputs HIGH	L
All Thirteen Inputs HIGH	H

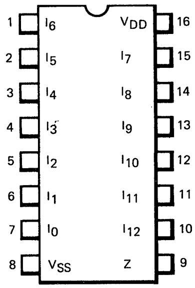
L = LOW Level
H = HIGH Level

LOGIC SYMBOL



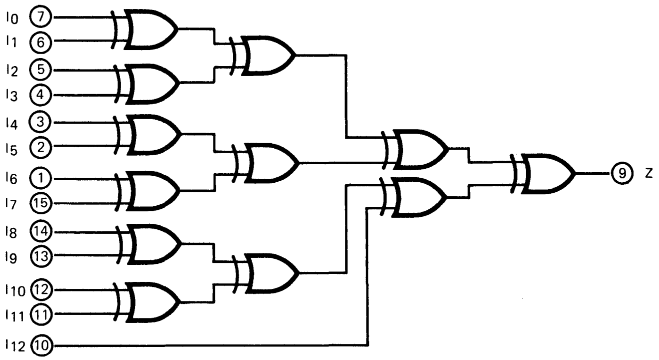
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, I_0-I_{11} to Z		195	500		80	225		55	180	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			195	500		80	225		55	180	ns	
t_{PLH}	Propagation Delay, I_{12} to Z		115	300		50	135		35	109	ns	
t_{PHL}			115	300		50	135		35	109	ns	
t_{TLH}	Output Transition Time		65	135		35	75		15	45	ns	
t_{THL}			65	135		35	75		15	45	ns	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

4532B

8-INPUT PRIORITY ENCODER

DESCRIPTION — The 4532B is an 8-Input Priority Encoder with eight active HIGH Priority Inputs (I_0-I_7), three active HIGH Address Outputs (A_0-A_2), an active HIGH Enable Input (E_{In}), an active HIGH Enable Output (E_{Out}) and an active HIGH Group Select Output (GS).

Data is accepted on the eight Priority Inputs (I_0-I_7). The binary code corresponding to the highest Priority Input (I_0-I_7) which is HIGH is generated on the Address Outputs (A_0-A_2) if the Enable Input (E_{In}) is HIGH. Priority Input I_7 is assigned the highest priority. The Group Select output (GS) is HIGH when one or more Priority Inputs (I_0-I_7) and the Enable Input (E_{In}) are HIGH. The Enable Output (E_{Out}) is HIGH when all the Priority Inputs (I_0-I_7) are LOW and the Enable Input (E_{In}) is HIGH. The Enable Input (E_{In}) when LOW, forces all Outputs (A_0-A_2, GS, E_{Out}) LOW.

- **ACTIVE HIGH PRIORITY INPUTS**
- **CASCADABLE**

PIN NAMES

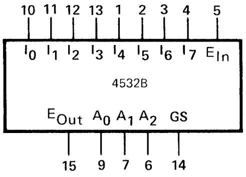
I_0-I_7	Priority Inputs
E_{In}	Enable Input
E_{Out}	Enable Output
GS	Group Select Output
A_0-A_2	Address Outputs

TRUTH TABLE

INPUTS									OUTPUTS				
E_{In}	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	GS	A_2	A_1	A_0	E_{Out}
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	X	X	X	X	X	X	X	H	H	H	H	L
H	L	H	X	X	X	X	X	X	H	H	H	L	L
H	L	L	H	X	X	X	X	X	H	H	L	H	L
H	L	L	L	H	X	X	X	X	H	H	L	L	L
H	L	L	L	L	H	X	X	X	H	L	H	H	L
H	L	L	L	L	L	H	X	X	H	L	H	L	L
H	L	L	L	L	L	L	H	X	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

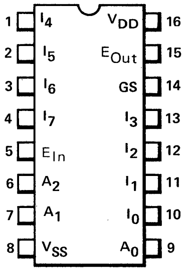
X = Don't Care (Either HIGH or LOW)
L = LOW Level
H = HIGH Level

LOGIC SYMBOL



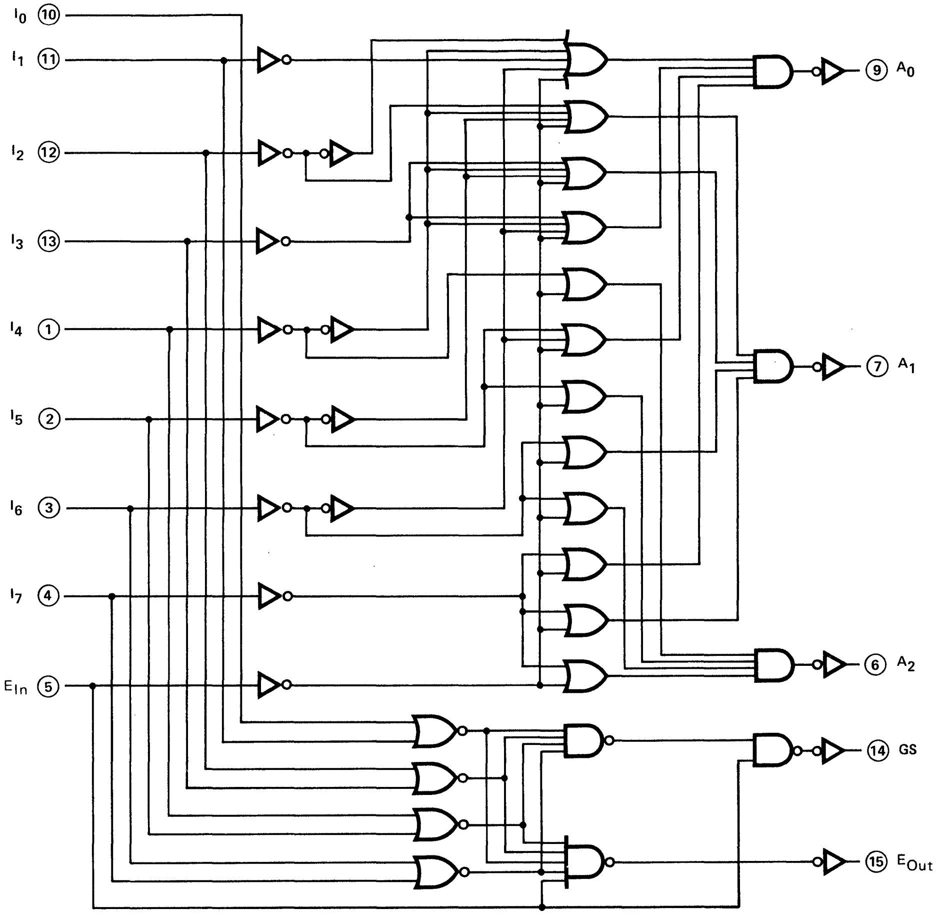
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMIT									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, E_{In} to E_{Out}		85 85	200 200		45 45	90 90		35 35	70 70	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, E_{In} to GS		65 65	150 150		35 35	70 70		25 25	56 56	ns	
t_{PLH} t_{PHL}	Propagation Delay, E_{In} to A_n		70 70	200 200		35 35	90 90		30 30	70 70	ns	
t_{PLH} t_{PHL}	Propagation Delay, I_n to A_n		70 70	200 200		35 35	90 90		30 30	70 70	ns	
t_{PLH} t_{PHL}	Propagation Delay, I_n to GS		75 70	200 200		40 35	90 90		31 28	70 70	ns	
t_{TLH} t_{THL}	Output Transition Time		65 65	135 135		35 35	75 75		15 15	45 45	ns	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characterisitcs.

4539B

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION – The 4539B is a Dual 4-Input Digital Multiplexer with common select logic. Each multiplexer has four Multiplexer Inputs (I_0-I_3), an active LOW Enable Input ($\overline{E}$) and a Multiplexer Output (Z). When HIGH, the Enable Input ($\overline{E}$) forces the Multiplexer Output (Z) of the respective multiplexer LOW, independent of the Select (S_0, S_1) and Multiplexer (I_0-I_3) Inputs. With the Enable Input ($\overline{E}$) LOW, the common Select Inputs (S_0, S_1) determine which Multiplexer Input (I_0-I_3) on each of the multiplexers is routed to the respective Multiplexer Output (Z).

- **COMMON SELECT LOGIC**
- **ACTIVE LOW ENABLES**

PIN NAMES

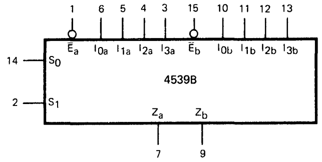
I_{0a}, I_{1a}, I_{2a}, I_{3a} I_{0b}, I_{1b}, I_{2b}, I_{3b}	Multiplexer Inputs
S_0, S_1	Select Inputs
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs (Active LOW)
Z_a, Z_b	Multiplexer Outputs

TRUTH TABLE

INPUTS			OUTPUT
S_0	S_1	$\overline{E}$	Z
X	X	H	L
L	L	L	I_0
H	L	L	I_1
L	H	L	I_2
H	H	L	I_3

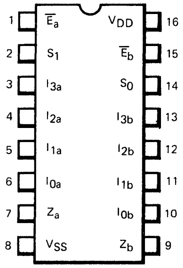
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC SYMBOL



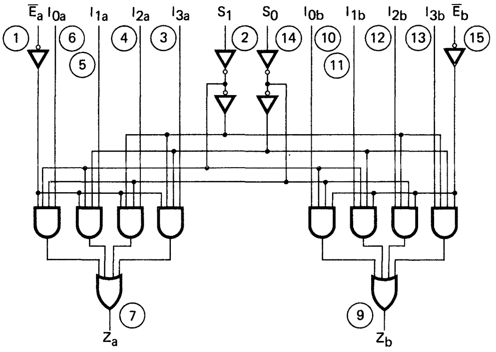
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, I_X to Z		166	375		71	160		51	125	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			140	350		58	140		40	110		
t_{PLH}	Propagation Delay, Select to Z		210	470		88	190		62	150	ns	
t_{PHL}			210	470		88	190		62	150		
t_{PLH}	Propagation Delay, $\overline{E}$ to Z		120	275		53	110		37	85	ns	
t_{PHL}			118	275		51	110		38	85		
t_{TLH}	Output Transition Time		76	135		39	75		29	45	ns	
t_{THL}			66	135		30	75		22	45		

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

4543B

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER FOR LIQUID CRYSTALS

DESCRIPTION — The 4543B is a BCD to 7-Segment Latch/Decoder/Driver for Liquid Crystal Displays with four Address Inputs (A_0-A_3), a Latch Enable Input (EL), a Blanking Input (I_B), a Clock Control Input (CP), and seven Segment Outputs (a-g).

When the Latch Enable Input (EL) is HIGH, the state of the Segment Outputs (a-g) is determined by the data on the four Address Inputs (A_0-A_3) and the Clock Control Input (CP). For driving Liquid Crystal Displays, a square wave must be applied to the CP input and to the electrically common backplane of the display. For common Cathode LED displays a LOW logic level must be applied to the CP input. For common anode LED displays a HIGH logic level must be applied to the CP input. When the Latch Enable Input (EL) goes LOW, the last data present at the address Inputs (A_0-A_3) is stored in the latches and the Segment Outputs (a-g) remain stable.

A HIGH on the Blanking Input (I_B) forces all Segment Outputs (a-g) LOW. The Blanking Input (I_B) does not affect the latch circuit.

- **BLANKING INPUT**
- **MULTIPLEXING CAPABILITY**
- **LCD DISPLAY OR COMMON ANODE OR COMMON CATHODE LED DISPLAY CAPABILITY**
- **BLANKING ON ALL ILLEGAL INPUT COMBINATIONS**

PIN NAMES

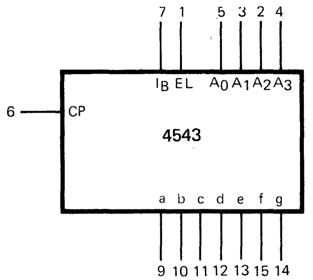
A_0-A_3	Address (Data) Inputs
EL	Latch Enable Input
I_B	Blanking Input
CP	Clock Control Input
a-g	Segment Outputs

TRUTH TABLE

INPUTS							OUTPUTS							
CP*	EL	I_B	A_3	A_2	A_1	A_0	a	b	c	d	e	f	g	DISPLAY
L	X	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	L	L	L	L	L	H	H	H	H	H	H	L	0
L	H	L	L	L	L	H	L	H	H	L	L	L	L	1
L	H	L	L	L	H	L	H	H	L	H	H	L	H	2
L	H	L	L	L	H	H	H	H	H	H	L	L	H	3
L	H	L	L	H	L	L	L	H	H	L	L	H	H	4
L	H	L	L	H	L	H	H	L	H	H	L	H	H	5
L	H	L	L	H	H	L	H	L	H	H	H	H	H	6
L	H	L	L	H	H	H	H	H	H	L	L	L	L	7
L	H	L	H	L	L	L	H	H	H	H	H	H	H	8
L	H	L	H	L	L	H	H	H	H	H	L	H	H	9
L	H	L	H	L	H	L	L	L	L	L	L	L	L	BLANK
L	H	L	H	L	H	H	L	L	L	L	L	L	L	BLANK
L	H	L	H	H	L	L	L	L	L	L	L	L	L	BLANK
L	H	L	H	H	L	H	L	L	L	L	L	L	L	BLANK
L	H	L	H	H	H	L	L	L	L	L	L	L	L	BLANK
L	H	L	H	H	H	H	L	L	L	L	L	L	L	BLANK
L	L	L	X	X	X	X			**					**
H	***	***	***			Inverse of the above Output Combinations								Display as Above

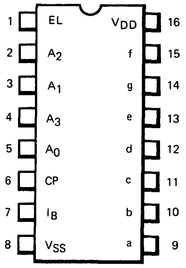
H = HIGH Level
L = LOW Level
X = Don't Care
* = For Liquid Crystal displays a square wave is applied to CP. For common cathod Light Emitting Diode displays a LOW logic level is applied to CP. For common anode Light Emitting Diode displays a HIGH logic level is applied to CP.
** = Depends upon the BCD Code applied during the HIGH-to-LOW transition of EL.
*** = The above combinations of logic levels.

LOGIC SYMBOL



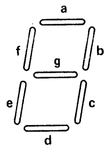
V_{DD} = PIN 16
V_{SS} = PIN 8

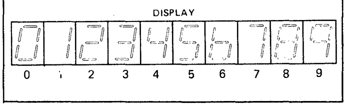
CONNECTION DIAGRAM
DIP (TOP VIEW)



Note: The flatpack version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

NUMERICAL DESIGNATIONS





4555B • 4556B

DUAL 1-OF-4 DECODERS/DEMULTIPLEXERS

DESCRIPTION – The 4555B and 4556B are Dual 1-of-4 Decoders/Demultiplexers. Each decoder/demultiplexer has two Address Inputs (A_0, A_1), an active LOW Enable Input ($\overline{E}$) and four mutually exclusive Outputs which are active HIGH for the 4555B (O_0-O_3) and active LOW for the 4556B ($\overline{O}_0$-$\overline{O}_3$).

When the 4555B is used as a decoder, the Enable Input ($\overline{E}$) when HIGH, forces all Outputs (O_0-O_3) LOW. When used as a demultiplexer, the appropriate Output is selected by the Data on the Address Inputs (A_0, A_1) and follows as the inverse of the Enable Input ($\overline{E}$). All unselected Outputs are LOW.

When the 4556B is used as a decoder, the Enable Input ($\overline{E}$) when HIGH forces all Outputs ($\overline{O}_0$-$\overline{O}_3$) HIGH. When used as a demultiplexer, the appropriate Output is selected by the data on the Address Inputs (A_0, A_1) and follows the state of the Enable Input ($\overline{E}$). All unselected Outputs are HIGH.

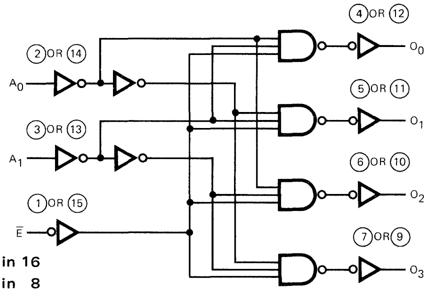
- **ACTIVE HIGH OUTPUTS FOR THE 4555B AND ACTIVE LOW OUTPUTS FOR THE 4556B**
- **OVERRIDING ACTIVE LOW ENABLE**

PIN NAMES

$\overline{E}$	Enable Input (Active LOW)
A_0, A_1	Address Inputs
O_0-O_3	Outputs (Active HIGH – 4555B Only)
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW – 4556B Only)

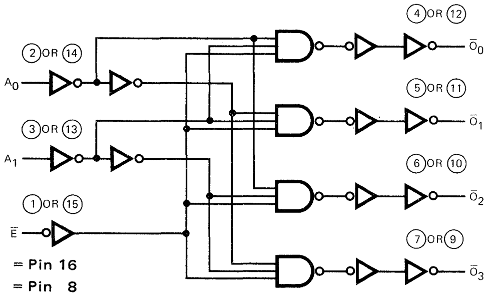
LOGIC DIAGRAMS

1/2 OF A 4555B



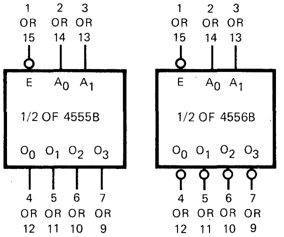
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

1/2 OF A 4556B



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

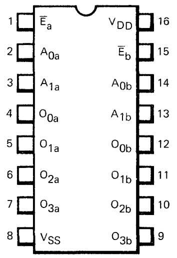
LOGIC SYMBOLS



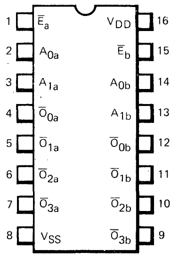
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

CONNECTION DIAGRAMS
DIP (TOP VIEW)

4555B



4556B



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

4555B TRUTH TABLE

$\overline{E}$	A_0	A_1	O_0	O_1	O_2	O_3
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H
H	X	X	L	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

4556B TRUTH TABLE

$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4555B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, Address to Output		148	285		60	145		40	116	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			127	265		54	120		45	96		
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		148	315		60	150		40	120	ns	
t_{PHL}			127	295		53	140		40	112		
t_{TLH}	Output Transition Time		65	135		20	70		25	45	ns	
t_{THL}			66	135		25	70		20	45		

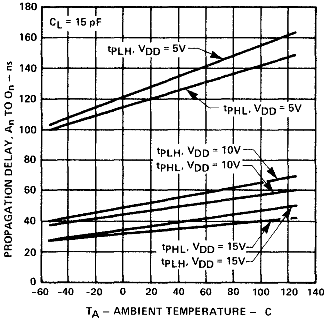
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4556B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, Address to Output		140	225		57	100		40	80	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			185	260		68	120		45	96		
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		134	225		55	110		40	88	ns	
t_{PHL}			145	245		58	110		40	88		
t_{TLH}	Output Transition Time		75	135		37	70		25	45	ns	
t_{THL}			77	135		29	70		20	45		

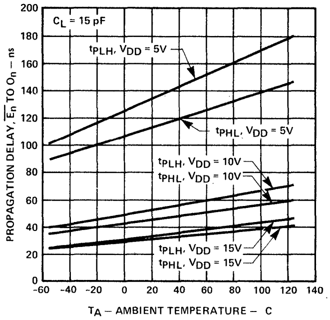
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

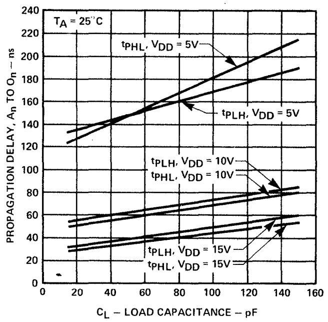
4555B
PROPAGATION DELAY,
A_n TO O_n,
VERSUS TEMPERATURE



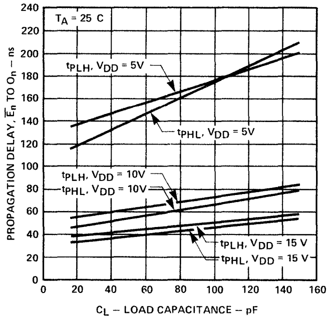
4555B
PROPAGATION DELAY,
$\overline{E}_n$ TO O_n,
VERSUS TEMPERATURE



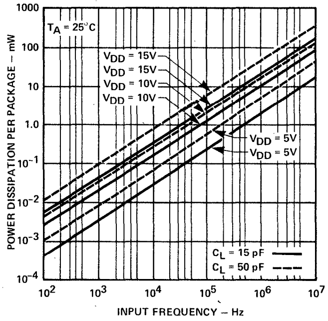
PROPAGATION DELAY,
A_n TO O_n,
VERSUS LOAD CAPACITANCE



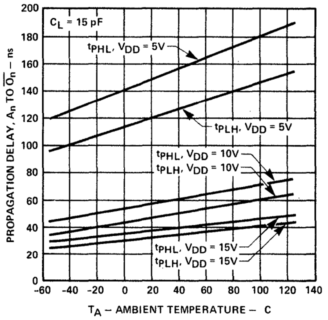
4555B
PROPAGATION DELAY,
$\overline{E}_n$ TO O_n,
VERSUS LOAD CAPACITANCE



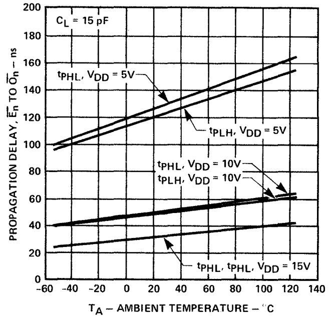
4555B AND 4556B
POWER DISSIPATION
VERSUS FREQUENCY



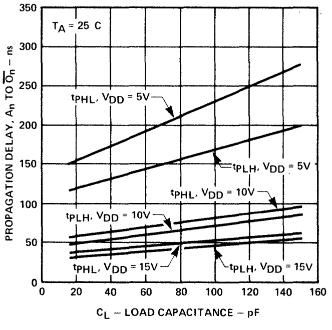
4556B
PROPAGATION DELAY,
A_n TO $\overline{O}_n$,
VERSUS TEMPERATURE



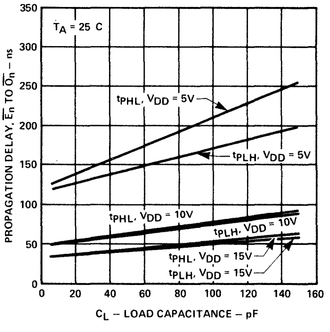
4556B
PROPAGATION DELAY,
$\overline{E}_n$ TO $\overline{O}_n$,
VERSUS TEMPERATURE



4556B
PROPAGATION DELAY,
A_n TO $\overline{O}_n$
VERSUS LOAD CAPACITANCE



4556B
PROPAGATION DELAY,
$\overline{E}_n$ TO $\overline{O}_n$,
VERSUS LOAD CAPACITANCE



4557B

1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER

DESCRIPTION – The 4557B is a 1-to-64 Bit Variable Length Shift Register with two Serial Data Inputs (D_A,D_B), a Data Select Input (S_D), six Register Length Select Inputs (S_1, S_2, S_4, S_8, S_{16} and S_{32}), active LOW and active HIGH Clock Inputs ($\overline{CP}_0$ and CP_1), True and Complementary Data Outputs (Q and $\overline{Q}$) and an overriding asynchronous Master Reset Input (MR).

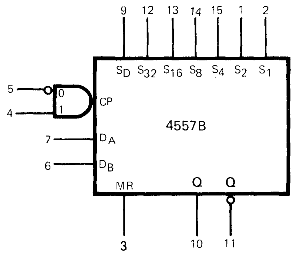
The 4557B register length is programmable. As shown in the Register Selection Table, any shift register length of between 1 and 64 bits can be selected by applying appropriate logic levels to the Register Length Select Inputs (S_1, S_2, S_4, S_8, S_{16} and S_{32}). Shift register length equals the sum of the 6-bit data word formed by the Register Length Select Inputs (S_{32} S_{16} S_8 S_4 S_2 S_1) plus one.

With Data Select Input (S_D) LOW, information at the Serial Data Input, D_B, is shifted into the Variable Length Shift Register on either a HIGH-to-LOW transition at $\overline{CP}_0$ while CP_1 is HIGH or a LOW-to-HIGH transition at CP_1 while $\overline{CP}_0$ is LOW. With the Data Select Input (S_D) HIGH, information at Serial Data Input D_A, is shifted into the register on appropriate logic level transitions and logic levels at the Clock Inputs ($\overline{CP}_0$ and CP_1) as described above.

True and Complementary Data Outputs (Q and $\overline{Q}$) from the last stage of the variable length shift register are made available.

A HIGH on the Master Reset Input (MR) clears all registers to zero (Q=LOW, $\overline{Q}$=HIGH) independent of all other inputs.

LOGIC SYMBOL



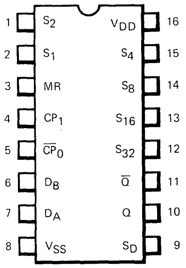
V_{DD} = Pin 16
V_{SS} = Pin 8

- **1-TO-64 BIT PROGRAMMABLE SHIFT REGISTER**
- **TRUE AND COMPLEMENTARY DATA OUTPUTS AVAILABLE**
- **ASYNCHRONOUS MASTER RESET**
- **TRIGGERS ON EITHER A HIGH-TO-LOW OR LOW-TO-HIGH TRANSITION**
- **SERIAL DATA INPUT FROM EITHER OF TWO SOURCES**

PIN NAMES

D_A,D_B	Serial Data Inputs
S_D	Data Select Input
S_1,S_2,S_4,S_8,S_{16},S_{32}	Register Length Select Inputs
$\overline{CP}_0$	Clock Input (H→L Triggered)
CP_1	Clock Input (L→H Triggered)
MR	Master Reset Input
Q	Data Output
$\overline{Q}$	Complementary Data (Active LOW) Output

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The flatpak version has the same (Connection Diagram) as the Dual In-Line Package.

REGISTER SELECTION TABLE

SELECT INPUTS						REGISTER LENGTH
S_{32}	S_{16}	S_8	S_4	S_2	S_1	
L	L	L	L	L	L	1-BITS
L	L	L	L	L	H	2-BITS
L	L	L	L	H	L	3-BITS
L	L	L	L	H	H	4-BITS
L	L	L	H	L	L	5-BITS
L	L	L	H	L	H	6-BITS
⋮	⋮	⋮	⋮	⋮	⋮	⋮
H	L	L	L	L	L	33-BITS
H	L	L	L	L	H	34-BITS
H	L	L	L	H	L	35-BITS
⋮	⋮	⋮	⋮	⋮	⋮	⋮
H	H	H	H	L	L	61-BITS
H	H	H	H	L	H	62-BITS
H	H	H	H	H	L	63 BITS
H	H	H	H	H	H	64-BITS

L = LOW Level
H = HIGH Level

Note: Shift Register Length equals the sum of the Register Length Select Input "Word" (S_1,S_2,S_4,S_8,S_{16} and S_{32}) plus one.

DATA INPUT SELECTION TABLE

INPUT			DATA INTO THE FIRST STAGE OF THE SELECTED SHIFT REGISTER
S_D	D_A	D_B	
L	X	L	L
L	X	H	H
H	L	X	L
H	H	X	H

L = LOW Level
H = HIGH Level
X = Don't Care

TRUTH TABLE

INPUTS			OPERATION
MR	$\overline{CP}_0$	CP_1	
L	L	↘	NO CHANGE
L	↗	H	NO CHANGE
L	H	X	NO CHANGE
L	X	L	NO CHANGE
L	↘	H	SELECTED REGISTER SHIFTS
L	L	↗	SELECTED REGISTER SHIFTS
H	X	X	MASTER RESET

L = LOW Level
H = HIGH Level
X = Don't Care
↗ = Positive-Going Transition
↘ = Negative-Going Transition

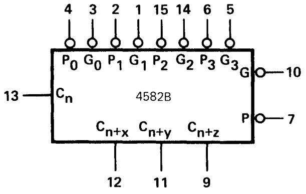
4582B

CARRY LOOKAHEAD GENERATOR

DESCRIPTION — The 4582B is a Carry Lookahead Generator which provides high speed lookahead over word lengths of more than four bits. The device has a Carry Input (C_n), four active LOW Carry Generate Inputs ($\overline{G}_0$-$\overline{G}_3$), four active LOW Carry Propagate Inputs ($\overline{P}_0$-$\overline{P}_3$), three Carry Outputs (C_{n+x}, C_{n+y}, C_{n+z}), an active LOW Carry Propagate Output ($\overline{P}$) and an active LOW Carry Generate Output ($\overline{G}$). The logic equations for all outputs are shown below.

- EXPANDABLE TO ANY NUMBER OF BITS
- HIGH SPEED LOOKAHEAD OVER WORD LENGTHS OF MORE THAN FOUR BITS

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

PIN NAMES

C_n	Carry Input
$\overline{G}_0$-$\overline{G}_3$	Carry Generate Inputs (Active LOW)
$\overline{P}_0$-$\overline{P}_3$	Carry Propagate Inputs (Active LOW)
C_{n+x}, C_{n+y}, C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

LOGIC EQUATIONS

$$C_{n+x} = G_0 + P_0 \cdot C_n$$

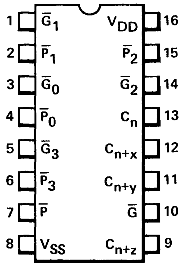
$$C_{n+y} = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_n$$

$$C_{n+z} = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_n$$

$$\overline{G} = \overline{G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0}$$

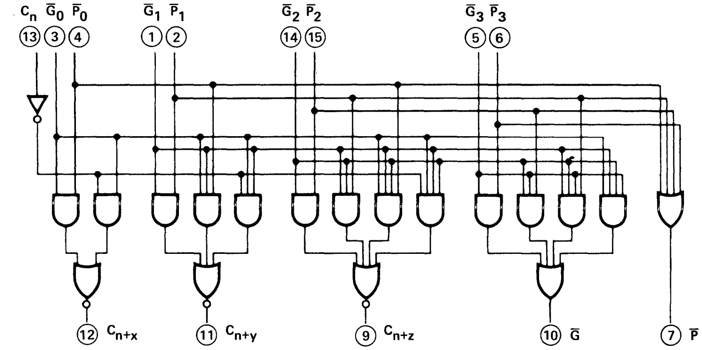
$$\overline{P} = \overline{P_3 \cdot P_2 \cdot P_1 \cdot P_0}$$

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, C_n to C_{n+x}, C_{n+y} or C_{n+z}		160			75			55		ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			160			75			55			
t_{PLH}	Propagation Delay, $\overline{P}_n$ to C_{n+x} C_{n+y} or C_{n+z}		160			75			55		ns	
t_{PHL}			160			75			55			
t_{PLH}	Propagation Delay, $\overline{G}_n$ to C_{n+x}, C_{n+y} or C_{n+z}		160			75			55		ns	
t_{PHL}			160			75			55			
t_{PLH}	Propagation Delay, $\overline{P}_n$ to $\overline{G}$ to $\overline{G}$		160			75			55		ns	
t_{PHL}			160			75			55			
t_{PLH}	Propagation Delay, $\overline{G}_n$ to $\overline{G}$		160			75			55		ns	
t_{PHL}			160			75			55			
t_{PLH}	Propagation Delay, $\overline{P}_n$ to $\overline{P}$		160			75			55		ns	
t_{PHL}			160			75			55			
t_{TLH}	Output Transition Time		60			30			20		ns	
t_{THL}			60			30			20			

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

4702B/4702BX

PROGRAMMABLE BIT-RATE GENERATOR

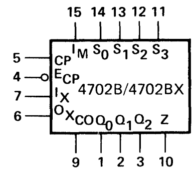
FAIRCHILD CMOS MACROLOGIC™

DESCRIPTION – The 4702B/4702BX Bit-Rate Generator provides the necessary clock signals for digital data transmission systems, such as Universal Asynchronous Receiver and Transmitter circuits (UARTs). It generates any of the 14 commonly used bit rates using an on-chip crystal oscillator, but its design also provides for easy and economical multi-channel operation, where any of the possible frequencies must be made available on any output channel.

One 4702B/4702BX can control up to eight output channels. When more than one bit-rate generator is required, they can still be operated from one crystal. The 4702B is specified to operate over a power supply voltage range of 5 V ± 10%. The 4702BX is a specially selected device specified to operate over a power supply voltage range of 4.5 V to 12.5 V.

- PROVIDES 14 COMMONLY USED BIT-RATES
- ONE 4702B/4702BX CONTROLS UP TO EIGHT TRANSMISSION CHANNELS
- USES 2.4576 MHz INPUT FOR STANDARD FREQUENCY OUTPUTS (16 TIMES BIT RATE)
- CONFORMS TO EIA RS-404
- ON-CHIP INPUT PULL UP CIRCUITS
- TTL COMPATIBLE-OUTPUTS WILL SINK 1.6 mA
- INITIALIZATION CIRCUIT FACILITIES DIAGNOSTIC FAULT ISOLATION
- LOW POWER DISSIPATION - 1.35 mA POWER DISSIPATION AT 5 V AND 2.4576 MHz
- 16-PIN DUAL IN-LINE PACKAGE

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

TABLE 1

CLOCK MODES AND INITIALIZATION

I_X	$\bar{E}_{CP}$	CP	OPERATION
⊓⊓⊓⊓	H	L	Clocked from I_X
X	L	⊓⊓⊓⊓	Clocked from CP
X	H	H	Continuous Reset
X	L	_⊓_	Reset During First CP = HIGH Time

H = HIGH Level
L = LOW Level
X = Don't Care
_⊓_ = 1st HIGH Level Clock Pulse After $\bar{E}_{CP}$ Goes LOW
⊓⊓⊓⊓ Clock Pulses

Note 1: Actual output frequency is 16 times the indicated output rate, assuming a clock frequency of 2.4576 MHz.

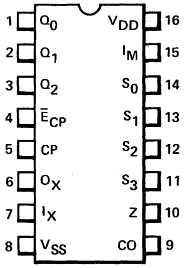
TABLE 2

TRUTH TABLE FOR RATE SELECT INPUTS

S_3	S_2	S_1	S_0	Output Rate (Z) Note 1
L	L	L	L	Multiplexed Input (I_M)
L	L	L	H	Multiplexed Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

L = LOW Level
H = HIGH Level

CONNECTION DIAGRAM
DIP (TOP VIEW)

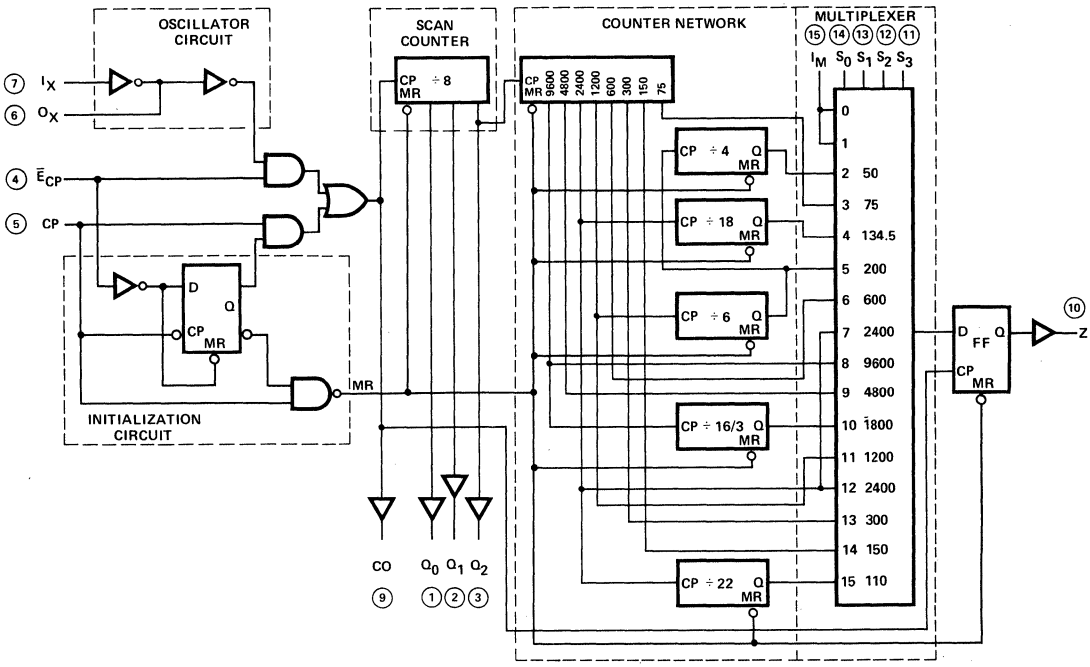


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

CP	External Clock Input
$\bar{E}_{CP}$	External Clock Enable Input (Active LOW)
I_X	Crystal Input
I_M	Multiplexed Input
S_0-S_3	Rate Select Inputs
CO	Clock Output
O_X	Crystal Drive Output
Q_0-Q_2	Scan Counter Outputs
Z	Bit Rate Output

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

FUNCTIONAL DESCRIPTION — Digital data transmission systems employ a wide range of standardized bit rates, ranging from 50 baud interfacing with electromechanical devices, to 9600 baud for high speed modems. Modern electronic systems commonly use Universal Asynchronous Receiver and Transmitter circuits (UARTs) to convert parallel data inputs into a serial bit stream (transmitter) and to reconvert the serial bit stream into parallel outputs (receiver). In order to resynchronize the incoming serial data, the receiver requires a clock rate that is a multiple of the incoming bit rate. Popular MOS-LSI UART circuits use a clock that is 16 times the transmitted bit rate. The 4702B/4702BX can generate 14 standardized clock rates from one commonly high frequency input.

The 4702B/4702BX contains the following five functional subsystems which are discussed in detail below:

1. An Oscillator Circuit with associated gating.
2. A prescaler used as Scan Counter for multichannel operation (described in the applications section).
3. A Counter Network to generate the required standardized frequencies.
4. An output Multiplexer (frequency selector) with resynchronizing output flip-flop.
5. An Initialization (reset) Circuit.

Oscillator — For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576 MHz (i.e. 9600 baud x 16 x 16, since the scan counter and the first flip-flop of the counter chain act as an internal ÷ 16 prescaler). A lower input frequency will obviously result in a proportionally lower output frequency.

The 4702B/4702BX can be driven from two alternate clock sources: (1) When the E_{CP} (active LOW External Clock Enable) input is LOW, the CP input is the clock source. (2) When the E_{CP} input is HIGH, a crystal connected between I_X and O_X, or a signal applied to the I_X input, is the clock source.

Prescaler (Scan Counter) — The clock frequency is made available on the CO (Clock Output) pin and is applied to the ÷ 8 prescaler with buffered outputs Q_0, Q_1, and Q_2. This prescaler is of no particular advantage in single frequency applications, but it is essential for the simple economical multichannel scheme described in the Applications section of this data book.

Counter Network — The prescaler output Q_2 is a square wave of 1/8 the input frequency and is used to drive the frequency counter network generating 13 standardized frequencies. Note that the frequencies are labeled in the block diagram and described in terms of the transmission bit rate. In a conventional system using a 2.4576 MHz clock input, the actual output frequencies are 16 times higher.

The output from the first frequency divider flip-flop is thus labeled 9600, since it is used to transmit or receive 9600 baud (bits per second). The actual frequency at this node is 16 x 9.6 kHz = 153.6 kHz. Seven more cascaded binaries generate the appropriate frequencies for bit rates 4800, 2400, 1200, 600, 300, 150, and 75.

The other five bit rates are generated by individual counters:

bit rate 1200 is divided by 6 to generate bit rate 200,
bit rate 200 is divided by 4 to generate bit rate 50,
bit rate 2400 is divided by 18 to generate bit rate 134.5 with a frequency error of –0.87%,
bit rate 2400 is also divided by 22 to generate bit rate 110 with a frequency error of –0.83%, and
bit rate 9600 is divided by 16/3 to generate bit rate 1800.

The 16/3 division is accomplished by alternating the divide ratio between 5 (twice) and 6 (once). The result is an exact average output frequency with some frequency modulation. Taking advantage of the ÷ 16 feature of the UART, the resulting distortion is less than 0.78%, irrespective of the number of elements in a character, and therefore well within the timing accuracy specified for high speed communications equipment. All signals except 1800, have a 50% duty cycle.

Output Multiplexer — The outputs of the counter network are fed to a 16-input multiplexer, which is controlled by the Rate Select inputs (S_0-S_3). The multiplexer output is then resynchronized with the incoming clock in order to cancel all cumulative delays and to present an output signal at the buffered output (Z) that is synchronous with the prescaler outputs (Q_0-Q_2). *Table 2* lists the correspondence between select code and output bit rate. Two of the 16 codes do not select an internally generated frequency, but select an input into which the user can feed either a different, nonstandardized frequency, or a static level (HIGH or LOW) to generate "zero baud".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 baud) require that no more than one input be grounded, easily achieved with a single pole, 5-position switch. 2400 baud is selected by two different codes, so that the whole spectrum of modern digital communication rates has a common HIGH on the S_3 input.

Initialization (Reset) — The initialization circuit generates a common master reset signal for all flip-flops in the 4702B/4702BX. This signal is derived from a digital differentiator that senses the first HIGH level on the CP input after the $\overline{E}_{CP}$ input goes LOW. When $\overline{E}_{CP}$ is HIGH, selecting the Crystal input, CP must be LOW. A HIGH level on CP would apply a continuous reset.

All inputs to the 4702B/4702BX, except I_X have on-chip pull-up circuits which improve TTL compatibility and eliminate the need to tie a permanently HIGH input to V_{DD}.

DC CHARACTERISTICS: V_{DD} = 5 V, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS			UNITS	TEMP	TEST CONDITIONS	
			MIN	TYP	MAX				
V_{IH}	Input HIGH Voltage		3.5			V	All	Guaranteed Input High Voltage	
V_{IL}	Input LOW Voltage				1.5	V	All	Guaranteed Input LOW Voltage	
V_{OH}	Output HIGH Voltage		4.95			V	MIN, 25°C	$I_{OH} < 1$ µA, Inputs at 0 or 5 V per the Logic Function or Truth Table	
			4.95				MAX		
			4.5			V	All	$I_{OH} < 1$ µA, Inputs at 1.5 or 3.5 V	
V_{OL}	Output LOW Voltage				0.05	V	MIN, 25°C	$I_{OL} < 1$ µA, Inputs at 0 or 5 V per the Logic Function or Truth Table	
					0.05		MAX		
					0.5	V	All	$I_{OL} < 1$ µA, Inputs at 1.5 or 3.5 V	
I_L (See Note 1)	Input LOW Current for Input I_X	XC			0.3	µA	MIN, 25°C	Pin under Test at 0 V All other Inputs Simultaneously at 5 V	
					1		MAX		
		XM			0.1	µA	MIN, 25°C		
					1		MAX		
	Input LOW Current for all Other Inputs	XC	-15	–30	-100	µA	25°C		
		XM	-15	–30	-100				
I_{IH}	Input HIGH Current for all Inputs	XC			0.3	µA	MIN, 25°C	Pin Under Test at 5 V All other Inputs Simultaneously at 0 V	
					1		MAX		
		XM			0.1	µA	MIN, 25°C		
					1		MAX		
I_{OH}	Output HIGH Current for Output O_X		–0.3			mA	MIN, 25°C	V_{OUT} = 4.5 V	Inputs at 0 or 5 V per Logic Function or Truth Table
			–0.1				MAX		
	Output HIGH Current for all other Outputs		–1.5			mA	MIN, 25°C	V_{OUT} = 2.5 V	
			–1				MAX		
			–0.5			mA	MIN, 25°C	V_{OUT} = 4.5 V	
			–0.3				MAX		
I_{OL}	Output LOW Current for Output O_X		0.2			mA	MIN, 25°C	V_{OUT} = 0.4 V	
			0.1				MAX		
	Output LOW Current for all Other Outputs		3.2			mA	MIN, 25°C		
			1.6				MAX		
I_{DD}	Quiescent Power Supply Current	XC			100	µA	MIN, 25°C	$\overline{E}_{CP} = V_{DD}$, CP = 0 V, All other Inputs at 0 V or V_{DD} (Note 6)	
					1000		MAX		
		XM			10	µA	MIN, 25°C		
					150		MAX		

See Notes on following page.

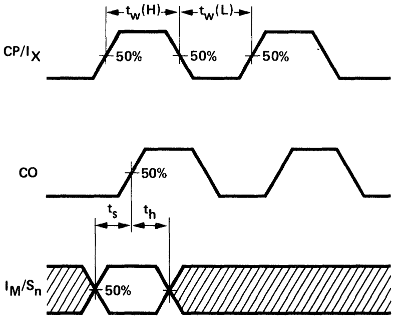
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: $V_{DD} = 5\ V$, $V_{SS} = 0\ V$, $T_A = 25^\circ C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Propagation Delay		175	350	ns	$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ≤ 20 ns $C_L \leqslant 7$ pF on O_X
t_{PHL}	I_X to CO		135	275		
t_{PLH}	Propagation Delay		130	260	ns	
t_{PHL}	CP to CO		110	220		
t_{PLH}	Propagation Delay		53	Note 5	ns	
t_{PHL}	CO to Q_n		45			
t_{PLH}	Propagation Delay		37	85	ns	
t_{PHL}	CO to Z		32	75		
t_{TLH}	Output Transition		80	160	ns	
t_{THL}	Time (Except O_X)		35	75		
t_s	Set-Up Time, Select to CO	350	185		ns	
t_h	Hold Time, Select to CO		−182			
t_s	Set-Up Time, I_M to CO	350	190		ns	
t_h	Hold Time, I_M to CO	0	−182			
$t_wCP(L)$	Minimum Clock Pulse Width	120	60		ns	
$t_wCP(H)$	LOW and HIGH	120	60			
$t_wI_X(L)$	Minimum I_X Pulse Width	160	75		ns	
$t_wI_X(H)$	LOW and HIGH	160	75			

NOTES:

1. Propagation Delays and Output Transition Times are graphically described under 4000B Series CMOS Family Characteristics.
2. The first HIGH level Clock Pulse after $\overline{E}_{CP}$ goes LOW must be at least 350 ns long to guarantee reset of all Counters.
3. It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15 μs at $V_{DD} = 5$ V, 4 μs at $V_{DD} = 10$ V, and 3 μs at $V_{DD} = 15$ V, and the V_{DD} pin should be decoupled.
4. Input current and quiescent power supply current are relatively higher for this device because of active pull-up circuits on all inputs except I_X. This is done for TTL compatibility.
5. For multichannel operation, propagation delay, CO to Q_n, plus set-up time, select to CO, is guaranteed to ≤ 367 ns.
6. I_{DD} is measured on Pin 8 and does not include Input Leakage Currents.

SWITCHING WAVEFORMS



MINIMUM CP AND I_X PULSE WIDTHS AND SET-UP AND HOLD TIMES,
SELECT INPUT (S_n) TO CLOCK OUTPUT (CO) AND I_M INPUT TO CLOCK OUTPUT (CO)

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

APPLICATIONS

Single Channel Bit Rate Generator — *Figure 1* shows the simplest application of the 4702B/4702BX. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The bit rate output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 Baud. For many low cost terminals these five bit rates are adequate.

Simultaneous Generation of Several Bit Rates:
Fixed Programmed Multichannel Operation — *Figure 2* shows a simple scheme that generates eight bit rates on eight output lines, using one 4702B/4702BX and one 93L34 8-Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter outputs back to the Select inputs of the multiplexer causes the 4702B/4702BX to interrogate sequentially the state of eight different frequency signals. The 93L34 8-Bit Addressable Latch, addressed by the same Scan Counter outputs, reconverts the multiplexed single output (Z) of the 4702B/4702BX into eight parallel output frequency signals. In the simple scheme of *Figure 2*, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0: 110 Baud, Q_1: 9600 Baud, Q_2: 4800 Baud, Q_3: 1800 Baud,
Q_4: 1200 Baud, Q_5: 2400 Baud, Q_6: 300 Baud, Q_7: 150 Baud.

Other bit rate combinations can be generated by changing the Scan Counter to selector interconnection or by inserting logic gates into this path.

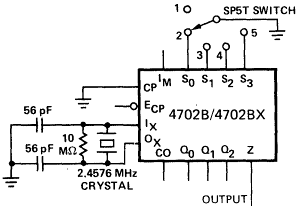
Fully Programmable Multichannel Operation — *Figure 3* shows a fully programmable 8-channel bit rate generator system that, under computer control, generates arbitrarily assigned bit rates on all eight outputs simultaneously. The basic operation is similar to the previously described fixed programmed system, but two 9LS170 4 x 4 Register File MSI packages are connected as programmable look-up tables between the Scan Counter outputs (Q_0 to Q_2) and the multiplexer Select inputs (S_0 to S_3). The content of this 8-word by 4-bit memory determines which frequency appears at what output.

19200 Baud Operation — Though a 19200 Baud signal is not internally routed to the multiplexer, the 4702B/4702BX can be used to generate this bit rate by connecting the Q_2 output to the I_M input and applying select code 0 or 1. An additional 2-input NAND gate can be used to retain the "Zero Baud" feature on select code 0. Any multichannel operation that involves 19200 Baud must be limited to four outputs as shown in *Figure 4.* Only the two least significant Scan Counter outputs are used, so that the scan is completed within one half period of the 19200 output frequency.

Clock Expansion — One 4702B/4702BX can control up to eight output channels. For more than eight channels, additional bit rate generators are required. These bit rate generators can all be run from the same crystal or clock input. *Figure 5* shows one possible expansion scheme. One 4702B/4702BX is provided with a crystal. All other devices derive their clock from this master. *Figure 6* shows a different scheme where the master clock output feeds into the I_X input of all slaves and all E_{CP} inputs are normally held HIGH. This scheme retains the reset feature and the selection between two different clock sources of the basic 4702B/4702BX circuit.

During normal operation, the common E_{CP} line is HIGH and the common clock line (CP) is LOW. For diagnostic purposes the common E_{CP} is forced LOW. This deselects the crystal frequency and initiates the diagnostic mode. When CP goes HIGH for the first time, all 4702B/4702BXs are reset through their individual on-chip initialization circuitry. Subsequent LOW-to-HIGH clock transitions on the common CP line advance the scan counter, causing all 4702B/4702BXs to operate synchronously.

TYPICAL APPLICATIONS



SWITCH POSITION	BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

Fig. 1
SWITCH SELECTABLE BIT RATE GENERATOR CONFIGURATION PROVIDING FIVE BIT RATES

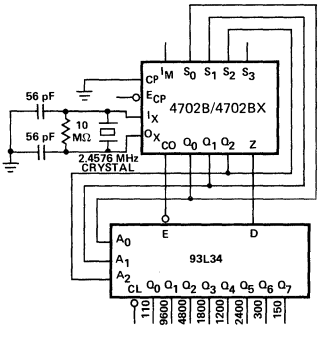


Fig. 2
BIT RATE GENERATOR CONFIGURATION WITH EIGHT SIMULTANEOUS FREQUENCIES

TYPICAL APPLICATIONS (Cont'd)

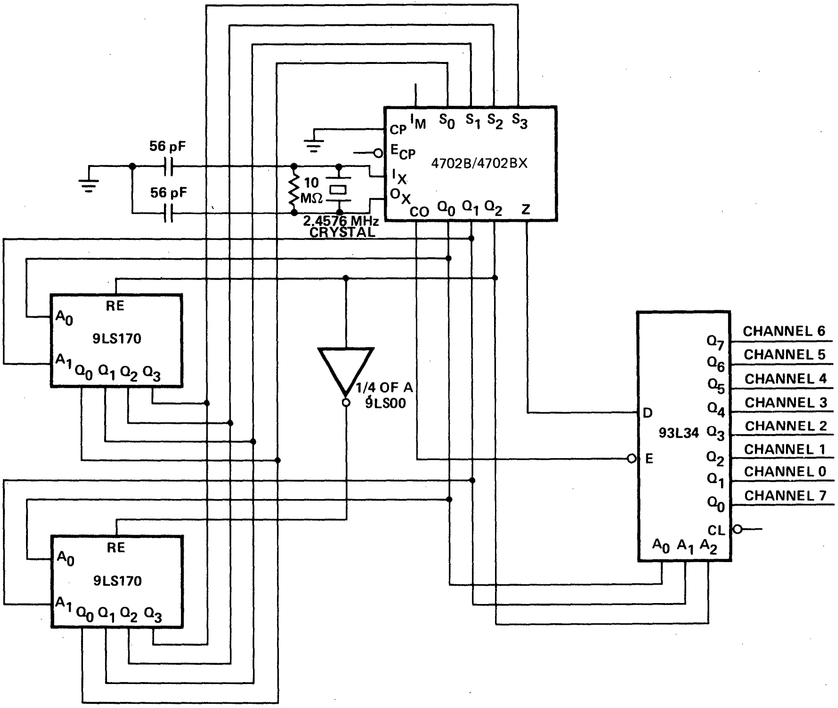


Fig. 3

FULLY PROGRAMMABLE 8-CHANNEL BIT RATE GENERATOR SYSTEM

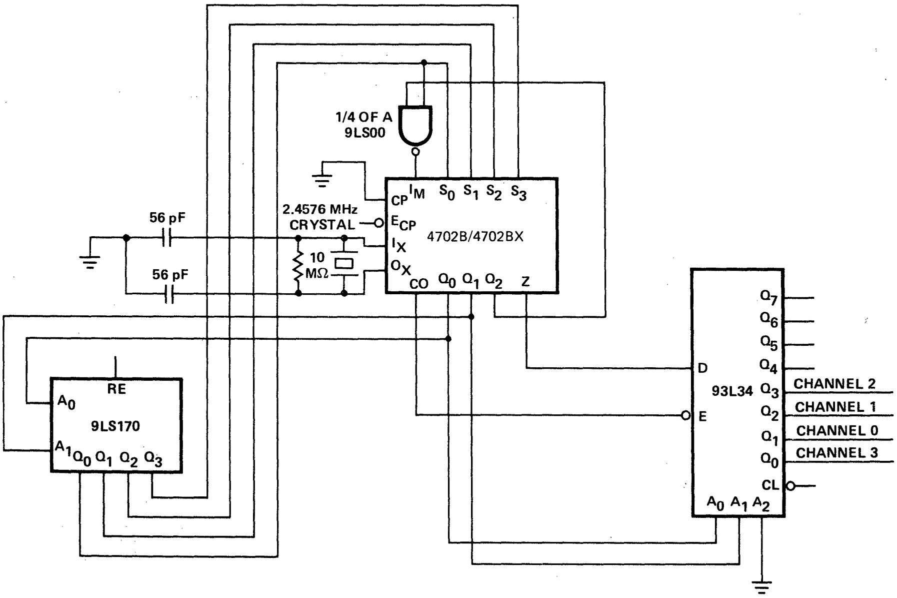


Fig. 4

FULLY PROGRAMMABLE 4-CHANNEL BIT RATE GENERATOR SYSTEM WITH THE 19.2k BAUD FEATURE

TYPICAL APPLICATIONS (Cont'd)

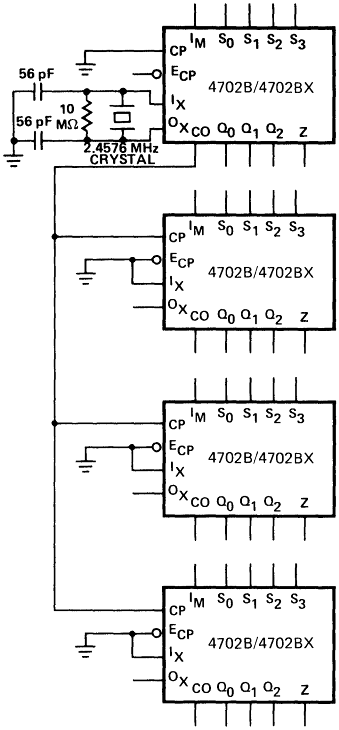


Fig. 5
CASCADE CLOCK EXPANSION SCHEME

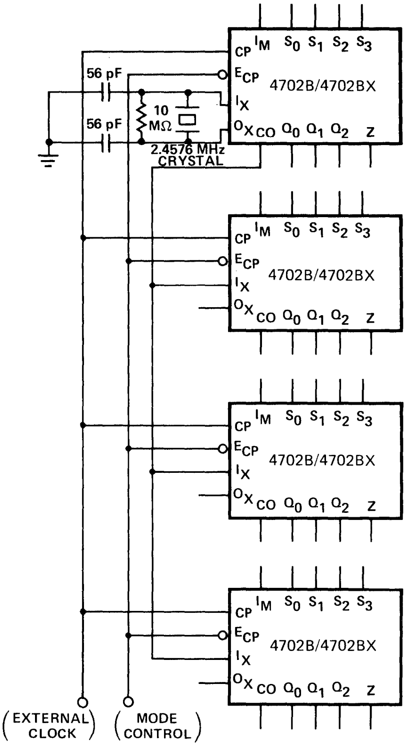


Fig. 6
TANDEM CLOCK EXPANSION SCHEME

CRYSTAL SPECIFICATION RECOMMENDATIONS — Table 3 is a convenient listing of recommended crystal specifications. Crystal manufacturers are also listed below.

TABLE 3 CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576 MHz "AT" Cut
Series Resistance (Max)	250 Ω
Unwanted Modes	−6 dB (Min)
Type of Operation	Parallel
Load Capacitance	32 pF ±0.5

CRYSTAL MANUFACTURERS

CTS Knights, Inc.
Sandwich, Ill. 60548
(815) 786-8411
Crystal #F1004

X - Tron Electronics
1869 National Ave.
Hayward, Calif.
(415) 783-2145

Erie Frequency Control
499 Lincoln St.
Carlisle, Pa. 17013
(717) 249-2232

International Crystal Mfg. Company
10 No. Lee
Oklahoma City, Okla. 73102
(405) 236-3741

Sentry Manufacturing Co.
Crystal Park
Chickasha, Oklahoma 73018
(405) 224-6780
Crystal # SGP 6-2.4576 or
Crystal # SGP-7-2.4576

4703B/4703BX

FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY

FAIRCHILD CMOS MACROLOGIC™

DESCRIPTION – The 4703B/4703BX is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 16 words by four bits and may be expanded to any number of words or any number of bits (in multiples of four). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 4703B/4703BX has 3-state outputs which provide added versatility and is fully compatible with all CMOS families.

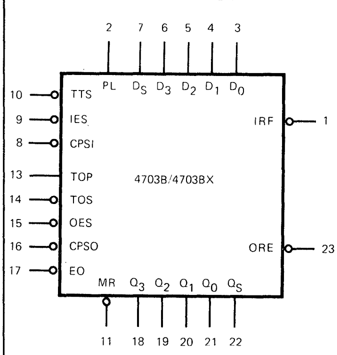
The 4703B is specified to operate over a power supply voltage range of 4.5 V to 12.5 V and the 4703BX is specified to operate over a power supply voltage range of 3 V to 15 V.

- **5.3 MHz SERIAL OR PARALLEL DATA RATE, TYPICALLY AT V_{DD} = 10 V**
- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE OUTPUTS**
- **FULLY COMPATIBLE WITH ALL CMOS FAMILIES**
- **SLIM 24-PIN PACKAGE**

PIN NAMES

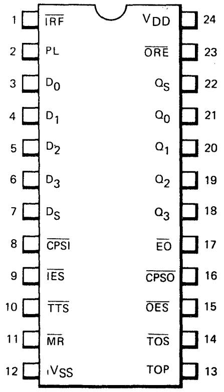
D_0–D_3	Parallel Data Inputs
D_S	Serial Data Input
PL	Parallel Load Input
$\overline{CPSI}$	Serial Input Clock Input (HIGH-to-LOW Triggered)
$\overline{CPSO}$	Serial Output Clock Input (HIGH-to-LOW Triggered)
$\overline{IES}$	Serial Input Enable (Active LOW)
$\overline{TTS}$	Transfer to Stack Input (Active LOW)
$\overline{TOS}$	Transfer Out Serial Input (Active LOW)
TOP	Transfer Out Parallel Input
$\overline{OES}$	Serial Output Enable Input (Active LOW)
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{MR}$	Master Reset Input (Active LOW)
$\overline{IRF}$	Input Register Full Output (Active LOW)
$\overline{ORE}$	Output Register Empty Output (Active LOW)
Q_0–Q_3	Parallel Data Outputs
Q_S	Serial Data Output

LOGIC SYMBOL



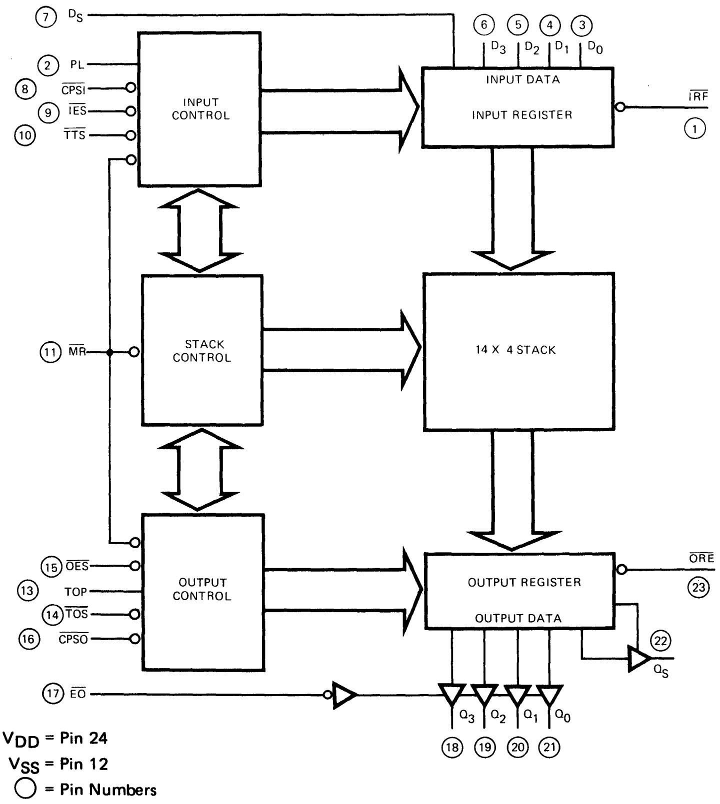
V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – As shown in the block diagram the 4703B/4703BX consists of three sections:

1. An Input Register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 14-word deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

Input Register (Data Entry):
The Input Register can receive data in either bit-serial or in 4-bit parallel form. It stores this data until it is sent to the fall-through stack and generates the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section, as described later, this 5-bit register is initialized by setting the F3 flip-flop and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

Parallel Entry – A HIGH on the PL input loads the D_0–D_3 inputs into the F_0–F_3 flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW indicating that the input register is full. During parallel entry, the $\overline{CPSI}$ input must be LOW. If parallel expansion is not being implemented, $\overline{IES}$ must be LOW to establish row mastership (see Expansion section). The D_0–D_3 inputs are "ones catching" and must remain stable while PL is HIGH.

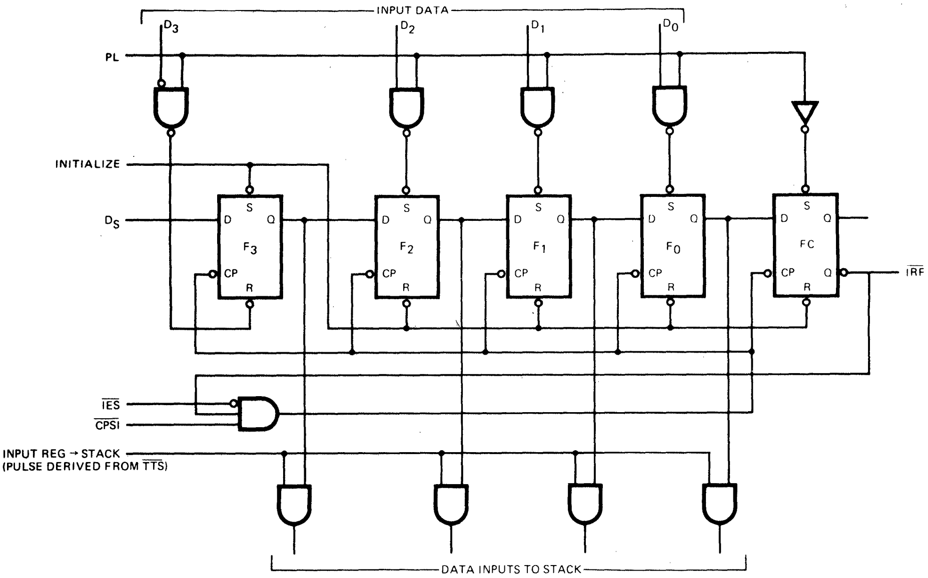


Fig. 1
CONCEPTUAL INPUT SECTION

Serial Entry — Data on the D_S input is serially entered into the F_3, F_2, F_1, F_0, FC shift register on each HIGH-to-LOW transition of the $\overline{CPSI}$ clock input, provided $\overline{IES}$ and PL are LOW.

After the fourth clock transition, the four data bits located in the four flip-flops F_0—F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ clock pulses from effecting the register. *Figure 2* illustrates the final positions in a 4703B/4703BX resulting from a 64-bit serial bit train. B_0 is the first bit, B_{63} the last bit.

Transfer to the Stack — The outputs of Flip-Flops F_0—F_3 feed the stack. A LOW level on the $\overline{TTS}$ input initiates a "fall-through" action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS Flip-Flop (the Request Initialization Flip-Flop shown in *Figure 10*) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack despite the fact the $\overline{IRF}$ and $\overline{TTS}$ may still be LOW. The Request Initialization Flip-Flop is not cleared until PL goes LOW. Once in the stack, data falls through the stack automatically, pausing only when it is necessary to wait for an empty next location. In the 4703B/4703BX, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the stack control section and does not clear the data.

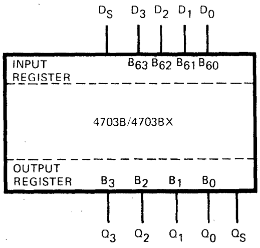


Fig. 2
FINAL POSITIONS IN A 4703B/4703BX RESULTING FROM A 64-BIT SERIAL TRAIN

Output Register (Data Extraction) – The Output Register receives 4-bit data words from the bottom stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. *Figure 3* is a conceptual logic diagram of the output section.

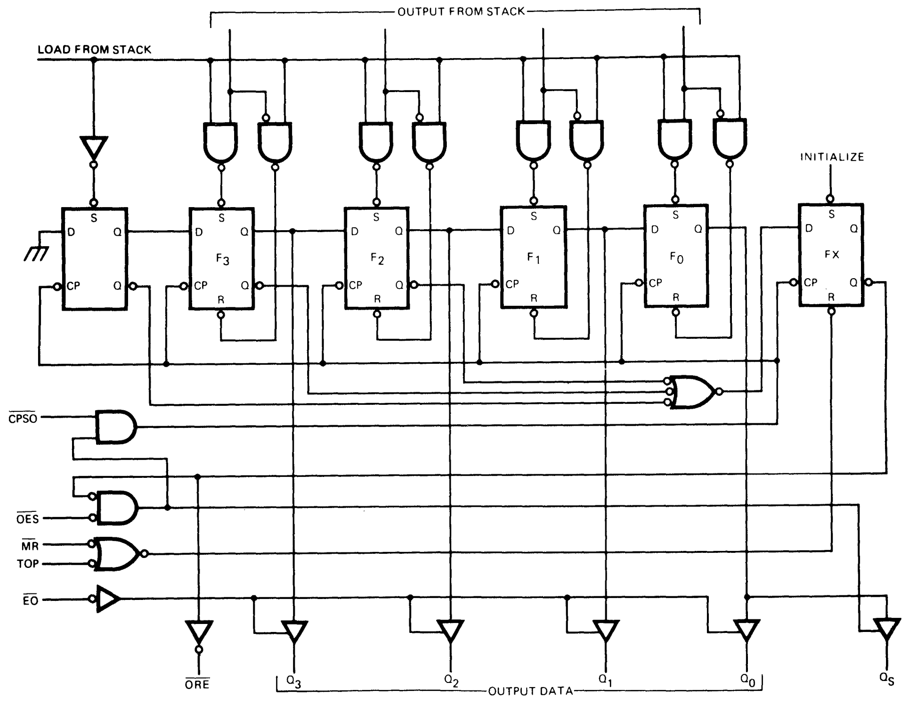


Fig. 3
CONCEPTUAL OUTPUT SECTION

Parallel Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{\text{MR}}$, the Output Register Empty ($\overline{\text{ORE}}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided the "Transfer Out Parallel" (TOP) input is HIGH. As a result of the data transfer $\overline{\text{ORE}}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{\text{ORE}}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next HIGH level at TOP permits the transfer of the next word (if available) into the Output Register. During parallel data extraction $\overline{\text{CPSO}}$ should be LOW. $\overline{\text{TOS}}$ should be grounded for single slice operation or connected to the appropriate $\overline{\text{ORE}}$ for expanded operation (see Expansion section).

TOP is not edge triggered. Therefore, if TOP goes HIGH before data is available from the stack, but data does become available before TOP goes LOW again, that data will be transferred into the Output Register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, $\overline{\text{ORE}}$ remains LOW indicating that there is no valid data at the outputs.

Serial Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{\text{MR}}$, the Output Register Empty ($\overline{\text{ORE}}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided $\overline{\text{TOS}}$ is LOW and TOP is HIGH. As a result of the data transfer $\overline{\text{ORE}}$ goes HIGH indicating valid data in the register. The 3-state Serial Data Output, Q_S, is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{\text{CPSO}}$. To prevent false shifting, $\overline{\text{CPSO}}$ should be LOW when the new word is being loaded into the Output Register. The fourth transition empties the shift register, forces $\overline{\text{ORE}}$ output LOW and disables the serial output, Q_S (refer to *Figure 3*). For serial operation the $\overline{\text{ORE}}$ output may be tied to the $\overline{\text{TOS}}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

EXPANSION

Vertical Expansion — The 4703B/4703BX may be vertically expanded to store more words without external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in *Figure 4*. Using the same technique, any FIFO of (15n + 1) words by four bits can be constructed, where n is the number of devices. Note that expansion does not sacrifice any of the 4703B/4703BX's flexibility for serial/parallel input and output. For other expansion schemes, refer to the Applications section of this book.

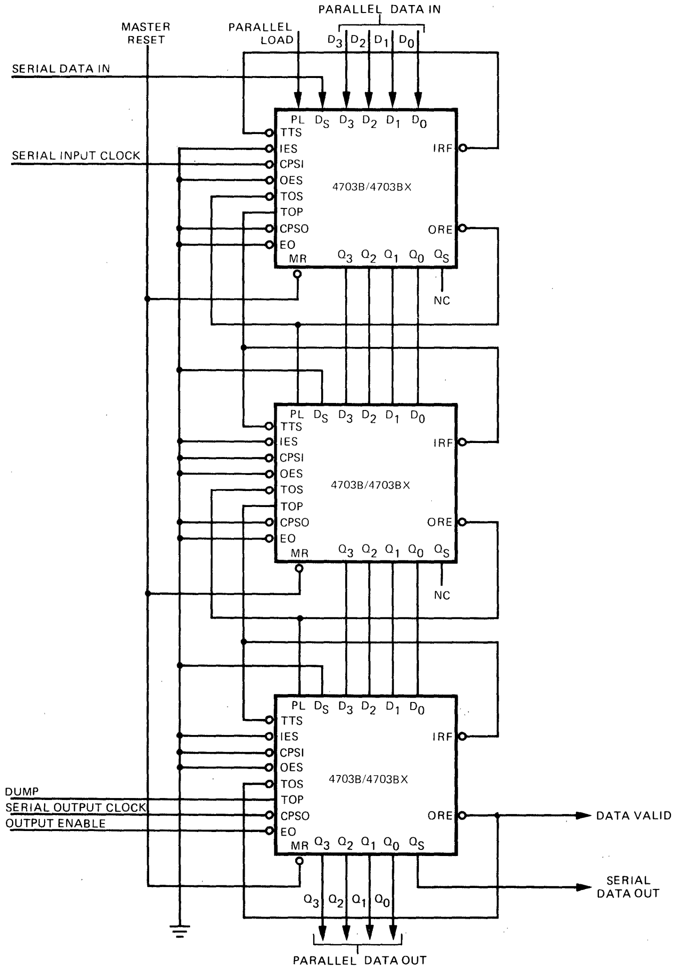


Fig. 4
A VERTICAL EXPANSION SCHEME

Horizontal Expansion – The 4703B/4703BX can also be horizontally expanded to store long words (in multiples of four bits) without external logic. The interconnections necessary to form a 16-word by 12-bit FIFO are shown in *Figure 5*. Using the same technique, any FIFO of 16 words by 4n bits can be constructed, where n is the number of devices. The $\overline{\text{IRF}}$ output of the right most device (most significant device) is connected to the $\overline{\text{TTS}}$ inputs of all devices. Similarly, the $\overline{\text{ORE}}$ output of the most significant device is connected to the $\overline{\text{TOS}}$ inputs of all devices. As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the 4703B/4703BX's flexibility for serial/parallel input and output.

It should be noted that this form of horizontal expansion extracts a penalty in speed. A single FIFO is guaranteed to operate at 3.4 MHz; an array of four FIFOs connected in the above manner is guaranteed at 1.5 MHz. An expansion scheme that provides higher speed but requires additional components is shown in the Applications section of this book.

Horizontal and Vertical Expansion – The 4703B/4703BX can be expanded in both the horizontal and vertical directions without any external parts and without sacrificing any of its FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in *Figure 6*. Using the same technique, any FIFO of (15m + 1) words by (4n) bits can be constructed, where m is the number of devices in a column and n is the number of devices in a row.

Figures 7 and *8* show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in *Figure 6*. The final position of data after serial insertion of 496 bits into the FIFO array of *Figure 6* is shown in *Figure 9*.

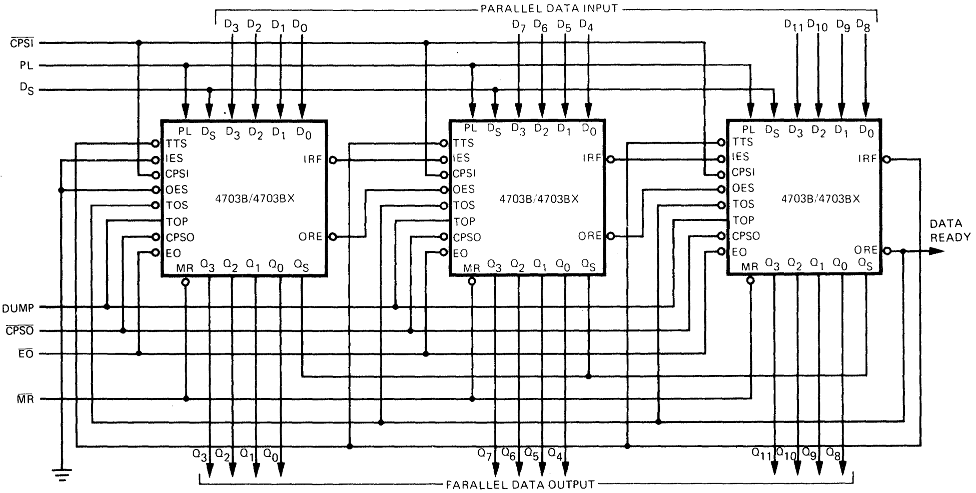


Fig. 5
A HORIZONTAL EXPANSION SCHEME

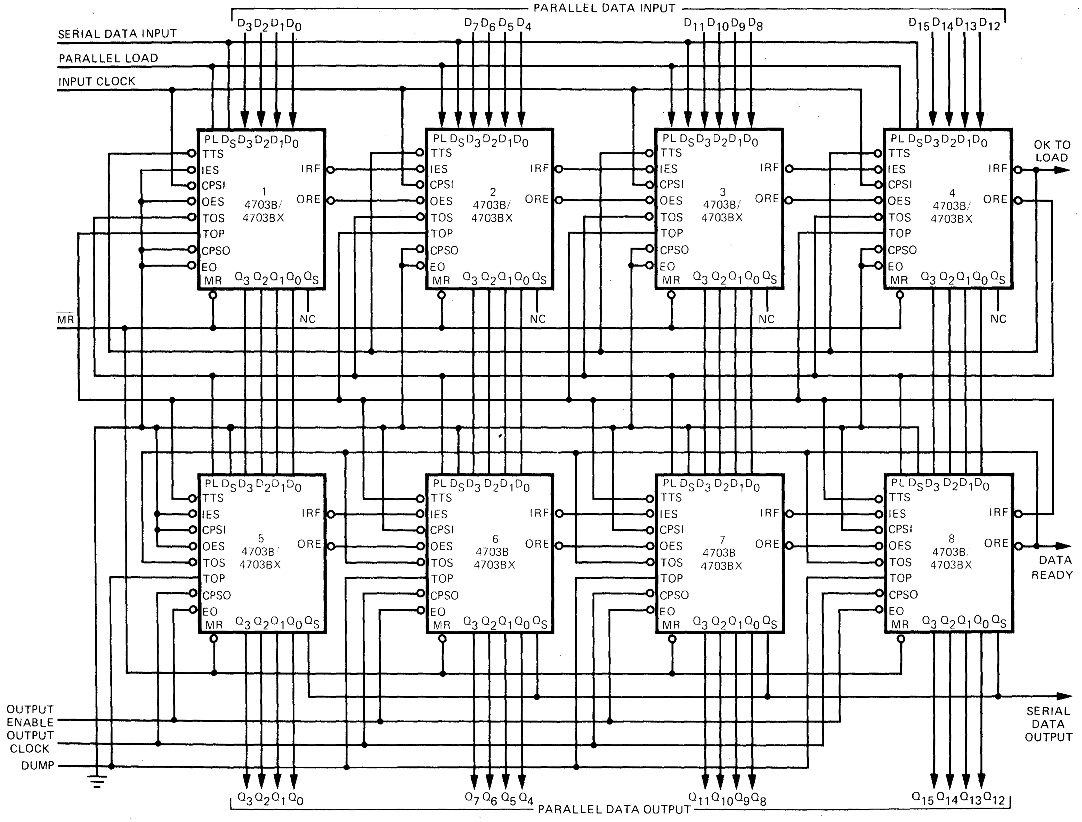


Fig. 6
A 31 X 16 FIFO ARRAY

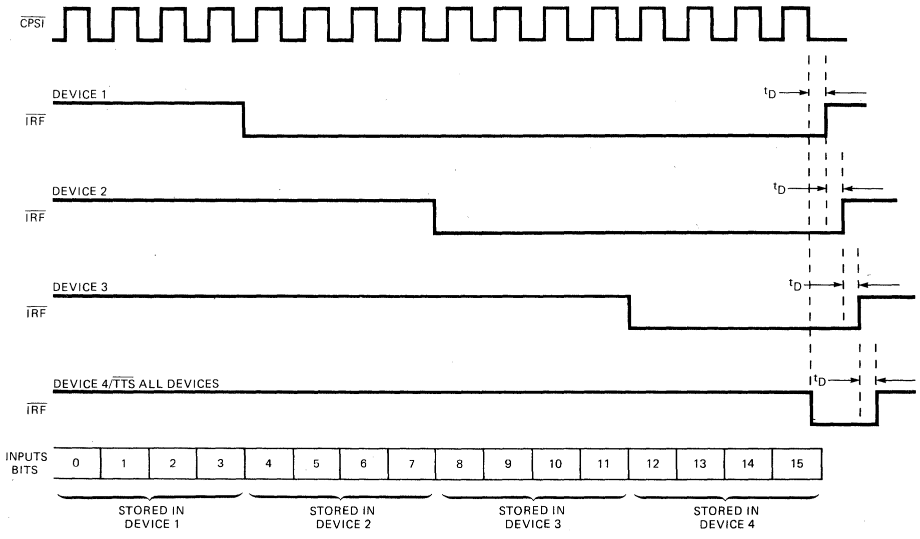


Fig. 7
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

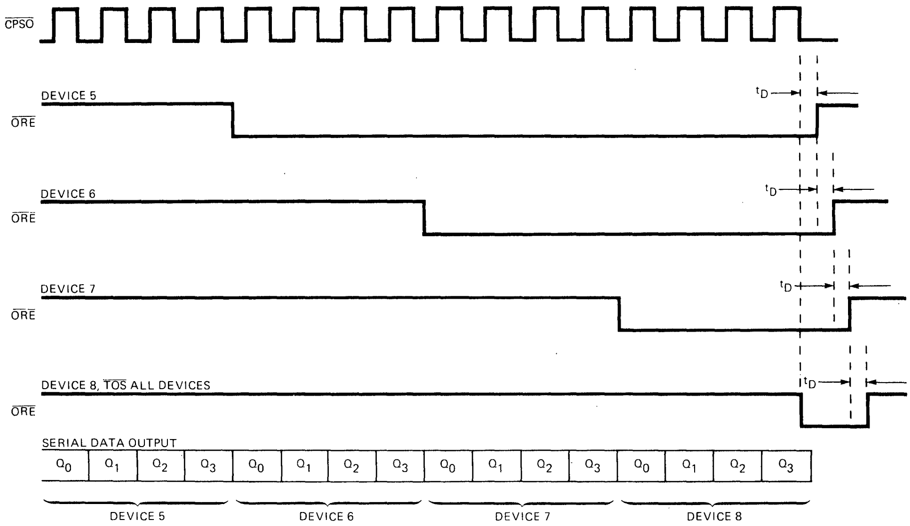


Fig. 8
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

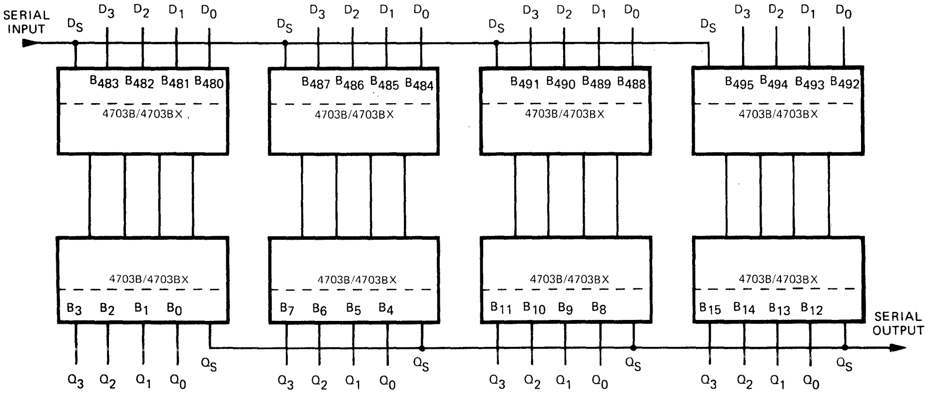


Fig. 9
FINAL POSITION OF A 496-BIT SERIAL INPUT

Interlocking Circuitry – Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 4703B/4703BX incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the 4703B/4703BX array of *Figure 6* devices 1 and 5 are defined as "row masters" and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{IES}$ input from a row, master or a slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes LOW and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of 4703B/4703BX FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization. *Figure 10* is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the Master Latch is set. Whenever $\overline{TTS}$ goes LOW the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop reset. If the Master Latch is reset, the Input Register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the ORE Request Flip-Flop. If the Master Latch is set, the last Output Register Flip-Flop is set and $\overline{ORE}$ goes HIGH. If the Master Latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

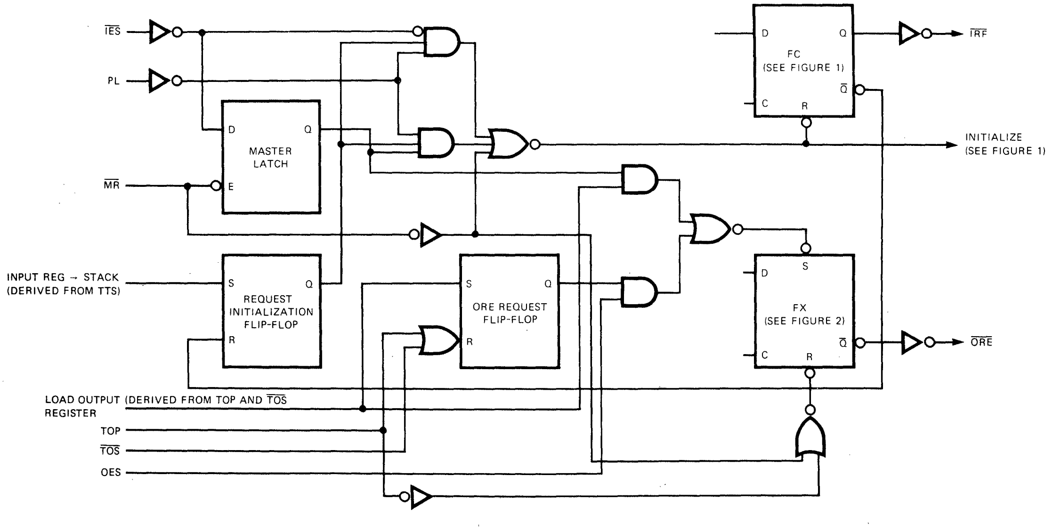


Fig. 10
CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF HIGH Current	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO} = V_{DD}$
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF LOW Current	XC									−1.6	μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO} = V_{DD}$
											−12		MAX	
		XM									−0.4		MIN, 25°C	
											−12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			32.5			65			130	μA	MIN, 25°C	All Inputs at 0 V or V_{DD}
					250			500			1000		MAX	
		XM			8.75			17.5			35	μA	MIN, 25°C	
					250			500			1000		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25^{\circ}$C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PHL}	Propagation Delay, $\overline{CPSI}$ to $\overline{IRF}$		215	430		81	162		57	114	ns	$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ⩽ 20 ns
t_{PLH}	Propagation Delay, $\overline{TTS}$ to $\overline{IRF}$		439	878		131	262		92	184	ns	
t_{PLH}	Propagation Delay, $\overline{CPSO}$ to Q_S		306	612		68	136		48	96	ns	
t_{PHL}			299	598		79	158		56	112		
t_{PLH}	Propagation Delay, TOP to Q_n		325	650		128	256		90	180	ns	
t_{PHL}			293	586		114	228		80	160		

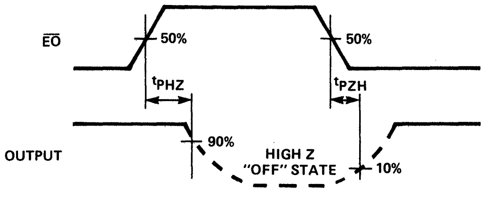
Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS (Cont'd): V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25^oC$

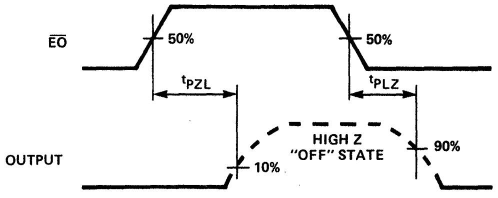
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PHL}	Propagation Delay, $\overline{CPSO}$ to $\overline{ORE}$		159	318		74	148		52	104	ns	
t_{PLH}	Propagation Delay, $\overline{TOS}$ to $\overline{ORE}$		320	640		114	228		80	160	ns	
t_{PLH} t_{PHL}	Propagation Delay, TOP to $\overline{ORE}$		401 256	802 512		134 109	268 218		94 77	188 154	ns	$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ≤ 20 ns
t_{PHL}	Propagation Delay, PL to $\overline{IRF}$		119	238		44	88		31	62	ns	
t_{FT}	Fall Through Time		2020	4040		820	1640		574	1148	ns	
t_{PZH} t_{PZL}	Output Enable Time		51 85	102 170		24 33	48 66		17 24	34 48	ns	($R_L = 1$ kΩ to V_{SS}) ($R_L = 1$ kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time		64 80	128 160		34 39	68 78		24 28	48 56	ns	($R_L = 1$ kΩ to V_{SS}) ($R_L = 1$ kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time		46 34	92 68		25 18	50 36		18 13	36 26	ns	
$t_W\overline{CP}(H)$	Min $\overline{CPSI}$ Pulse Width (HIGH)	118	59		44	22		31	16		ns	
$t_W\overline{CP}(L)$	Min $\overline{CPSI}$ Pulse Width (LOW)	220	110		108	54		76	38		ns	
$t_W\overline{CP}(L)$	Min $\overline{CPSO}$ Pulse Width (LOW)	120	60		60	30		42	21		ns	
$t_W\overline{CP}(H)$	Min $\overline{CPSO}$ Pulse Width (HIGH)	110	55		72	36		51	26		ns	
$t_WPL(H)$	Min PL Pulse Width (HIGH)	122	61		44	22		31	16		ns	
$t_W\overline{TTS}(L)$	Min $\overline{TTS}$ Pulse Width (LOW)	160	80		124	62		87	44		ns	
$t_W\overline{TOS}(L)$	Min $\overline{TOS}$ Pulse Width (LOW)	182	91		60	30		42	21		ns	
$t_WTOP(L)$	Min TOP Pulse Width (LOW)	142	71		52	26		37	19		ns	
$t_W\overline{MR}(L)$	Min $\overline{MR}$ Pulse Width (LOW)	192	96		108	54		76	38		ns	
t_{rec}	$\overline{MR}$ Recovery Time	44	22		36	18		26	13		ns	
t_s t_h	Set-Up and Hold Times, D_s to $\overline{CPSI}$	104 −8	52 −15		40 24	20 12		28 18	14 9		ns	
t_s t_h	Set-Up and Hold Times, $\overline{TTS}$ to $\overline{IRF}$, Serial or Parallel Mode	186 76	93 38		98 52	49 26		70 38	35 19		ns	
t_s	Set-Up Time, $\overline{ORE}$ to $\overline{TOS}$	−151	−302		−21	−42		−15	−30		ns	
f_{MAX}	Input CLOCK Frequency (Note 2)	1.1	2.3		2.6	5.3		3.4	6.9		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at $V_{DD} = 5$ V, 4 μs at $V_{DD} = 10$ V, and 3 μs at $V_{DD} = 15$ V.

SWITCHING WAVEFORMS



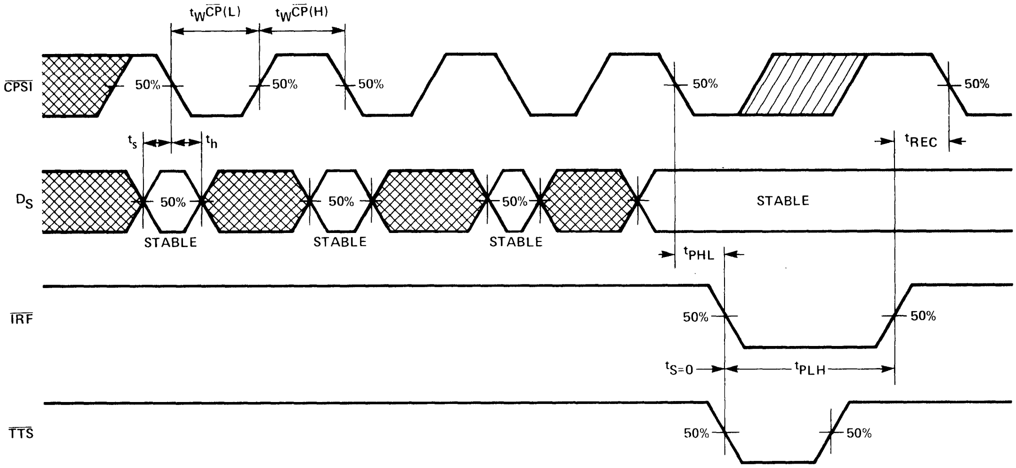
OUTPUT ENABLE TIME
(t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME
(t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

SWITCHING WAVEFORMS (Cont'd)

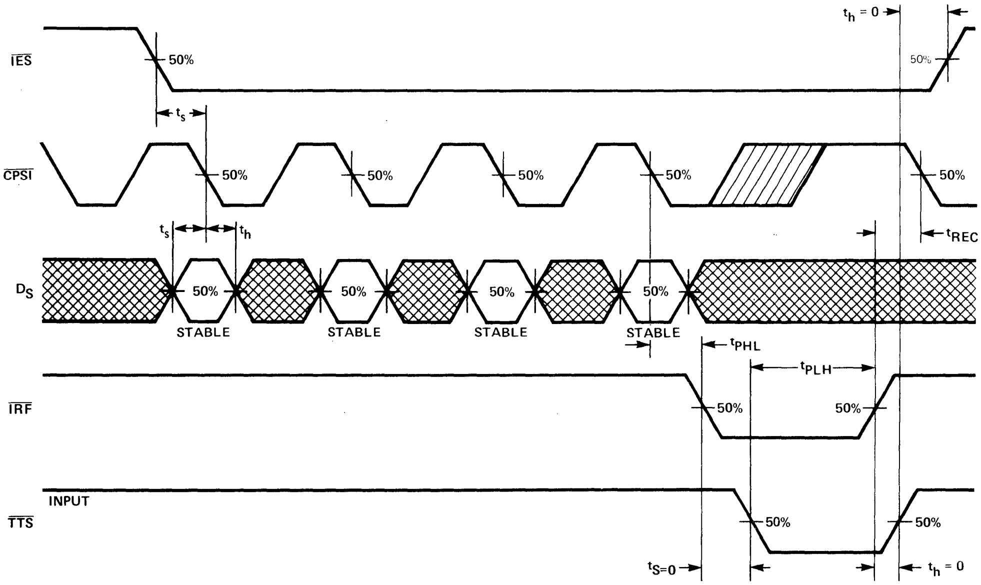
SERIAL INPUT UNEXPANDED OR MASTER OPERATION



MINIMUM $\overline{CPSI}$ PULSE WIDTH, PROPAGATION DELAY, $\overline{CPSI}$ TO $\overline{IRF}$ AND $\overline{TTS}$ TO $\overline{IRF}$, RECOVERY TIME, $\overline{IRF}$ TO $\overline{CPSI}$, AND SET-UP AND HOLD TIMES, D_S TO $\overline{CPSI}$, AND $\overline{TTS}$ TO $\overline{IRF}$.

CONDITIONS: STACK NOT FULL, $\overline{IES}$, = PL = LOW

SERIAL INPUT EXPANDED SLAVE OPERATION



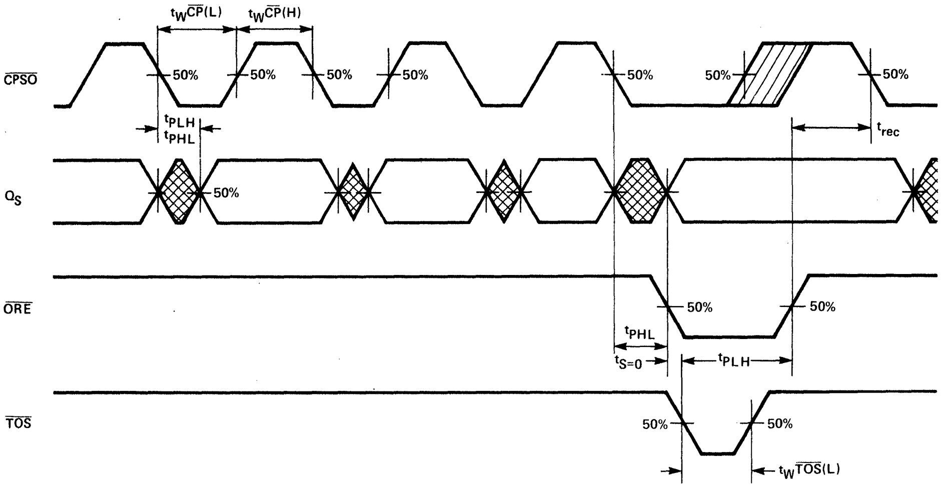
PROPAGATION DELAY, $\overline{CPSI}$ TO $\overline{IRF}$ AND $\overline{TTS}$ TO $\overline{IRF}$, RECOVERY TIME, $\overline{IRF}$ TO $\overline{CPSI}$ AND SET-UP AND HOLD TIMES, $\overline{IES}$ TO $\overline{CPSI}$, D_S TO $\overline{CPSI}$ AND $\overline{TTS}$ TO $\overline{IRF}$.

CONDITIONS: STACK NOT FULL $\overline{IES}$ = HIGH
WHEN INITIALIZED, PL = LOW

NOTE:
Set-up and hold times are shown as positive values but may be specified as negative values.

SWITCHING WAVEFORMS (Cont'd)

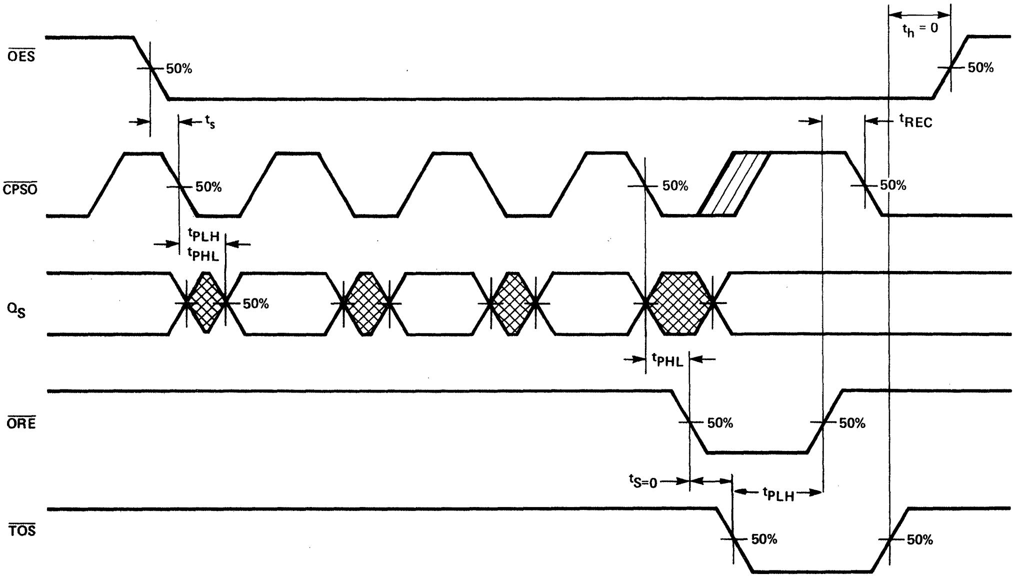
SERIAL OUTPUT, UNEXPANDED OR MASTER OPERATION



$\overline{\mathrm{ORE}}$ RECOVERY TIME, PROPAGATION DELAY $\overline{\mathrm{CPSO}}$ TO QS, $\overline{\mathrm{CPSO}}$ TO $\overline{\mathrm{ORE}}$, $\overline{\mathrm{TOS}}$ TO $\overline{\mathrm{ORE}}$, MINIMUM $\overline{\mathrm{CPSO}}$ PULSE WIDTH, MINIMUM $\overline{\mathrm{TOS}}$ PULSE WIDTH AND SET-UP TIME $\overline{\mathrm{ORE}}$ TO $\overline{\mathrm{TOS}}$.

CONDITIONS: DATA IN STACK, TOP = HIGH, $\overline{\mathrm{IES}}$ = LOW
WHEN INITIALIZED, $\overline{\mathrm{OES}}$ = LOW

SERIAL OUTPUT, SLAVE OPERATION



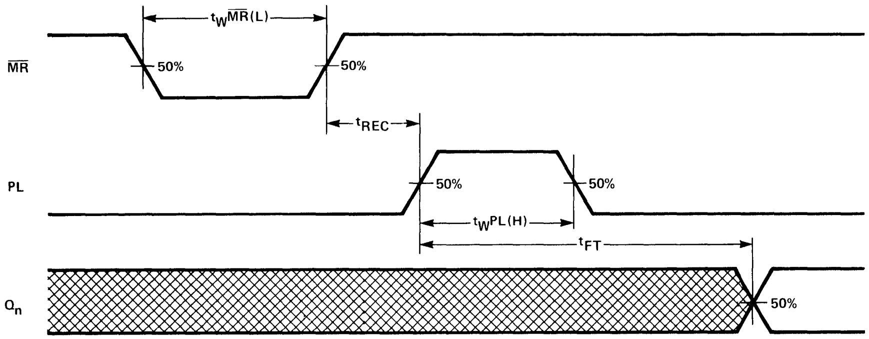
$\overline{\mathrm{ORE}}$ RECOVERY TIME, PROPAGATION DELAY $\overline{\mathrm{CPSO}}$ TO Q_S, $\overline{\mathrm{CPSO}}$ TO $\overline{\mathrm{ORE}}$, $\overline{\mathrm{TOS}}$ TO $\overline{\mathrm{ORE}}$, AND SET-UP AND HOLD TIMES, $\overline{\mathrm{OES}}$ TO $\overline{\mathrm{CPSO}}$, $\overline{\mathrm{ORE}}$ TO $\overline{\mathrm{TOS}}$, $\overline{\mathrm{TOS}}$ TO $\overline{\mathrm{OES}}$

CONDITIONS: DATA IN STACK, TOP = HIGH, $\overline{\mathrm{IES}}$ = HIGH
WHEN INITIALIZED

NOTE:
Set-up (t_s) and hold times (t_h) are shown as positive values but may be specified as negative values.

SWITCHING WAVEFORMS (Cont'd)

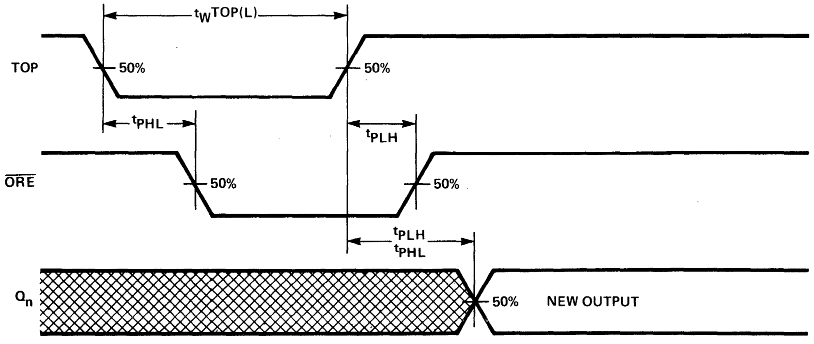
FALL THROUGH TIME



MINIMUM $\overline{MR}$ AND PL PULSE WIDTHS, RECOVERY TIME FOR $\overline{MR}$ AND FALL THROUGH TIME

CONDITIONS: $\overline{TTS}$ CONNECTED TO $\overline{IRF}$, $\overline{TOS}$ CONNECTED TO $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ = LOW. TOP = HIGH

PARALLEL OUTPUT, FOUR BIT WORD OR MASTER IN PARALLEL EXPANSION

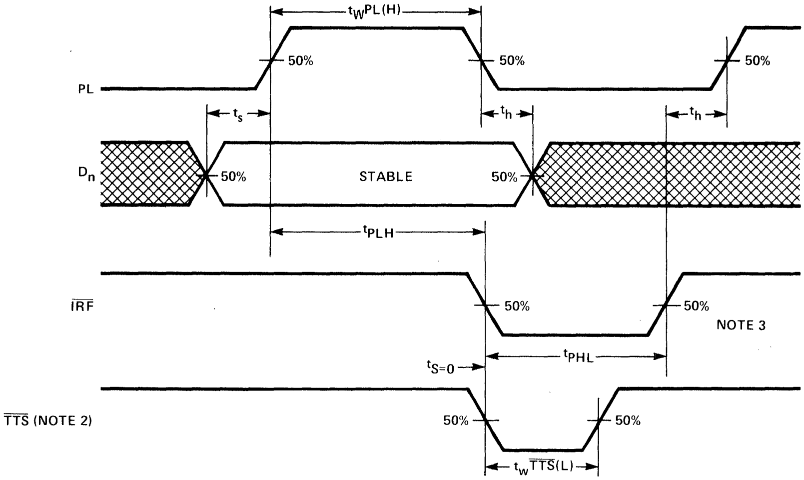


PROPAGATION DELAY, TOP TO $\overline{ORE}$, TOP TO Q_n, AND MINIMUM TOP PULSE WIDTH

CONDITIONS: $\overline{IES}$ = LOW WHEN INITIALIZED, $\overline{EO}$ = $\overline{CPSO}$ = LOW. DATA AVAILABLE IN STACK

SWITCHING WAVEFORMS (Cont'd)

PARALLEL LOAD MODE, FOUR BIT WORD (UNEXPANDED) OR MASTER IN PARALLEL EXPANSION



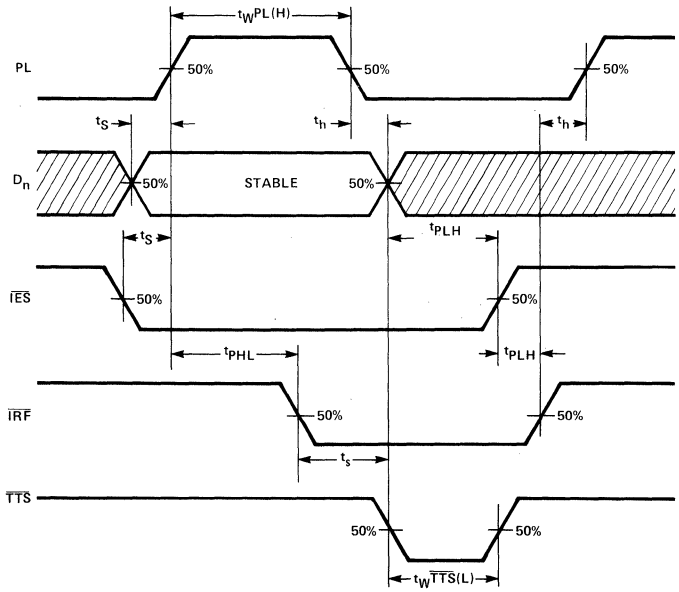
PROPAGATION DELAY PL TO $\overline{IRF}$, $\overline{TTS}$ TO $\overline{IRF}$, MINIMUM PL AND $\overline{TTS}$ PULSE WIDTHS, AND SET-UP AND HOLD TIMES D_n TO PL, $\overline{IRF}$ TO PL, $\overline{TTS}$ TO $\overline{IRF}$.

CONDITIONS: STACK NOT FULL, $\overline{IES}$ = LOW WHEN INITIALIZED

NOTES:

1. Initialization requires a master reset to occur after power has been applied.
2. $\overline{TTS}$ normally connected to $\overline{IRF}$.
3. If stack is full, $\overline{IRF}$ will stay LOW.

PARALLEL LOAD, SLAVE MODE



PROPAGATION DELAY, $\overline{TTS}$ TO $\overline{IES}$, $\overline{IES}$ TO $\overline{IRF}$, PL TO $\overline{IRF}$, MINIMUM PL AND $\overline{TTS}$ PULSE WIDTHS, AND SET-UP AND HOLD TIMES, D_n TO PL, $\overline{IRF}$ TO $\overline{TTS}$, $\overline{IRF}$ TO PL

CONDITIONS: STACK NOT FULL, DEVICE INITIALIZED WITH $\overline{IES}$ HIGH

NOTE:

Set-up (t_s) and hold times (t_h) are shown as positive values but may be specified as negative values.

4710B/4710BX

REGISTER STACK • 16×4 RAM WITH 3-STATE OUTPUT REGISTER

FAIRCHILD CMOS MACROLOGIC™

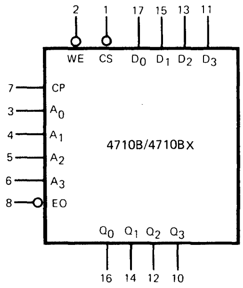
DESCRIPTION – The 4710B/4710BX is a register oriented high speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge triggered 4-bit output register allows new input data to be written while previous data is held. 3-state outputs are provided for maximum versatility. The 4710B/4710BX is fully compatible with all CMOS families. The 4710B is specified to operate over a power supply voltage range of 4.5 V to 12.5 V. The 4710BX is specified to operate over a power supply voltage range of 3 V to 15 V.

- **EDGE-TRIGGERED OUTPUT REGISTER**
- **3-STATE OUTPUTS**
- **OPTIMIZED FOR REGISTER STACK OPERATION**
- **18-PIN PACKAGE**

PIN NAMES

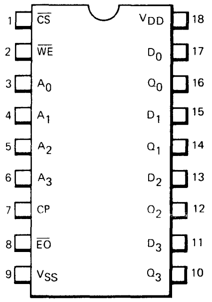
A_0-A_3	Address Inputs
D_0-D_3	Data Inputs
$\overline{CS}$	Chip Select Input (Active LOW)
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
CP	Clock Input (Outputs Change on LOW to HIGH Transition)
Q_0-Q_3	Outputs

LOGIC SYMBOL



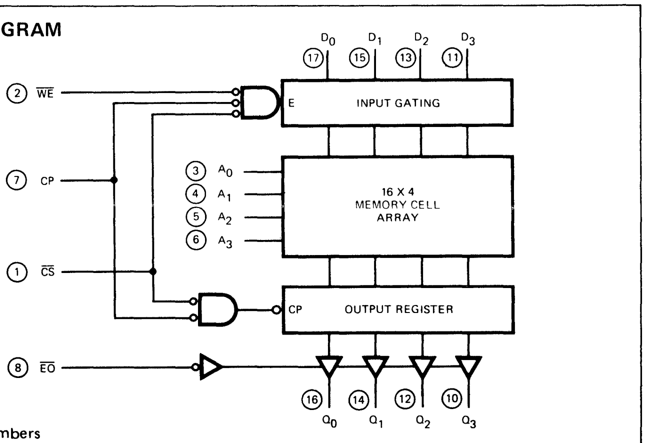
V_{DD} = Pin 18
V_{SS} = Pin 9

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



V_{DD} = Pin 18
V_{SS} = Pin 9
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 4710B/4710BX consists of a 16 X 4-bit RAM selected by four address inputs (A_0 – A_3) and an edge-triggered 4-bit Output Register with 3-state Output Buffers.

Write Operation - When the three control inputs: Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are LOW the information on the data inputs (D_0 - D_3) is written into the memory location selected by the address inputs (A_0 - A_3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are LOW, the contents of the selected memory location follows these changes provided set-up time criteria are met.

Read Operation - Whenever $\overline{CS}$ is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the address inputs (A_0 - A_3) is edge triggered into the Output Register.

A 3-State Output Enable ($\overline{EO}$) controls the output buffers. When $\overline{EO}$ is HIGH the four outputs (Q_0 - Q_3) are in a high impedance or OFF state; when $\overline{EO}$ is LOW, the outputs are determined by the state of the Output Register.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	μA	MIN, 25°C	Output Returned to V_{SS} $\overline{EO}$ = V_{DD}
											- 12		MAX	
		XM									-0.4		MIN, 25°C	
											- 12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20		MIN, 25°C	
					150			300			600		MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

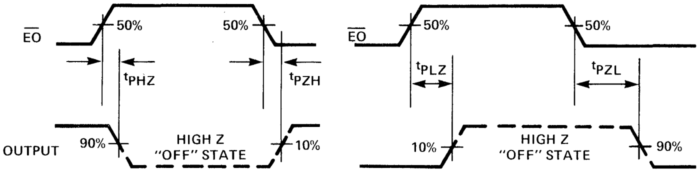
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
	READ MODE											
t_{PLH}	Propagation Delay, CP to Output		146	292		56	112		40	80	ns	
t_{PHL}			125	250		49	98		34	68		
t_{PZH}	Enable Time, $\overline{EO}$ to Output		57	114		20	40		16	32	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			81	162		31	62		23	46		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Disable Time, $\overline{EO}$ to Output		57	114		29	58		23	46	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			72	144		31	62		25	50		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		75	150		45	90		35	70	ns	
t_{THL}			80	160		45	90		35	70		
	WRITE MODE											
$t_w\overline{WE}$	Minimum $\overline{WE}$ Pulse Width (Note 3)	218	109		104	52		62	31		ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
$t_w\overline{CS}$	Minimum $\overline{CS}$ Pulse Width (Note 3)	226	113		124	62		74	37		ns	
t_wCP	Minimum CP Pulse Width (Note 3)	240	120		124	62		74	37		ns	
t_s	Set-Up Time $\overline{CS}$ to $\overline{WE}$ (Note 4)	326	163		198	99		134	67		ns	
t_h	Hold Time, $\overline{CS}$ to $\overline{WE}$ (Note 4)	0	-15		0	-10		0	-5		ns	
t_s	Set-Up Time, $\overline{CS}$ to CP	186	93		104	52		68	34		ns	
t_h	Hold Time, $\overline{CS}$ to CP	0	-15		0	-10		0	-5		ns	
t_s	Set-Up Time, $\overline{D}_n$ to $\overline{WE}$ (Note 4)	176	68		70	35		48	24		ns	
t_h	Hold Time, $\overline{D}_n$ to $\overline{WE}$ (Note 4)	0	-15		0	-10		0	-5		ns	
t_s	Set-Up Time, Address to $\overline{WE}$ (Note 4)	206	103		100	50		58	29		ns	
t_h	Hold Time, Address to $\overline{WE}$ (Note 4)	0	-15		0	-10		0	-5		ns	
	READ MODE											
t_s	Set-Up Time Address to CP	706	353		372	186		208	104		ns	
t_h	Hold Time Address to CP	0	-15		0	-10		0	-5		ns	

NOTES:

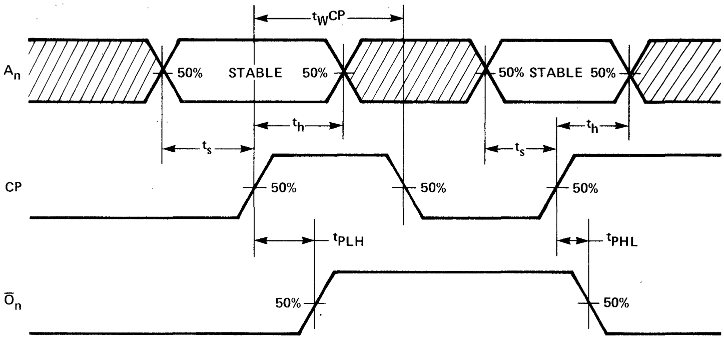
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. Writing occurs when $\overline{WE}$; $\overline{CE}$, and CP are LOW.
4. Assuming $\overline{WE}$ is utilized as a Writing STROBE.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS

READ MODE



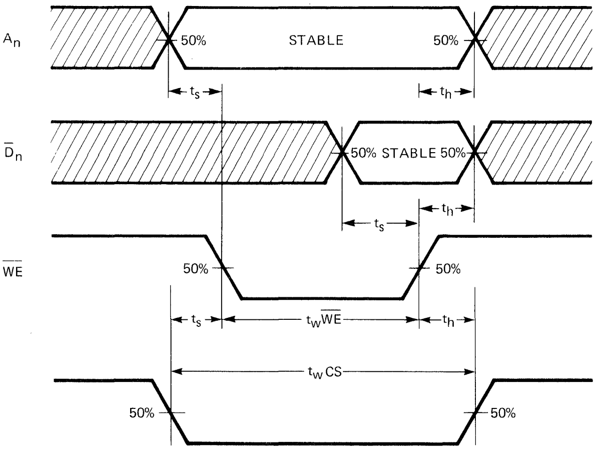
$\overline{EO}$ TO OUTPUT ENABLE AND DISABLE TIMES



MINIMUM CP PULSE WIDTH, PROPAGATION DELAY CLOCK TO OUTPUT, AND SET-UP AND HOLD TIMES ADDRESS TO CLOCK

CONDITIONS: $\overline{CS}$ = $\overline{EO}$ = LOW, $\overline{WE}$ = HIGH

WRITE MODE



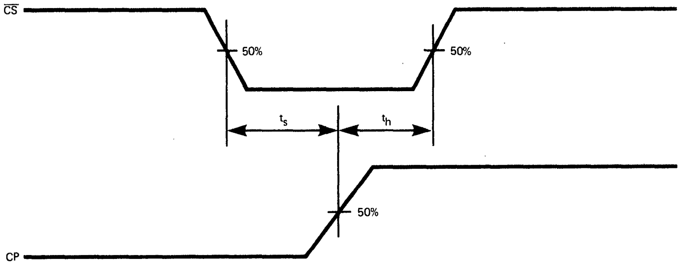
MINIMUM $\overline{CS}$ PULSE WIDTH, MINIMUM WRITE ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES ADDRESS TO $\overline{WE}$, DATA TO $\overline{WE}$, AND $\overline{CS}$ to $\overline{WE}$

CONDITIONS: CP = LOW

NOTE: Set-Up (t_s) and Hold Times (t_h) are shown as positive values but may be specified as negative values.

SWITCHING WAVEFORMS (CONT'D)

WRITE MODE



SET-UP AND HOLD TIMES, $\overline{CS}$ TO CP

NOTE: Set-up Times (t_s) and Hold Times (t_h) are shown as positive values, but may be specified as negative values.

4720B/4720BX

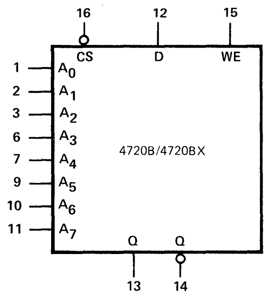
256-BIT RANDOM ACCESS MEMORY WITH 3-STATE OUTPUT

DESCRIPTION – The 4720B/4720BX is a 256-Bit Random Access Memory with 3-State Outputs. It has a Data Input (D), eight Address inputs (A_0-A_7), an active HIGH Write Enable Input (WE), an active LOW Chip Select Input ($\overline{CS}$), an active HIGH 3-State Output (Q) and an active LOW 3-State Output ($\overline{Q}$). Information on the Data Input (D) is written into the memory location selected by the Address Inputs (A_0-A_7) when the Chip Select Input ($\overline{CS}$) is LOW and the Write Enable Input (WE) is HIGH. Under these conditions, the device is transparent, i.e., the data input is reflected at the True and Complementary Outputs (Q, $\overline{Q}$). Information is read from the memory location selected by the Address Inputs (A_0-A_7) while the Chip Select ($\overline{CS}$) and the Write Enable (WE) Inputs are LOW. The Q Output is the information written into the memory, $\overline{Q}$ is its complement. When the Chip Select Input ($\overline{CS}$) is HIGH, both outputs (Q, $\overline{Q}$) are held in the high impedance OFF state. This allows other 3-State outputs to be wired together in a bus arrangement. The 4720B/4720BX offers fully static operation.

The 4720B is specified to operate over a power supply voltage range of 4.5 to 12.5 V. The 4720BX is specified to operate over a power supply voltage range of 3 to 15 V.

- **3-STATE OUTPUTS**
- **ORGANIZATION – 256 WORDS X 1-BIT**
- **ON-CHIP DECODING**
- **TRUE AND COMPLEMENT OUTPUTS AVAILABLE**
- **FULLY STATIC**
- **LOW POWER DISSIPATION**
- **HIGH SPEED**
- **TYPICAL HOLDING VOLTAGE OF 1.5 V**

LOGIC SYMBOL

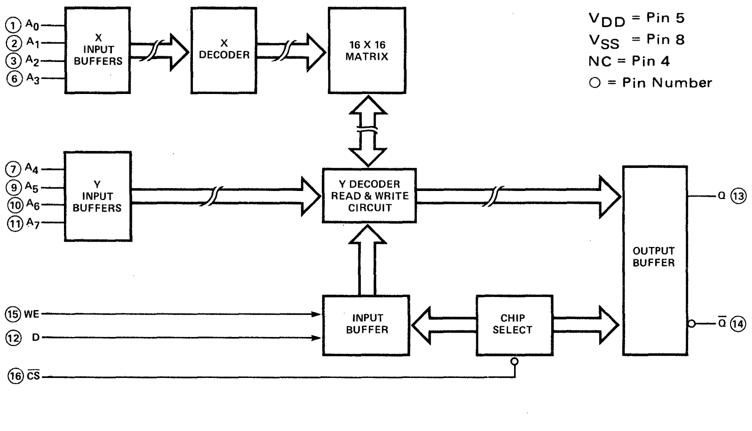


V_{DD} = Pin 5
V_{SS} = Pin 8
NC = Pin 4

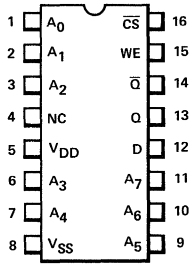
MODE SELECTION

$\overline{CS}$	WE	Q	$\overline{Q}$	MODE
L	H	Data Written Into Memory	Complement of Data Written Into Memory	Write
L	L	Data Written Into Memory	Complement of Data Written Into Memory	Read
H	X	High Impedance	High Impedance	Inhibit

BLOCK DIAGRAM



CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

$\overline{CS}$	Chip Select Input (Active LOW)
WE	Write Enable Input
D	Data Input
A_0-A_7	Address Inputs
Q	3-State Output (Active HIGH)
$\overline{Q}$	3-State Output (Active LOW)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current, HIGH	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{CS} = V_{DD}$
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current, LOW	XC									-1.6	μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{CS} = V_{DD}$
											-12		MAX	
		XM									-0.4		MIN, 25°C	
											-12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

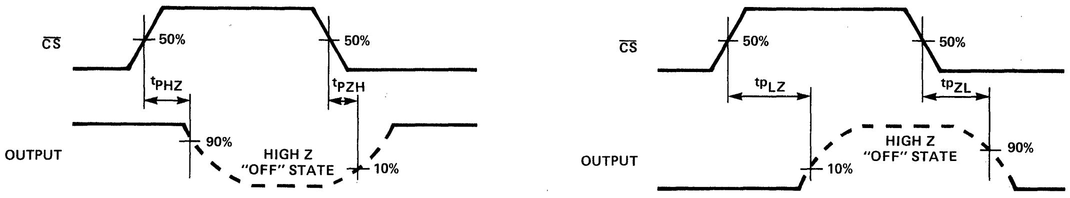
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25°C$ (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
	READ MODE											
t_{PLH}	Propagation Delay,		250	500		95	190		68	136	ns	
t_{PHL}	Address to Output		250	500		95	190		68	136		
t_{PZH}	Enable Time, $\overline{CS}$ to Output		30	60		15	30		11	22	ns	($R_L = 1$ kΩ to V_{SS})
t_{PZL}			35	70		17	34		12	24		($R_L = 1$ kΩ to V_{DD})
t_{PHZ}	Disable Time, $\overline{CS}$ to Output		25	50		15	30		11	22	ns	($R_L = 1$ kΩ to V_{SS})
t_{PLZ}			27	54		16	32		12	24		($R_L = 1$ kΩ to V_{DD})
t_{TLH}	Output Transition Time		75	150		35	70		25	50	ns	
t_{THL}			75	150		35	70		25	50		
	WRITE MODE											
t_{PLH}	Propagation Delay,		250	500		100	200		65	130	ns	
t_{PHL}	WE to Output		250	500		100	200		65	130		$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ≤ 20 ns
	WRITE MODE											
t_wWE	Minimum WE Pulse Width	240	120		110	55		80	40		ns	
t_s	Set-Up Time, D to WE	80	40		38	19		28	14		ns	
t_h	Hold Time, D to WE	40	20		22	11		18	9			
t_s	Set-Up Time, Address to WE	260	130		130	65		90	45		ns	
t_h	Hold Time, Address to WE	160	80		80	40		40	20			
t_s	Set-Up Time, $\overline{CS}$ to WE	60	30		30	15		20	10		ns	
t_h	Hold Time, $\overline{CS}$ to WE	60	30		30	15		20	10			

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. All set-up (t_s) and hold (t_h) times are measured with minimum write enable pulse width (t_wWE).

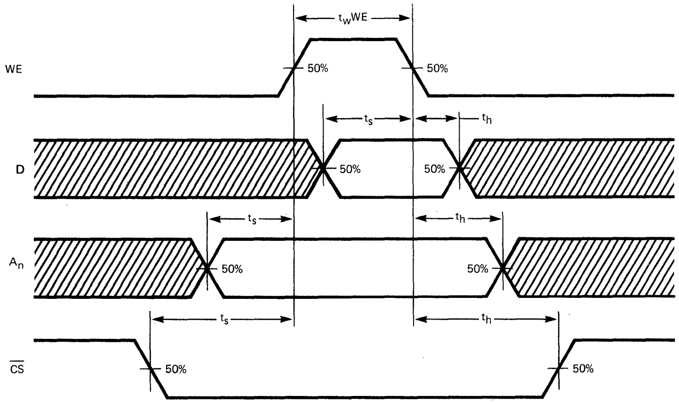
SWITCHING WAVEFORMS

READ MODE



$\overline{\text{CS}}$ TO OUTPUT ENABLE AND DISABLE TIMES

WRITE MODE



MINIMUM PULSE WIDTH FOR WE AND SET-UP AND HOLD TIMES,
D TO WE, A_n TO WE, AND $\overline{\text{CS}}$ TO WE

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

4722B

PROGRAMMABLE TIMER/COUNTER

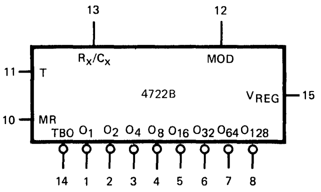
GENERAL DESCRIPTION —The 4722B Programmable Timer/Counter is a monolithic controller capable of producing accurate microsecond to five day time delays. Long delays, up to three years, can easily be generated by cascading two timers. The timer consists of a time base oscillator programmable 8-bit counter and control flip-flop. An external resistor capacitor (R_xC_x) network sets the oscillator frequency and allows delay times from 1 R_xC_x to 255 R_xC_x to be selected. In the astable mode of operation, 255 frequencies or pulse patterns can be generated from a single R_xC_x network. These frequencies or pulse patterns can also easily be synchronized to an external signal. The Trigger Input (T), Master Reset Input (MR) and Data Outputs ($\overline{O}_0$, $\overline{O}_2$, $\overline{O}_4$, $\overline{O}_8$, $\overline{O}_{16}$, $\overline{O}_{32}$, $\overline{O}_{64}$, $\overline{O}_{128}$) are all TTL and DTL compatible for easy interface with digital system. The timer's high accuracy and versatility in producing a wide range of time delays makes it ideal as a direct replacement for mechanical or electromechanical devices.

- **ACCURATE TIMING FROM MICROSECONDS TO DAYS**
- **PROGRAMMABLE DELAYS FROM 1 R_xC_x TO 255 R_xC_x**
- **TTL, DTL AND CMOS COMPATIBLE OUTPUTS**
- **TIMING DIRECTLY PROPORTIONAL TO R_xC_x TIME CONSTANT**
- **HIGH ACCURACY**
- **EXTERNAL SYNC AND MODULATION CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE**
- **EXCELLENT SUPPLY VOLTAGE REJECTION**
- **LOW POWER DISSIPATION**

PIN NAMES

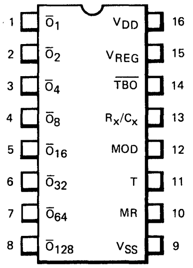
R_x/C_x	External Resistor/Capacitor Connection
T	Trigger Input
MOD	Modulation Input
MR	Master Reset Input
V_{REG}	Regulator Output
$\overline{TBO}$	Time Base Output (Open Drain)
$\overline{O}_1, \overline{O}_2, \overline{O}_4, \overline{O}_8, \overline{O}_{16}, \overline{O}_{32}, \overline{O}_{64}, \overline{O}_{128}$	Data Outputs (Active Low-Open Drain)

LOGIC SYMBOL



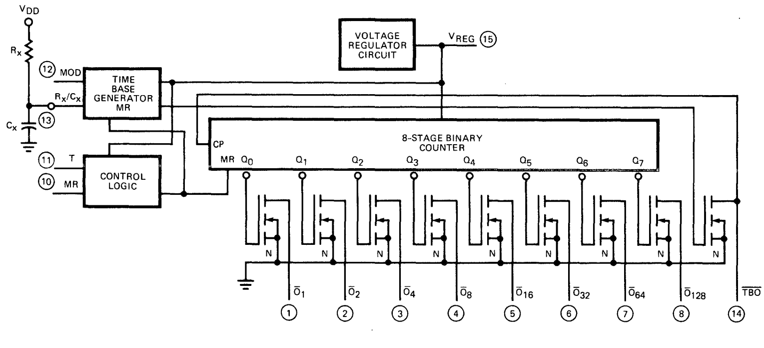
V_{DD} = Pin 16
V_{SS} = Pin 9

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

When power is applied to the 4722B with no Trigger (T) or Master Reset (MR) Inputs, the circuit starts with all outputs in a high impedance OFF state. Application of a positive-going trigger pulse to T initiates the timing cycle. The Trigger Input (T) activates the Time-Base Generator, enables the counter and sets the counter outputs LOW. The time-base generator generates timing pulses with a period $T = 1\ R_xC_x$. These clock pulses are counted by the 8-stage Binary Counter. The timing sequence is completed when a positive-going pulse is applied to MR.

Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a Master Reset is applied. If both the Master Reset and Trigger Inputs are activated simultaneously, the Trigger Input takes precedence.

Figure 1 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a Trigger Input. When the circuit is in a Master Reset state, both the time-base and the counter sections are disabled and all the counter outputs are in a high impedance OFF state.

In most timing applications, one or more of the counter outputs are connected to the Master Reset terminal with S1 closed *(Figure 2)*. The circuit starts timing when a Trigger Input is applied and automatically resets itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the Master Reset terminal (switch S1 open), the circuit operates in an astable or free-running mode, following a Trigger Input.

Important Operating Information

- Ground connection is pin 9.
- Master Reset sets all outputs to a high impedance OFF state.
- Trigger sets all outputs LOW.
- Time-base $\overline{\text{TBO}}$ can be disabled by bringing the R_x/C_x Input LOW via a pull-down resistor.
- Normal Time-base Output ($\overline{\text{TBO}}$) is a negative-going pulse greater than 500 ns.
- Master Reset stops the time-base generator.
- Data outputs $\overline{O}_1 \ldots . \overline{O}_{128}$ sink 1.6 mA current with $V_{OL} \leqslant 0.4$ V;
- For use with external clock, minimum clock pulse amplitude should be 0.7 V_{DD}, with greater than 1 µs pulse duration.

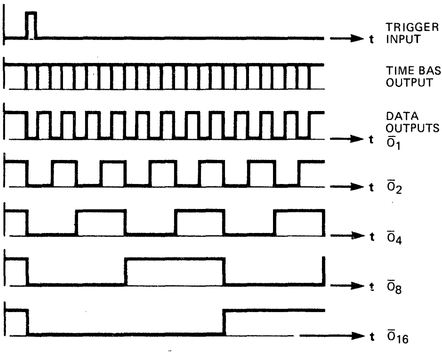


Fig. 1 Timing Diagram of Output Waveforms

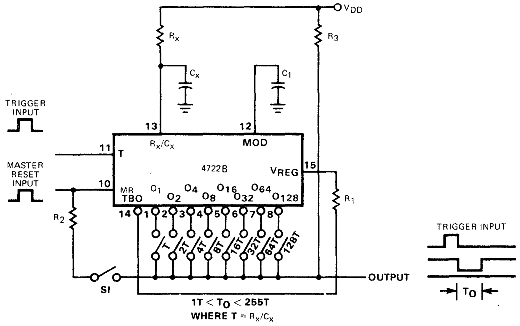


Fig. 2 Basic Circuit Connection for Timing Applications
Monostable: S1 Closed
Astable: S1 Open

CIRCUIT CONTROLS

Data Outputs ($\overline{O}_1 \ldots \overline{O}_{128}$)
The Data Outputs are buffered open-drain type stages, as shown in the block diagram. Each output is capable of sinking 1.6 mA at 0.4 V V_{OL}. In the Master Reset condition, all the Data Outputs are in a high impedance OFF state. Following a Trigger Input, the Outputs change state in accordance with the timing diagram of ***Figure 1.*** The Data Outputs can be used individually, or can be connected together in a wired-OR configuration, as described in the Programming section.

Master Reset and Trigger Inputs (MR and T)
The circuit is reset or triggered with positive-going control pulses applied to MR and T, respectively. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Modulation Input (MOD)
The oscillator time-base period T can be modulated by applying a dc voltage to MOD. The time-base generator can be synchronized to an external clock by applying a sync pulse to MOD, as shown in ***Figure 3.***

The time base can be synchronized by setting the time-base period T to be an integer multiple of the sync pulse period, T_s. This can be done by choosing the timing components R_x and C_x such that:

$$T = R_xC_x = (T_s/m)$$

where

$$m \text{ is an integer, } 1 \leqslant m \leqslant 10$$

Figure 4 gives the typical pull-in range for harmonic synchronization for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.

R_x/C_x Connection
The time-base period T is determined by the external R_xC_x network connected to R_x/C_x. When the time base is triggered, the waveform at R_x/C_x is an exponential ramp with a period $T = 1.0\ R_xC_x$.

Time-Base Output ($\overline{\text{TBO}}$)
The Time-Base Output is an open-drain type stage as shown in the block diagram and requires a pull-up resistor to V_{REG} for proper circuit operation. In the Master Reset state, the time-base output is in a high impedance OFF state. After triggering, it produces a negative-going pulse train with a period $T = R_xC_x$ as shown in the diagram of ***Figure 1.*** The Time-Base Output is internally connected to the binary-counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative-going edge of the timing or clock pulses generated at $\overline{\text{TBO}}$. The counter section can be disabled by clamping the voltage level at $\overline{\text{TBO}}$ to ground.

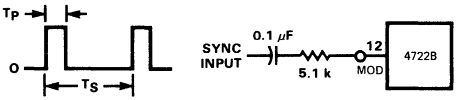


Fig. 3 Operation with External Sync. Signal

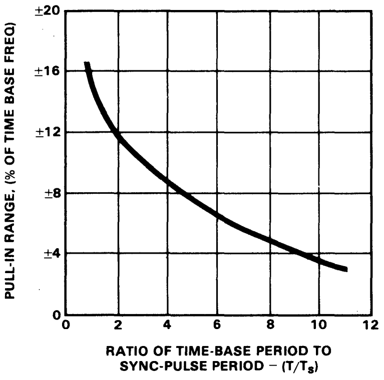


Fig. 4 Typical Pull-in Range for Harmonic Synchronization

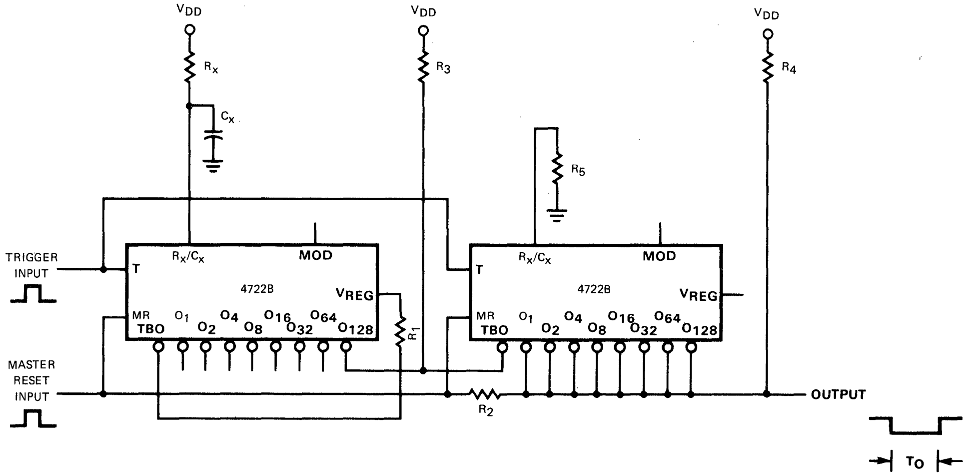


Fig. 5 Cascaded Operation for Long Delays

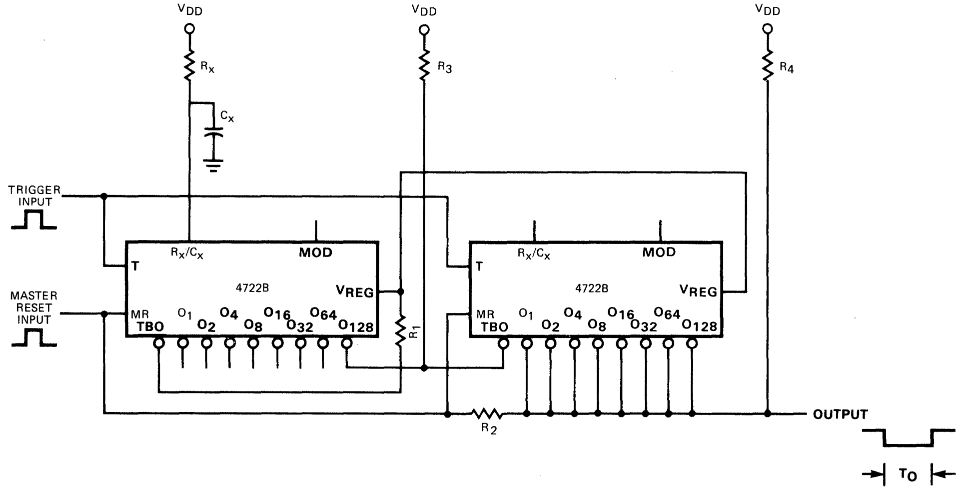


Fig. 6 Low Power Operation of Cascaded Timers

Regulator Output (V_{REG})

The Regulator Output (V_{REG} is used internally to drive the counter and the control logic. This terminal can also be used as a supply to additional 4722B circuits when several timer circuits are cascaded (see *Figure 6*) to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{DD} input terminal to power down the internal time base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time-base, V_{REG} should be shorted to V_{DD}.

MONOSTABLE OPERATION

Precision Timing

In precision timing applications, the 4722B is used in its monostable or self-resetting mode. The generalized circuit connection for this application is shown in *Figure 2.* The output is normally OFF and goes LOW following a Trigger Input. It remains LOW for the time duration, T_O, and then returns to the OFF state. The duration of the timing cycle T_O is given as:

$$T_O = NT = NR_xC_x$$

where $T = R_xC_x$ is the time-base period as set by the choice of timing components at R_x/C_x and N is an integer in the range of $1 \leqslant N \leqslant 255$ as determined by the combination of counter outputs $\overline{O}_1 \ldots \overline{O}_{128}$, connected to the output bus.

Counter-Output Programming

The Data Outputs, $\overline{O}_1 \ldots \overline{O}_{128}$, are open-drain type stages and can be shorted together to a common pull-up resistor to form a wired-OR connection; the combined output will be LOW as long as any one of the outputs is LOW. The time delays associated with each Data Output can be added together. This is done by simply shorting the outputs together to form a common output bus as shown in *Figure 2.* For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, is 32 T. Similarly, if pins 1, 5, and 6 are shorted to the output bus, the total time delay is $T_O = (1 + 16 + 32)\ T = 49\ T$. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1\ T \leqslant T_O \leqslant 255\ T$.

Ultra-Long Time-Delay Application

Two 4722Bs can be cascaded as shown in *Figure 5* to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_O = 256\ R_xC_x$ to $T_O = 65.536\ R_xC_x$ in 256 discrete steps by selectively shorting one or more of the Data Outputs from Unit 2 to the output bus. In this application, the Master Reset and the Trigger Inputs of both units are tied together and the Unit 2 time base generator is disabled. Normally, the output is OFF when the system is reset. On triggering, the output goes LOW where it remains for a total of $(256)^2$ or 65.536 cycles of the time-base oscillator.

In cascaded operation, the time-base generator of Unit 2 can be powered down to reduce power consumption by using the circuit connection of *Figure 6*. In this case, the V_{DD} terminal of Unit 2 is left open, and the second unit is powered from the V_{REG} Output of Unit 1 by connecting the V_{REG} (pins 15) of both units together.

ASTABLE OPERATION

The 4722B can be operated in its astable or free-running mode by disonnecting the Master Reset Input from the Data Outputs. Two typical circuits are shown in *Figure 7* and *8*. The circuit in *Figure 7* operates in its free-running mode with external trigger and reset signals. It starts counting and timing following a Trigger Input until an external Master Reset pulse is applied. Upon application of a positive-going reset signal to MR, the circuit reverts back to its Master Reset state. This circuit is essentially the same as that of *Figure 2* with the feedback switch S1 open.

The circuit of *Figure 8* is designed for continuous operation. It self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely, in astable or free-running operation; each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Binary Pattern Generation

In astable operation, as shown in *Figure 7*, the output of the 4722B appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of *Figure 1*, which shows the phase relations between the counter outputs. *Figures 9* and *10* show some of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.

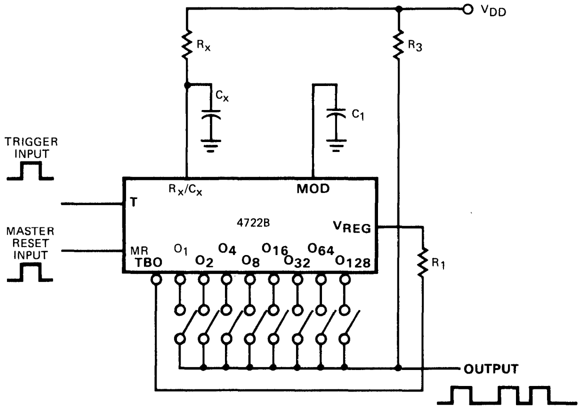


Fig. 7 Operation with External Trigger and Master Reset Inputs

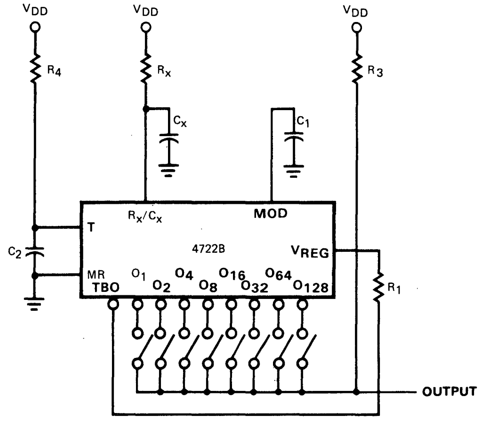


Fig. 8 Free-Running or Continuous Operation

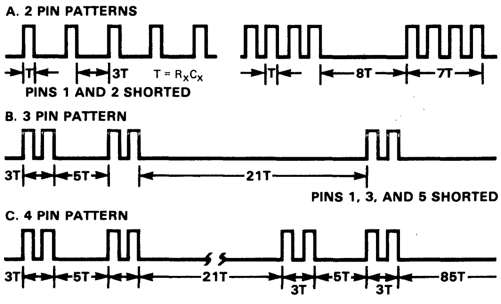


Fig. 9 Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

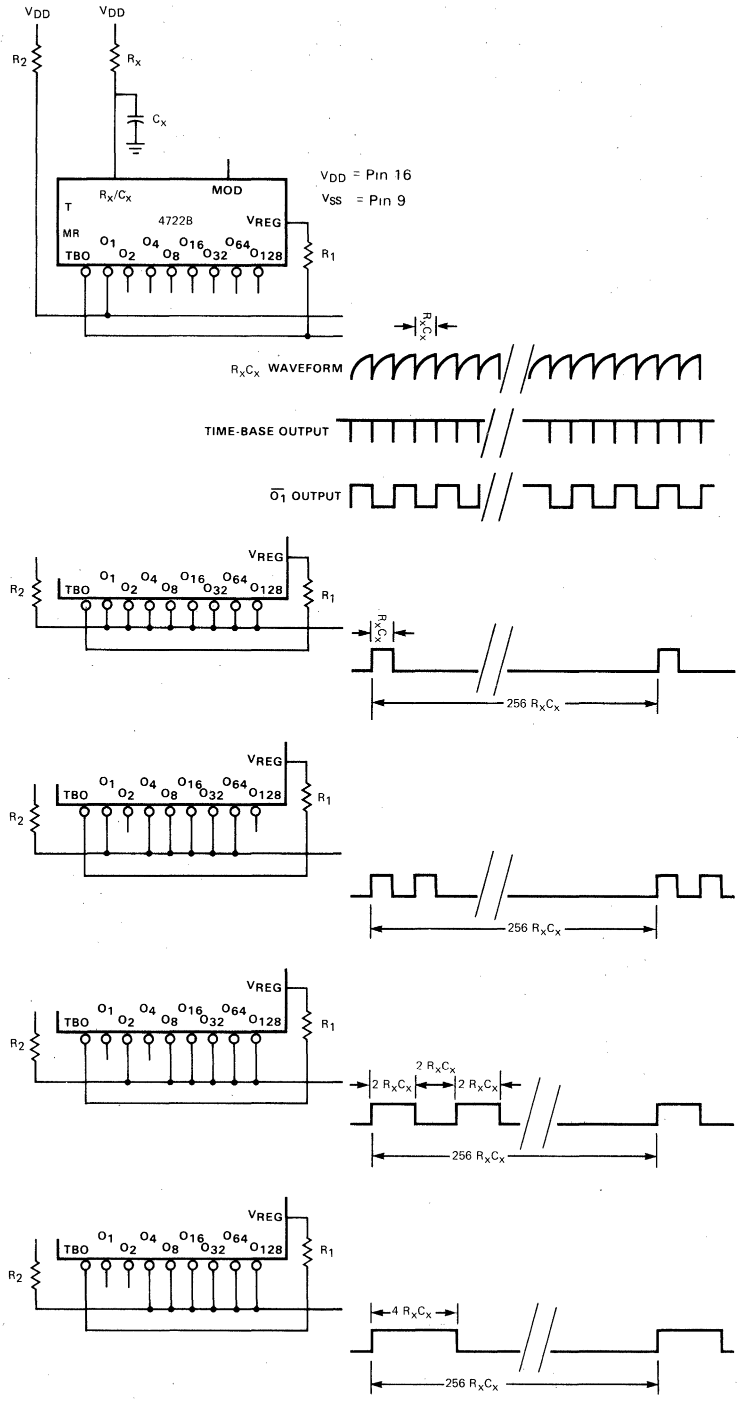


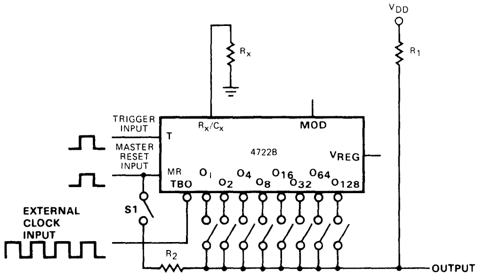
Fig. 10 Continuous Free-run Operation Examples of Output

OPERATION WITH EXTERNAL CLOCK

The 4722B can be operated with an external clock or time base by disabling the internal time-base generator and applying the external clock input to $\overline{\text{TBO}}$. The recommended circuit connection for this application is shown in *Figure 11.* The internal time base is de-activated by connecting a resistor from R_XC_X to ground. The counters are triggered on the negative-going edges of the external clock pulse.

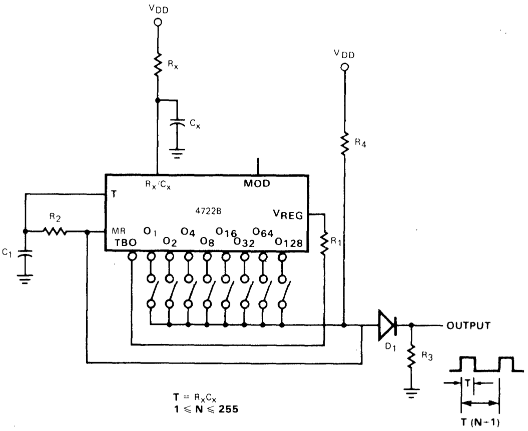
FREQUENCY SYNTHESIZER

The programmable counter section of the 4722B can be used to generate 255 discrete frequencies from a given Time-Base Output setting using the circuit connection of *Figure 12.* The circuit output is a positive pulse train with a pulse width equal to T, and a period equal to (N + 1) T where N is the programmed count in the counter. The modulus N is the total count corresponding to the Data Outputs connected to the output bus. For example, if pins 1, 3, and 4 are connected together to the output bus, the total count is N = 1 + 4 + 8 = 13, and the period of the output waveform is equal to (N + 1) T or 14 T. In this manner, 255 different frequencies can be synthesized from a given time-base setting.



S1 OPEN: ASTABLE OPERATION
S1 CLOSED: MONOSTABLE

Fig. 11 Operation with External Clock



T = RxCx
1 ≤ N ≤ 255

Fig. 12 Frequency Synthesis from Internal Time-Base

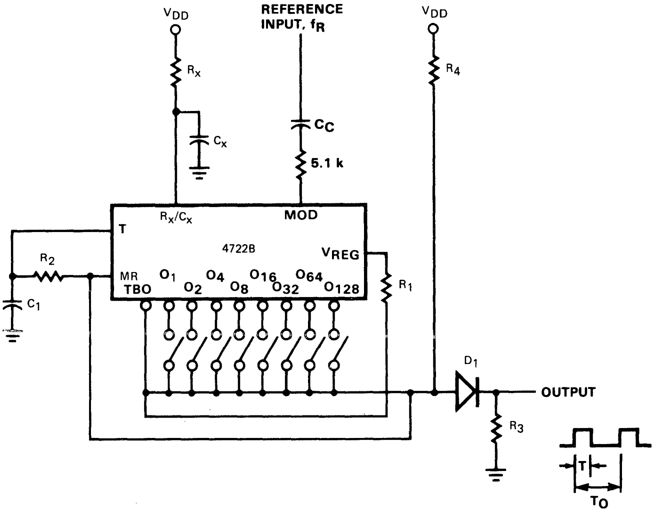


Fig. 13 Frequency Synthesis by Harmonic Locking to an External Reference

SYNTHESIS WITH HARMONIC LOCKING

The harmonic synchronizing feature of the time base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in ***Figure 13*** (see ***Figures 3*** and ***4*** for external sync waveform and harmonic capture range). If the time base is synchronized to (m)th harmonic of input frequency where $1 \leqslant m \leqslant 10$, the frequency f_O of the output waveform in ***Figure 13*** is related to the input reference frequency f_R as

$$f_O = f_R \frac{m}{(N+1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leqslant N \leqslant 255$, the circuit of ***Figure 13*** can produce 2550 different frequencies from a single fixed reference.

The circuit of ***Figure 13*** can be used to generate frequencies which are not harmonically related to a reference input. For example, by selecting the external R_XC_X to set m = 10 and setting N = 5, a 100 Hz output frequency synchronized to 60 Hz power line frequency can be obtained.

STAIRCASE GENERATOR

The 4722B Programmable Timer/Counter can be interconnected with an external operational amplifier and a precision resistor ladder to form a staircase generator as shown in ***Figure 14.*** Under Master Reset condition, the output is LOW. When a Trigger is applied, the op amp output goes HIGH and generates a negative-going staircase of 256 equal steps. The time duration of each step is equal to the time-base period T. The staircase can be stopped at any level by applying a disable signal to $\overline{\text{TBO}}$, through a steering diode, as shown in ***Figure 14.*** The count is stopped when $\overline{\text{TBO}}$ is clamped.

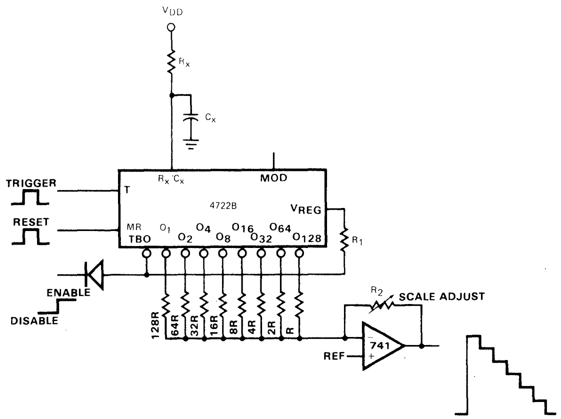


Fig. 14 Staircase Generator

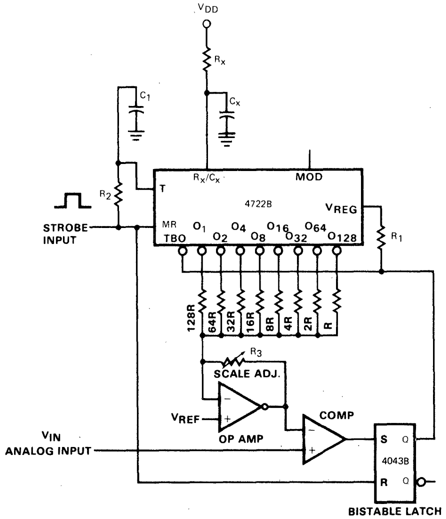


Fig. 15 Digital Sample and Hold Circuit

DIGITAL SAMPLE AND HOLD

Figure 15 shows a digital sample and hold circuit using the 4722B. Circuit operation is similar to the staircase generator described in the previous section. When a strobe input is applied, the R_xC_x low-pass network between the Master Reset and the Trigger Inputs resets the timer, then triggers it. This strobe input also sets the output of the bistable latch to a HIGH stage and activates the counter.

The circuit generates a staircase voltage at the op amp output. When the level of the staircase reaches that of the analog input to be sampled, the comparator changes state, activates the bistable latch and stops the count. At this point, the voltage level at the op amp output corresponds to the sampled analog input. Once the input is sampled, it is held until the next strobe signal.

ANALOG-TO-DIGITAL CONVERTER

Figure 16 shows a simple 8-bit A/D converter system using the 4722B. Circuit operation is very similar to that of the digital sample and hold system of *Figure 15*. In the case of A/D conversion, the digital output is obtained in parallel format from the binary-counter outputs with the output at pin 8 corresponding to the most significant bit (MSB).

DIGITAL TACHOMETER TIME BASE

A digital tachometer requires a time-base generator to supply two pulse outputs at specific intervals, *e.g.,* every second. The first pulse is a command (load) to transfer the accumulated counts in the counter section into latches (memory); the second resets the counter to zero. A simple adjustable time base, accurate to approximately ±0.5%, can be implemented using the circuit in *Figure 17.*

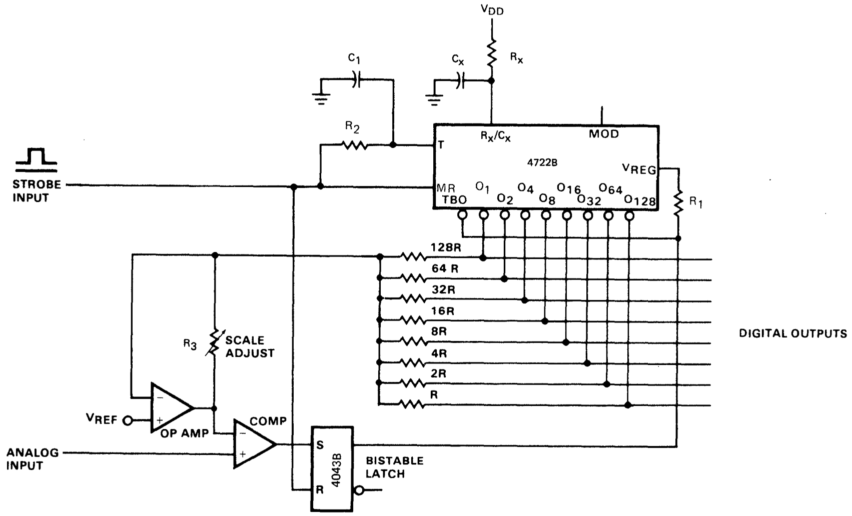


Fig. 16. **Analog-to-Digital Converter**

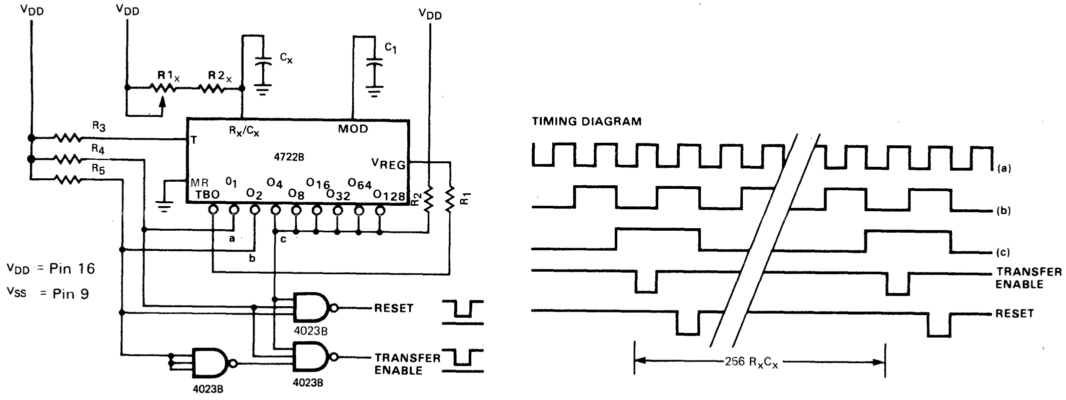


Fig. 17 **Simple Time Generator for a Digital Tachometer**

4723B

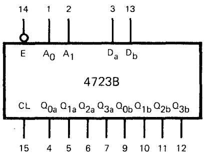
DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION – The 4723B is a Dual 4-Bit Addressable Latch with common control inputs; these include two Address Inputs (A_0, A_1), an active LOW Enable Input ($\overline{E}$) and an active HIGH Clear Input (CL). Each latch has a Data Input (D) and four Outputs (Q_0-Q_3).

When the Enable ($\overline{E}$) and Clear (CL) Inputs are HIGH, all Outputs (Q_0-Q_3) are LOW. Dual 4-channel demultiplexing occurs when the Clear Input (CL) is HIGH and the Enable Input ($\overline{E}$) is LOW.

When the Clear (CL) and Enable ($\overline{E}$) inputs are LOW, the selected Output (Q_0-Q_3), determined by the Address Inputs (A_0, A_1), follows the Data Input (D). When the Enable Input ($\overline{E}$) goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), changing more than one bit of the address (A_0, A_1) could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).

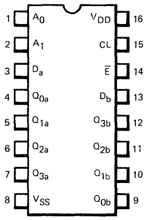
LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

- SERIAL-TO-PARALLEL CAPABILITY
- OUTPUT FROM EACH STORAGE BIT IS AVAILABLE
- RANDOM (ADDRESSABLE) DATA ENTRY
- ACTIVE HIGH DECODING OR DEMULTIPLEXING CAPABILITY
- EASILY EXPANDABLE
- ACTIVE HIGH COMMON CLEAR

CONNECTION DIAGRAM
DIP (TOP VIEW)

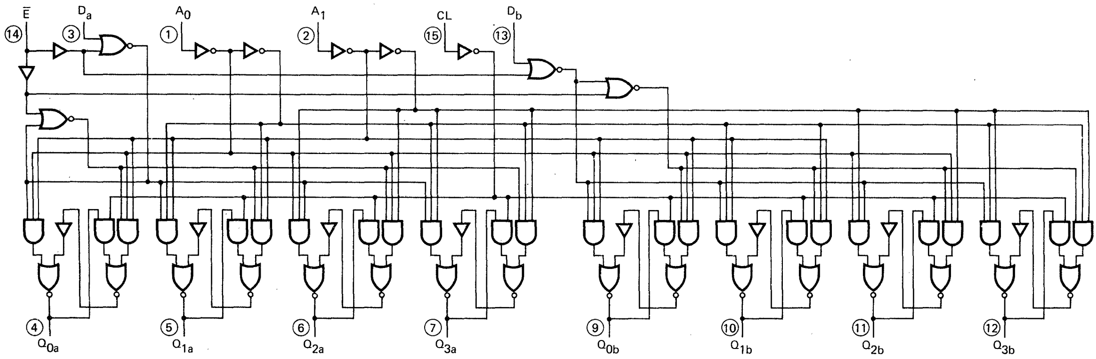


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

A_0, A_1	Address Inputs
D_a, D_b	Data Inputs
$\overline{E}$	Enable Input (Active LOW)
CL	Clear Input (Active HIGH)
Q_{0a}-Q_{3a}, Q_{0b}-Q_{3b}	Parallel Latch Outputs

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

MODE SELECTION

$\overline{E}$	CL	MODE
L	L	Addressable Latch
H	L	Memory
L	H	Dual 4-Channel Demultiplexer
H	H	Clear

H = HIGH Level
L = LOW Level

TRUTH TABLE

CL	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	MODE
H	H	X	X	X	L	L	L	L	Clear
H	L	L	L	L	L	L	L	L	Demultiplex
H	L	H	L	L	H	L	L	L	
H	L	L	H	L	L	L	L	L	
H	L	H	H	L	L	H	L	L	
H	L	L	L	H	L	L	L	L	
H	L	H	L	H	L	L	H	L	
H	L	L	H	H	L	L	L	L	
H	L	H	H	H	L	L	L	H	
L	H	X	X	X	Q_{N-1}	Q_{N-1}	Q_{N-1}	Q_{N-1}	Memory
L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}	Addressable Latch
L	L	H	L	L	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	
L	L	L	H	L	Q_{N-1}	L	Q_{N-1}	Q_{N-1}	
L	L	H	H	L	Q_{N-1}	H	Q_{N-1}	Q_{N-1}	
L	L	L	L	H	Q_{N-1}	Q_{N-1}	L	Q_{N-1}	
L	L	H	L	H	Q_{N-1}	Q_{N-1}	H	Q_{N-1}	
L	L	L	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	L	
L	L	H	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	H	

L = LOW Level
H = HIGH Level
X = Don't Care
Q_{N-1} = State before the positive transition of the Enable Input

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

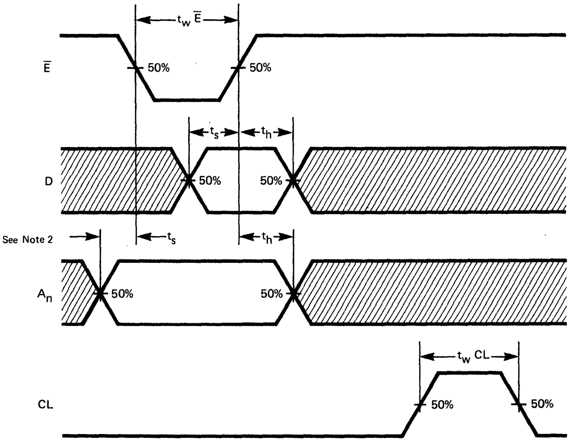
Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{E}$ to Q_n		110	225		50	100		35	80	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			110	225		50	100		35	80		
t_{PLH}	Propagation Delay, D to Q_n		95	200		45	85		30	68	ns	
t_{PHL}			95	200		45	85		30	68		
t_{PLH}	Propagation Delay,		120	250		55	100		40	80	ns	
t_{PHL}	Address to Q_n		120	250		55	100		40	80		
t_{PHL}	Propagation Delay, CL to Q_n		95	190		45	85		30	68	ns	
t_{TLH}	Output Transition Time		75	135		40	70		25	45	ns	
t_{THL}			75	135		40	70		25	45		
t_s	Set-Up Time, D to $\overline{E}$	50	30		30	10		24	5		ns	
t_h	Hold Time, D to $\overline{E}$	30	15		30	15		24	10			
t_s	Set-Up Time, Address to $\overline{E}$	90	30		35	10		28	5		ns	
t_h	Hold Time, Address to $\overline{E}$	0	-5		5	0		4	0			
$t_w\overline{E}$	Minimum $\overline{E}$ Pulse Width	70	50		35	20		28	15		ns	
t_wCL	Minimum CL Pulse Width	70	50		35	20		28	15		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

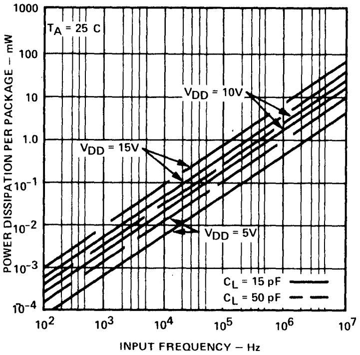
SWITCHING WAVEFORMS



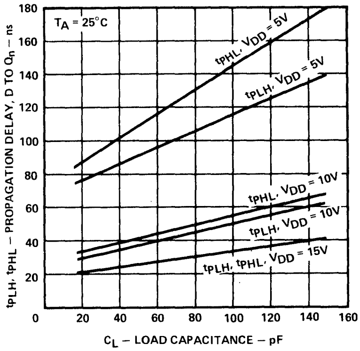
MINIMUM PULSE WIDTH FOR $\overline{E}$ AND CL AND SET-UP AND HOLD TIMES, D TO $\overline{E}$ AND A_n TO $\overline{E}$

NOTES:
1. Set-up and Hold Times are shown as positive values but may be specified as negative values.
2. The Address to Enable Set-up Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

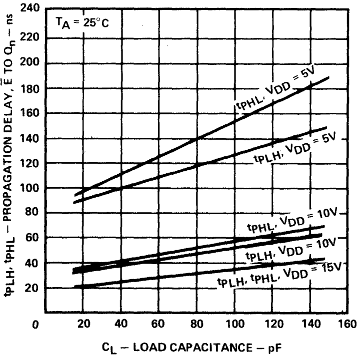
TYPICAL ELECTRICAL CHARACTERISTICS



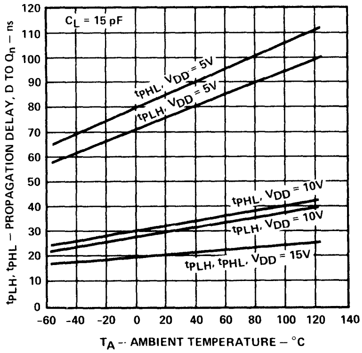
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY, D TO Q_n, VERSUS LOAD CAPACITANCE



PROPAGATION DELAY, $\overline{E}$ TO Q_n, VERSUS LOAD CAPACITANCE



PROPAGATION DELAY, D TO Q_n, VERSUS TEMPERATURE

4724B

8-BIT ADDRESSABLE LATCH

DESCRIPTION – The 4724B is an 8-Bit Addressable Latch with three Address Inputs (A_0–A_2), a Data Input (D), an active LOW Enable Input ($\overline{E}$), an active HIGH Clear Input (CL) and eight Parallel Latch Outputs (Q_0–Q_7).

When the Enable ($\overline{E}$) and the Clear (CL) Inputs are HIGH, all Outputs (Q_0-Q_7) are LOW. Eight-channel demultiplexing or active HIGH 1-of-8 decoding with output enable operation occurs when the Clear Input (CL) is HIGH and the Enable Input ($\overline{E}$) is LOW.

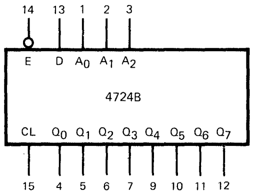
When the Clear (CL) and Enable ($\overline{E}$) Inputs are LOW, the selected Output (Q_0-Q_7) (determined by the address Inputs A_0-A_2) follows the Data Input (D). When the Enable Input ($\overline{E}$) goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), changing more than one bit of the address (A_0-A_2) could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).

- **SERIAL-TO-PARALLEL CAPABILITY**
- **EIGHT BITS OF STORAGE WITH THE OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON ACTIVE HIGH CLEAR**

PIN NAMES

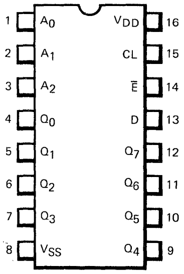
A_0-A_2	Address Inputs
D	Data Input
$\overline{E}$	Enable Input (Active LOW)
CL	Clear Input (Active HIGH)
Q_0-Q_7	Parallel Latch Outputs

LOGIC SYMBOL



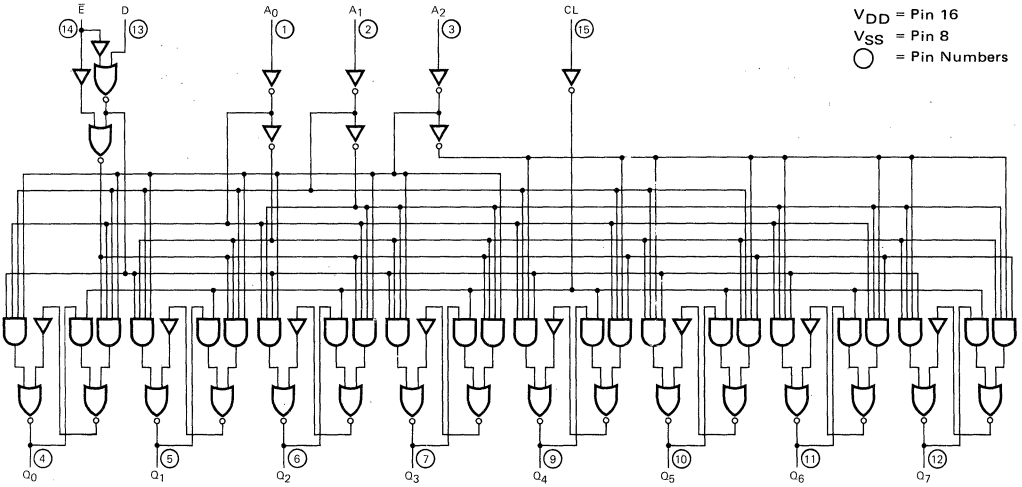
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

MODE SELECTION

$\overline{E}$	CL	MODE
L	L	Addressable Latch
H	L	Memory
L	H	Active HIGH 8-Channel Demultiplexer
H	H	Clear

L = LOW Level
H = HIGH Level

TRUTH TABLE

						PRESENT OUTPUT STATES								
CL	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
H	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
H	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
H	L	H	L	L	L	H	L	L	L	L	L	L	L	
H	L	L	H	L	L	L	L	L	L	L	L	L	L	
H	L	H	H	L	L	L	H	L	L	L	L	L	L	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
H	L	H	H	H	H	L	L	L	L	L	L	L	H	
L	H	X	X	X	X	Q_{N-1} ⟶								MEMORY
L	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} ⟶					ADDRESSABLE LATCH
L	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} ⟶						
L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} ⟶						
L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} ⟶						
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮						
L	L	L	H	H	H	Q_{N-1} ⟶						Q_{N-1}	L	
L	L	H	H	H	H	Q_{N-1} ⟶						Q_{N-1}	H	

L = LOW Level
H = HIGH Level
X = Don't Care
Q_{N-1} = State Before the Positive Transition of the Enable Input

---

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

Notes on following page.

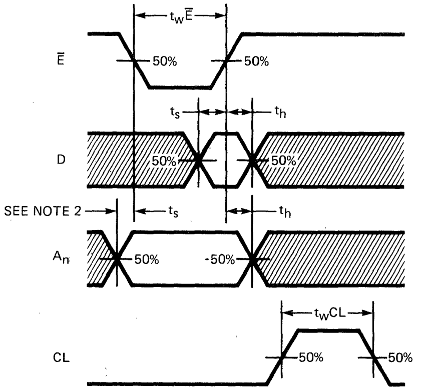
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25°C$ (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{E}$ to Q_n		110	225		50	100		35	80	ns	$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			110	225		50	100		35	80		
t_{PLH}	Propagation Delay, D to Q_n		95	200		45	85		30	68	ns	
t_{PHL}			95	200		45	85		30	68		
t_{PLH}	Propagation Delay,		120	250		55	100		40	80	ns	
t_{PHL}	Address to Q_n		120	250		55	100		40	80		
t_{PHL}	Propagation Delay, CL to Q_n		95	190		45	85		30	68	ns	
t_{TLH}	Output Transition Time		75	135		40	70		25	45	ns	
t_{THL}			75	135		40	70		25	45		
t_s	Set-Up Time, D to $\overline{E}$	50	30		30	10		24	5		ns	
t_h	Hold Time, D to $\overline{E}$	30	15		30	15		24	10			
t_s	Set-Up Time, Address to $\overline{E}$	90	30		35	10		28	5		ns	
t_h	Hold Time, Address to $\overline{E}$	0	-5		5	0		4	0			
$t_w\overline{E}$	Minimum $\overline{E}$ Pulse Width	70	50		35	20		28	15		ns	
t_wCL	Minimum CL Pulse Width	70	50		35	20		28	15		ns	

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

SWITCHING WAVEFORMS



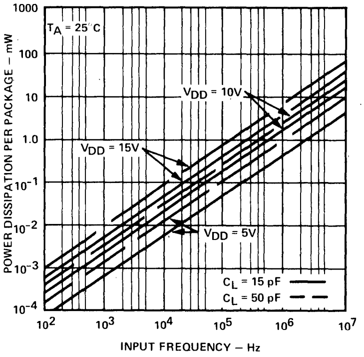
MINIMUM PULSE WIDTH FOR $\overline{E}$ AND CL AND SET-UP AND HOLD TIMES, D TO $\overline{E}$ AND A_n TO $\overline{E}$

NOTES:

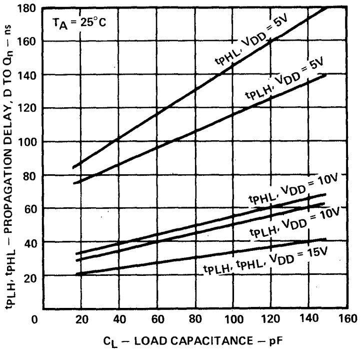
1. Set-up and Hold Times are shown as positive values but may be specified as negative values.
2. The Address to Enable Set-up Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

TYPICAL ELECTRICAL CHARACTERISTICS

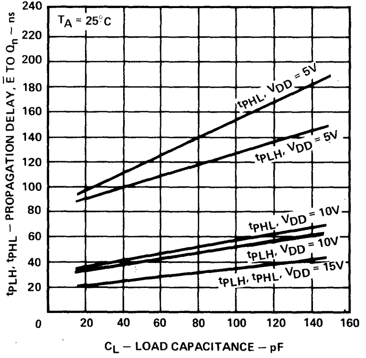
POWER DISSIPATION VERSUS FREQUENCY



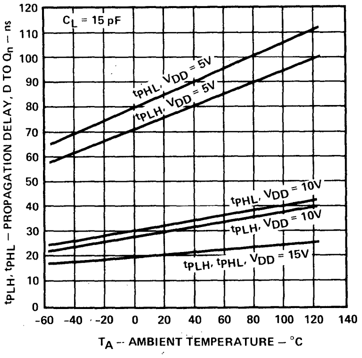
PROPAGATION DELAY, D TO Q_n, VERSUS LOAD CAPACITANCE



PROPAGATION DELAY, $\overline{E}$ TO Q_n, VERSUS LOAD CAPACITANCE



PROPAGATION DELAY, D TO Q_n, VERSUS TEMPERATURE



4725B/4725BX

64-BIT (16×4) RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

DESCRIPTION – The 4725B/4725BX is a 64-Bit Random Access Memory with 3-State Outputs organized as 16 words by four bits with four Data Inputs (D_0-D_3), four Address Inputs (A_0-A_3), an active LOW Write Enable Input ($\overline{WE}$), an active LOW Chip Select Input ($\overline{CS}$) and four active LOW 3-State Outputs ($\overline{Q}_0$-$\overline{Q}_3$).

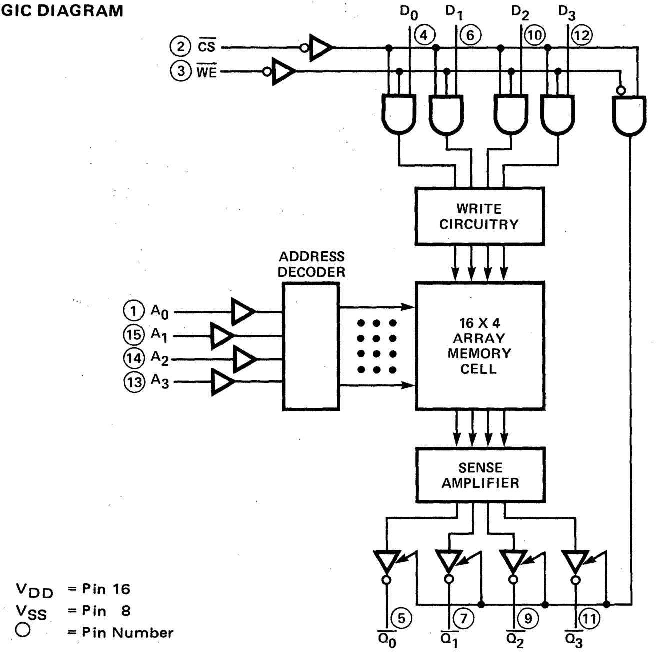
Information on the four Data Inputs (D_0-D_3) is written into the memory location selected by the Address Inputs (A_0-A_3) when both the Chip Select Input ($\overline{CS}$) and the Write Enable Input ($\overline{WE}$) are LOW. Under these conditions, the Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are held in a high impedance OFF state. Information is read from the memory location selected by the Address Inputs (A_0-A_3) while the Chip Select Input ($\overline{CS}$) is LOW and the Write Enable Input ($\overline{WE}$) is HIGH. The Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are the complement of the information written into the memory. When the Chip Select Input ($\overline{CS}$) is HIGH, all Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are held in the high impedance OFF state. This allows other 3-State outputs to be wired together in a bus arrangement. The 4725B/A725BX offers fully static operation. The 4725B is specified to operate over a power supply voltage range of 4.5 to 12.5V. The 4725BX is specified to operate over a power supply voltage range of 3 to 15V.

- **3-STATE OUTPUTS**
- **ORGANIZATION – 16 WORDS X 4 BITS**
- **ON-CHIP DECODING**
- **INVERTED DATA OUTPUT**
- **FULLY STATIC OPERATION**
- **TYPICAL HOLDING VOLTAGE OF 1.5V**

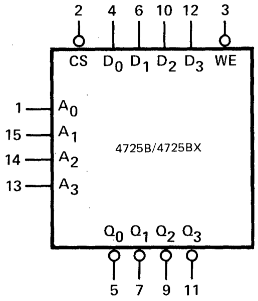
MODE SELECTION

$\overline{CS}$	$\overline{WE}$	OUTPUTS	MODE
L	L	High Impedance	Write
L	H	Outputs are Complement of Data Written into Location	Read
H	X	High Impedance	Inhibit

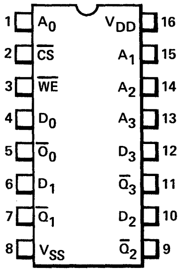
LOGIC DIAGRAM



LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



V_{DD} = Pin 16
V_{SS} = Pin 8

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

$\overline{CS}$	Chip Select Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
D_0-D_3	Data Inputs
A_0-A_3	Address Inputs
$\overline{Q}_0$-$\overline{Q}_3$	3-State Outputs (Active LOW)

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{CS}$ = V_{DD}
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{CS}$ = V_{DD}
											- 12		MAX	
		XM									-0.4		MIN, 25°C	
											- 12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20		MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
	READ MODE											C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PLH}	Propagation Delay,		250	500		98	196		65	130	ns	
t_{PHL}	Address to Output		250	500		98	196		65	130		
t_{PZH}	Enable Time, $\overline{CS}$ to Output		55	110		24	50		18	36	ns	R_L = 1 kΩ to V_{SS}
t_{PZL}			66	135		30	60		22	44		R_L = 1 kΩ to V_{DD}
t_{PHZ}	Disable Time, $\overline{CS}$ to Output		53	100		33	66		28	56	ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}			60	120		30	60		23	46		R_L = 1 kΩ to V_{DD}
t_{TLH}	Output Transition Time		65	130		30	60		25	50	ns	
t_{THL}			75	150		35	70		25	50		
	WRITE MODE											
t_{PZH}	Enable Time, $\overline{WE}$ to Output		69	138		28	56		20	40	ns	R_L = 1 kΩ to V_{SS}
t_{PZL}			83	166		35	70		24	48		R_L = 1 kΩ to V_{DD}
t_{PHZ}	Disable Time, $\overline{WE}$ to Output		60	120		26	52		18	36	ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}			72	144		32	64		24	48		R_L = 1 kΩ to V_{DD}
$t_{w\overline{WE}}$	Minimum $\overline{WE}$ Pulse Width	160	79		72	36		52	26		ns	
t_s	Set-Up Time, D_n to $\overline{WE}$	170	85		80	39		60	30		ns	
t_h	Hold Time, D_n to $\overline{WE}$	24	12		12	6		7	3			
t_s	Set-Up Time, Address to $\overline{WE}$	300	150		160	80		120	60		ns	
t_h	Hold Time, Address to $\overline{WE}$	0	-40		0	-20		30	-15			
t_s	Set-Up Time, $\overline{CS}$ to $\overline{WE}$	300	150		160	80		120	60		ns	
t_h	Hold Time, $\overline{CS}$ to $\overline{WE}$	80	40		40	20		30	15			

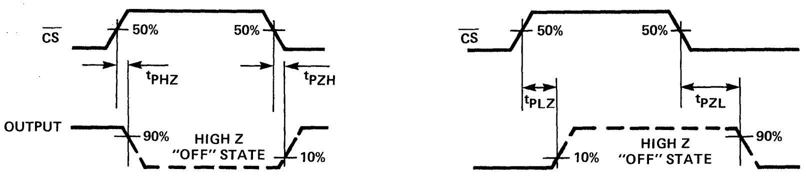
Notes on following page

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. All Set-Up (t_s) and Hold (t_h) times are measured with minimum Write Enable Pulse Width ($t_W\overline{WE}$).

SWITCHING WAVEFORMS

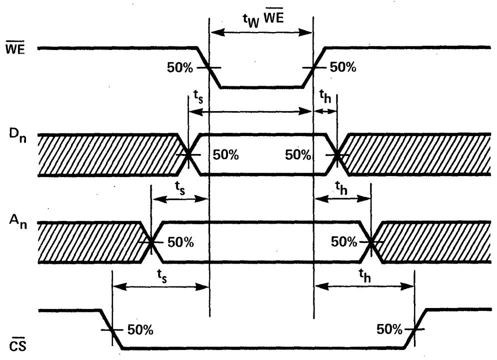
READ MODE



$\overline{CS}$ TO OUTPUT ENABLE AND DISABLE TIMES

WRITE MODE

$\overline{WE}$ TO OUTPUT ENABLE AND DISABLE TIMES



MINIMUM $\overline{WE}$ PULSE WIDTH AND SET-UP AND HOLD TIMES, D_n TO $\overline{WE}$, A_n TO $\overline{WE}$, AND $\overline{CS}$ TO $\overline{WE}$

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

4727B

7-STAGE COUNTER

DESCRIPTION – The 4727B is a 7-Stage Frequency Counter especially useful for frequency synthesis in musical applications. The device is designed to generate, from a primary chromatic scale, each of the twelve flats, sharps, and naturals comprising each chromatic scale of the seven additional octaves in the musical spectrum. Twelve 4727B devices are required to generate the entire musical spectrum from a primary scale.

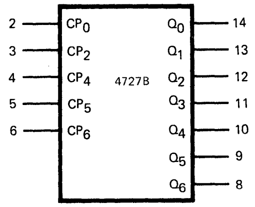
The 4727B consists of a pair of 2-Bit Counters, with Clock Inputs (CP_0 and CP_2) and Parallel Outputs (Q_0 and Q_1, Q_2 and Q_3), available, and three 1-bit counters, also with Clock Inputs (CP_4, CP_5, and CP_6) and Parallel Outputs (Q_4, Q_5, and Q_6) available. Each counter advances on a LOW-to-HIGH transition at the appropriate Clock Input.

- **REPEATS A PRIMARY MUSICAL NOTE OR HALF NOTE IN SEVEN OCTAVES**
- **CLOCK INPUT EDGE – TRIGGERED ON THE LOW-TO-HIGH TRANSITION**
- **BUFFERED OUTPUTS AVAILABLE FROM ALL SEVEN STAGES**

PIN NAMES

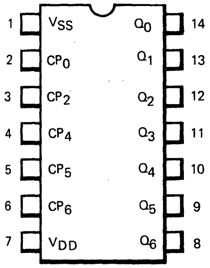
CP_0-CP_6	CLOCK INPUTS (L→H TRIGGERED)
Q_0-Q_6	PARALLEL OUTPUTS

LOGIC SYMBOL



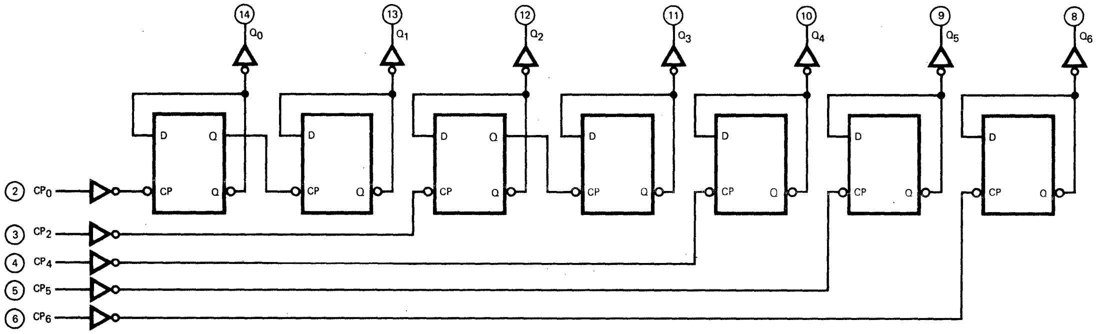
V_{DD} = PIN 7
V_{SS} = PIN 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

BLOCK DIAGRAM



V_{DD}= PIN 7
V_{SS}= PIN 1
○ = PIN NUMBER

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

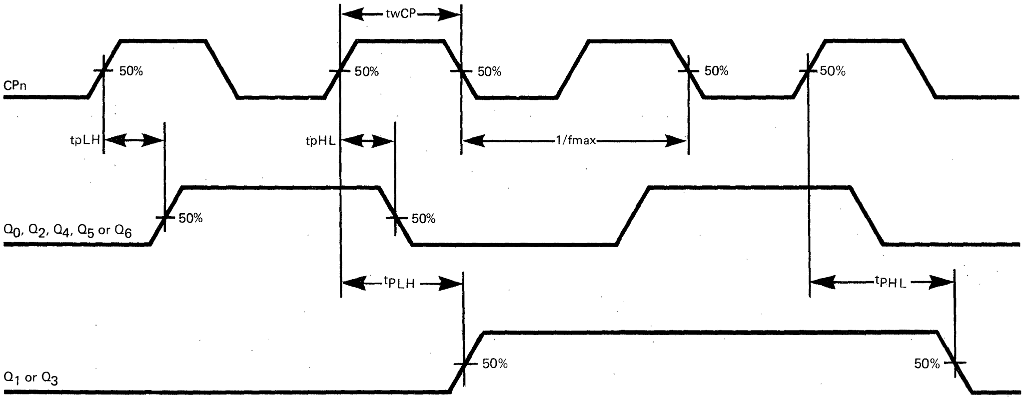
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS	
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V						
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
I_{OH}	Output High Current		-0.3			-0.84			-1.8			mA	MIN	$V_{OUT} = 4.5$ V For $V_{DD} = 5$ V. $V_{OUT} = 9.5$ V For $V_{DD} = 10$ V. $V_{OUT} = 13.5$ V For $V_{DD} = 15$ V.	Inputs at V_{SS} or V_{DD} Per the Logic Function or Truth Table
			-0.25			-0.7			-1.5				25° C		
			-0.2			-0.56			-1.1				MAX		
I_{OL}	Output Low Current		0.64			1.6			4.2			mA	MIN	$V_{OUT} = 0.4$ V for $V_{DD} = 5$ V $V_{OUT} = 0.5$V for $V_{DD} = 10$ V $V_{OUT} = 1.5$ V for $V_{CC} = 15$ V	
			0.51			1.3			3.4				25° C		
			0.36			0.9			2.4				MAX		
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN,25° C	All Inputs at V_{DD} or V_{SS}	
					150			300			600		MAX		
		XM			5			10			20	µA	MIN,25° C		
					150			300			600		MAX		

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25$° C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP_n to Q_0, Q_2, Q_4, Q_5 or Q_6		225 225	500 500		90 90	250 250		75 75	200 200	ns	$C_L = 50$ pF $R_L = 200$ kΩ Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP_n to Q_1 or Q_3		365 365	1000 1000		130 130	500 500		100 100	400 400	ns	
t_{TLH} t_{THL}	Output Transition Times		70 70	500 500		40 40	250 250		30 30	200 200	ns	
T_{wCP}	Min Clock Pulse Width	250	125		125	65		100	50		ns	
f_{MAX}	Input Count Frequency (Note 3)	2	4		4	8		5	10		MHz	

NOTES:
1. Additional DC characteristics are listed in this section under "4000B Series CMOS Family Characteristics."
2. Propagation Delays and Output Transition Times are graphically described in this section under "4000B Series CMOS Family Characteristics."
3. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.

SWITCHING WAVEFORMS



PROPAGATION DELAY, CP to Qn, MINIMUM CLOCK PULSE WIDTH AND MAXIMUM FREQUENCY

4731B/4731BX

QUAD 64-BIT STATIC SHIFT REGISTER

DESCRIPTION – The 4731B/4731BX is a Quad 64-Bit Shift Register each with separate Serial Data Inputs (D_A-D_D), Clock Inputs ($\overline{CP}_A$-$\overline{CP}_D$) and Data Outputs (Q_{63A}-Q_{63D}) from the 64th register position.

Information present on the Serial Data Inputs is shifted into the first register position and all the data in the register is shifted one position to the right on a HIGH-to-LOW transition of the Clock Inputs ($\overline{CP}_A$-$\overline{CP}_D$).

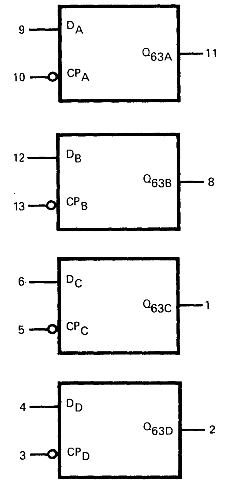
Low impedance outputs are provided for direct interface to TTL. The 4731B is specified to operate over a power supply voltage range of 4.5 V to 12.5 V, the 4731BX is specified to operate over a power supply voltage range of 3 V to 15 V.

- **FREQUENCIES UP TO 8 MHz AT V_{DD} = 10 V**
- **SERIAL-TO-SERIAL DATA TRANSFER**
- **SEPARATE CLOCK INPUTS, DATA INPUTS AND FULLY BUFFERED OUTPUTS FOR EACH REGISTER**
- **DIRECT INTERFACE TO TTL**
- **14-PIN PACKAGE**

PIN NAMES

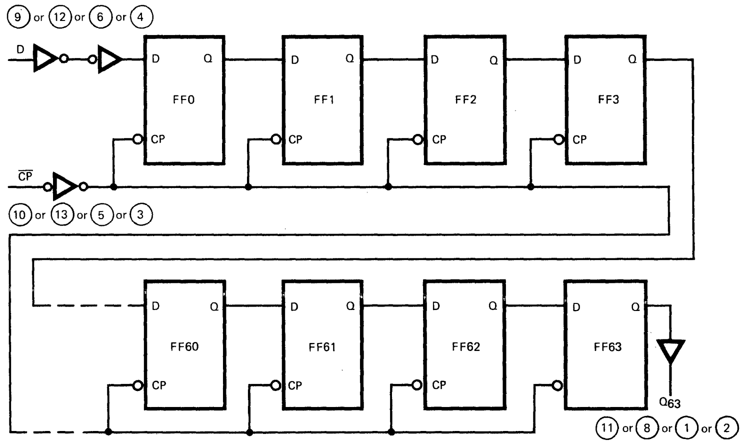
D_A-D_D	Serial Data Inputs
$\overline{CP}_A$-$\overline{CP}_D$	Clock Input (H→L Edge-Triggered)
Q_{63A}-Q_{63D}	Buffered Outputs from the 64th Register Position

LOGIC SYMBOL



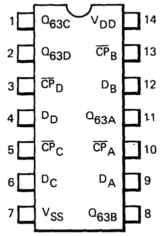
V_{DD} = Pin 14
V_{SS} = Pin 7

LOGIC DIAGRAM
1/4 OF A 4731B/4731BX

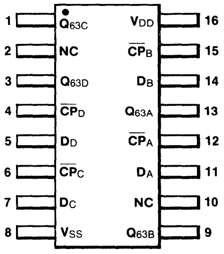


V_{DD}= Pin 14
V_{SS} = Pin 7
○ = Pin Number

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			100			200			400	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					750			1500			3000		MAX	
		XM			25			50			100	µA	MIN, 25°C	
					750			1500			3000		MAX	

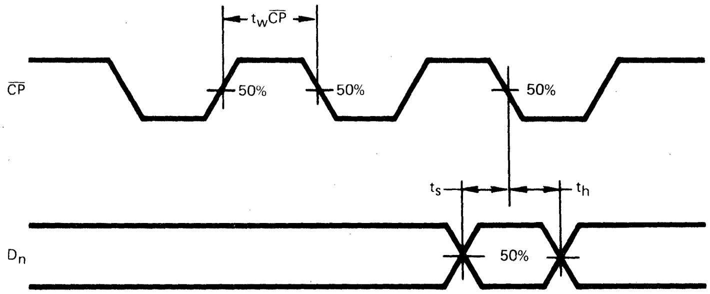
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_{63}		190 190	450 450		95 95	200 200		65 65	160 160	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{TLH} t_{THL}	Output Transition Time		45 30	135 90		30 30	70 50		20 20	45 35	ns	
$t_w\overline{CP}$	$\overline{CP}$ Minimum Pulse Width	300	100		150	50		120	40		ns	
t_s t_h	Set-Up Time D to $\overline{CP}$ Hold Time D to $\overline{CP}$	100 100	-20 35		40 40	-12 12		40 40	-7 11		ns	
f_{MAX}	Max. Input Clock Frequency (Note 3)	1.5	4		3	8		4	14		MHz	

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH
AND SET-UP AND HOLD TIMES, D TO $\overline{CP}$

NOTE:

1. Set-up and Hold Times are shown as positive values but may be specified as negative values.

4741B

4 x 4 CROSS POINT SWITCH

DESCRIPTION – The 4741B is a 4 X 4 Crosspoint Switch consisting of a 16-Bit Addressable Latch and 16 independent bi-directional analog switches arranged in a four by four matrix such that any analog switch or any combination of analog switches may be ON or OFF at any one time providing a multitude of analog input/output switching combinations.

The device has four Address Inputs (A_0-A_3), a Data Input (D), an Enable Input (E) and eight independent analog Input/Outputs (Y_0-Y_3 and Z_0-Z_3). When the Enable Input (E) is HIGH, the selected Output (Q_0-Q_{15}) of the 16-Bit Addressable Latch (determined by the Address Inputs, A_0-A_3) follows the Data Input (D) thus turning the selected analog switch ON or OFF. With the Data Input (D) HIGH, any one of the 16 analog switches may be individually turned ON by first applying the appropriate Address Inputs (A_0-A_3) and then taking the Enable Input (E) HIGH. With the Data Input (D) LOW, any one of the 16 switches may be individually turned OFF by first applying the appropriate Address Inputs (A_0-A_3) and then taking the Enable Input (E) HIGH. The Enable Input (E) may remain HIGH as long as the Address Inputs (A_0-A_3) are stable. However, to prevent erroneous switch selection the Enable Input (E) must be LOW whenever the Address Inputs (A_0-A_3) are changed.

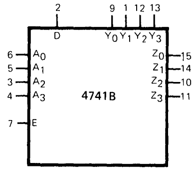
Although only one switch at a time may be turned ON or OFF, any number or combination of switches may be ON or OFF at any one time.

- **LOW ON RESISTANCE–TYPICALLY 85Ω at V_{DD} = 10V**
- **ON-CHIP ADDRESS DECODER AND CONTROL LATCHES**
- **INPUT SIGNAL FREQUENCIES UP TO 10 MHz**
- **ANALOG OR DIGITAL CROSSPOINT SWITCH**

PIN NAMES

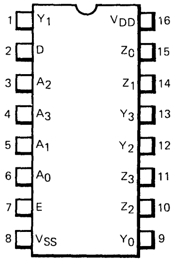
Y_0-Y_3	Analog Input/Outputs
Z_0-Z_3	Analog Input/Outputs
A_0-A_3	Address Inputs
D	Data Input
E	Enable Input

LOGIC SYMBOL



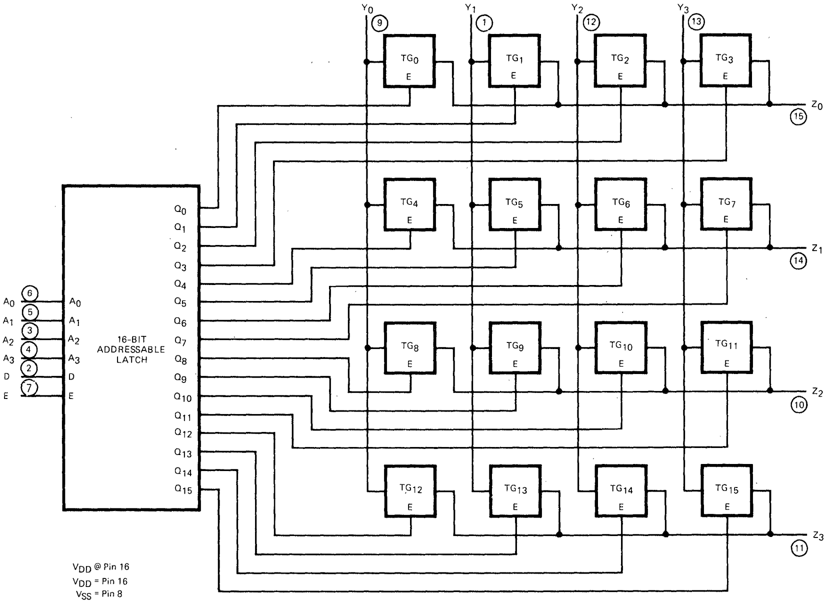
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

BLOCK DIAGRAM



V_{DD} @ Pin 16
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number
TG = Transmission Gale

TRUTH TABLE

INPUTS						CHANNELS															
E	A_3	A_2	A_1	A_0	D	Y_0-Z_0	Y_1-Z_0	Y_2-Z_0	Y_3-Z_1	Y_0-Z_1	Y_1-Z_1	Y_2-Z_1	Y_3-Z_1	Y_0-Z_2	Y_1-Z_2	Y_2-Z_2	Y_3-Z_2	Y_0-Z_3	Y_1-Z_3	Y_2-Z_3	Y_3-Z_3
L	X	X	X	X	X	NC															
H	L	L	L	L	L	OFF	NC														
H	L	L	L	L	H	ON	NC														
H	L	L	L	H	L	NC	OFF	NC													
H	L	L	L	H	H	NC	ON	NC													
H	L	L	H	L	L	NC		OFF	NC												
H	L	L	H	L	H	NC		ON	NC												
H	L	L	H	H	L	NC			OFF	NC											
H	L	L	H	H	H	NC			ON	NC											
H	L	H	L	L	L	NC				OFF	NC										
H	L	H	L	L	H	NC				ON	NC										
H	L	H	L	H	L	NC					OFF	NC									
H	L	H	L	H	H	NC					ON	NC									
H	L	H	H	L	L	NC						OFF	NC								
H	L	H	H	L	H	NC						ON	NC								
H	L	H	H	H	L	NC							OFF	NC							
H	L	H	H	H	H	NC							ON	NC							
H	H	L	L	L	L	NC								OFF	NC						
H	H	L	L	L	H	NC								ON	NC						
●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
H	H	H	H	H	L	NC															OFF
H	H	H	H	H	H	NC															ON

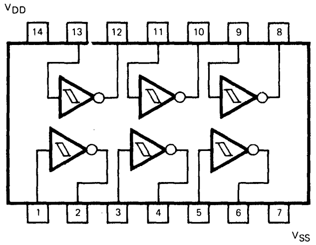
L = LOW level
H = HIGH level
X = Don't Care
NC = No Change

40014B/74C14/54C14

HEX SCHMITT TRIGGER

DESCRIPTION – The 40014B is a general purpose Hex Schmitt Trigger offering positive and negative threshold voltages, V_{T+} and V_{T-}, which show very low variation with temperature (typically 0.0005V/°C at V_{DD} = 10V) and guaranteed hysteresis, V_{T+} to $V_{T-} \geqslant 0.2\ V_{DD}$. Outputs are fully buffered for highest noise immunity. The 40014B is a direct replacement for the 74C14/54C14.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The flatpak version has the same pinouts (Connection Diagram) as the dual in-line package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

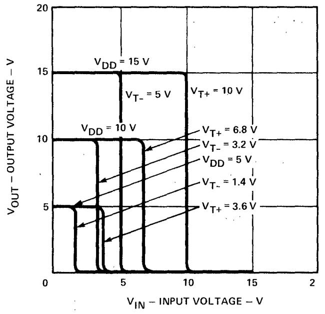
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
V_{T+}	Positive-Going Threshold Voltage		2.9	3.6	4.3	6	6.8	8.6	9	10	12.9	V	All	$V_{IN} = V_{SS}$ to V_{DD}
V_{T-}	Negative-Going Threshold Voltage		0.7	1.4	1.9	1.4	3.2	4	2.1	5	6	V	All	$V_{IN} = V_{DD}$ to V_{SS}
V_{T+} to V_{T-}	Hysteresis		1	2.2	3.6	2	3.6	7.2	3	5	10.8	V	All	Guaranteed Hysteresis = V_{T+} Minus V_{T-}
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	µA	MIN, 25°C	All Inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	µA	MIN, 25°C	
					7.5			15			30		MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C.

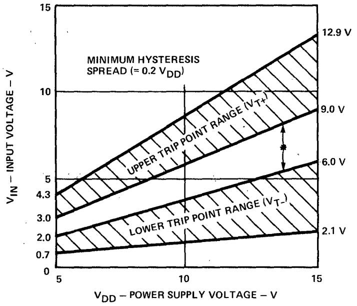
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS (See Note 2)
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		90	200		42	100		35	80	ns	C_L = 50 pF,
t_{PHL}			90	200		42	100		35	80		R_L = 200 kΩ
t_{TLH}	Output Transition Time		70	135		30	75		22	45	ns	Input Transition
t_{THL}			70	135		30	75		22	45		Times ≤ 20 ns

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

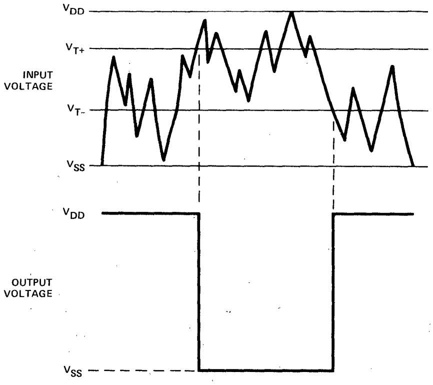
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL
TRANSFER CHARACTERISTICS

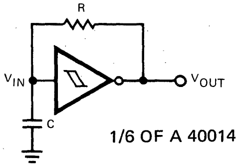


GUARANTEED TRIP
POINT RANGE

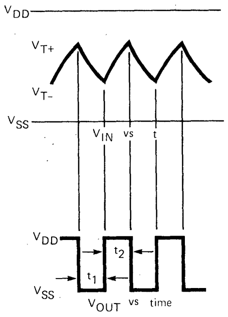


LOW POWER OSCILLATOR

TYPICAL APPLICATION



1/6 OF A 40014B



$$t_1 = RC\,Ln\left(\frac{V_{T+}}{V_{T-}}\right)$$

$$t_2 = RC\,Ln\left(\frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}}\right)$$

$$f \approx \frac{1}{RC\,L_n\left[\frac{V_{T+}(V_{DD} - V_{T-})}{V_{T-}(V_{DD} - V_{T+})}\right]}$$

NOTE:
The equations assume that $t_1 + t_2 \gg t_{PLH} + t_{PHL}$.

40085B/74C85/54C85

4-BIT MAGNITUDE COMPARATOR

DESCRIPTION – The 40085B is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0-A_3,B_0-B_3); A_3,B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the 40085B under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

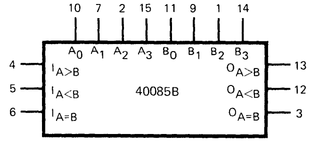
The 40085B is a direct replacement for the 74C85/54C85.

- **EASILY EXPANDABLE**
- **BINARY OR BCD COMPARISON**
- **$O_{A>B}$, $O_{A<B}$, AND $O_{A=B}$ OUTPUTS AVAILABLE**

PIN NAMES

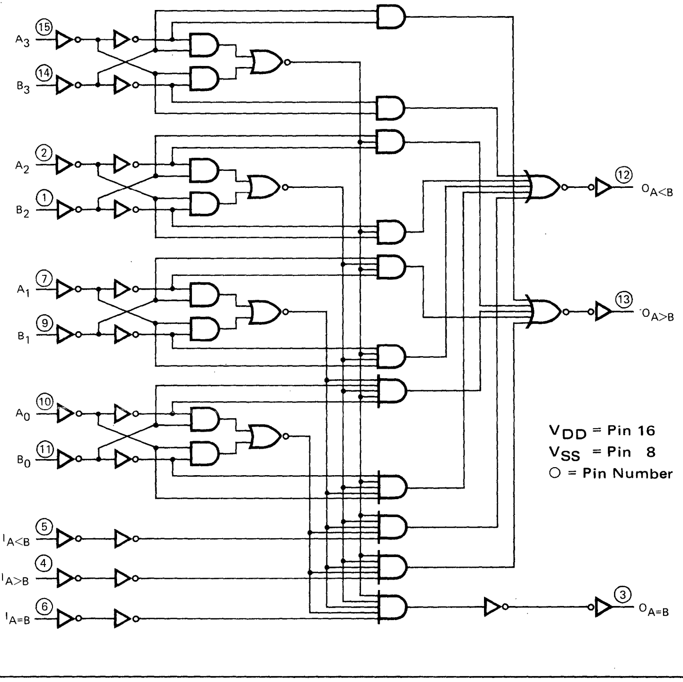
A_0-A_3	Word A Parallel Inputs
B_0-B_3	Word B Parallel Inputs
$I_{A>B}$, $I_{A<B}$, $I_{A=B}$	Expander Inputs
$O_{A>B}$	A Greater than B Output
$O_{A<B}$	A Less than B Output
$O_{A=B}$	A Equal to B Output

LOGIC SYMBOL



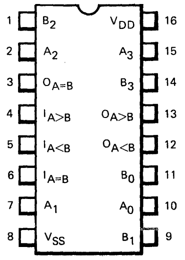
V_{DD} = Pin 16
V_{SS} = Pin 8

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	H	L	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	H	H	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	H	H	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	H	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

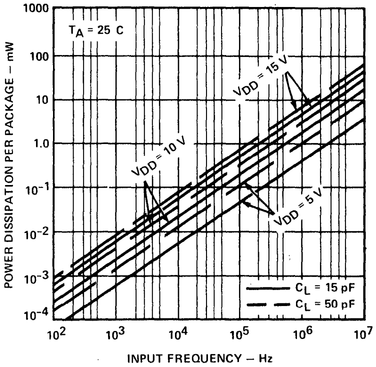
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25°C$ (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, A_n or B_n to any Output		180 180	335 335		70 70	140 140		50 50	112 112	ns	$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, Any I to any Output		135 135	275 275		55 55	120 120		40 40	96 96	ns	
t_{TLH} t_{THL}	Output Transition Time		60 60	135 135		30 30	70 70		20 20	45 45	ns	

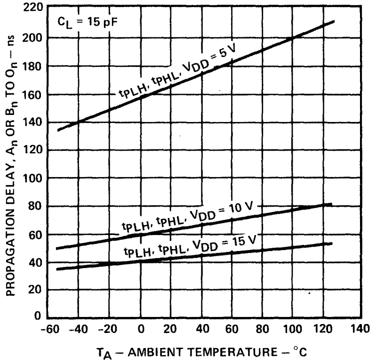
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

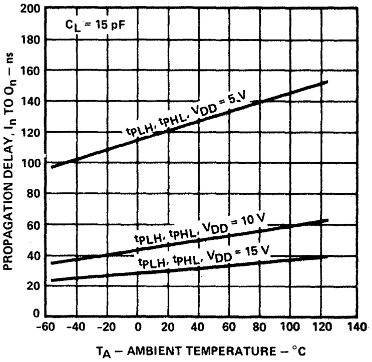
POWER DISSIPATION VERSUS FREQUENCY



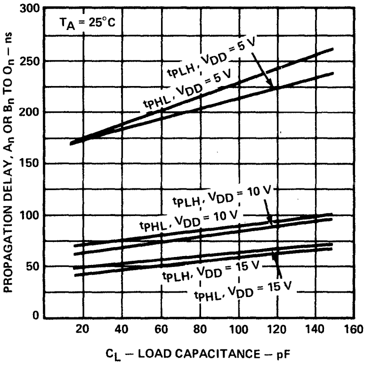
PROPAGATION DELAY A_n OR B_n TO O_n, VERSUS TEMPERATURE



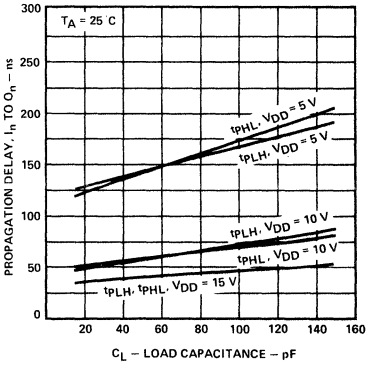
PROPAGATION DELAY I_n TO O_n VERSUS TEMPERATURE



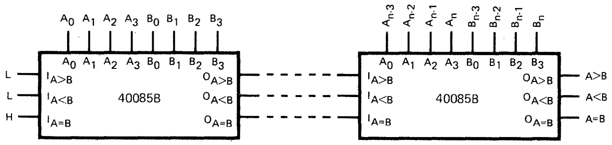
PROPAGATION DELAY A_n OR B_n TO O_n VERSUS LOAD CAPACITANCE



PROPAGATION DELAY I_n TO O_n VERSUS LOAD CAPACITANCE



APPLICATIONS



L = LOW Level
H = HIGH Level

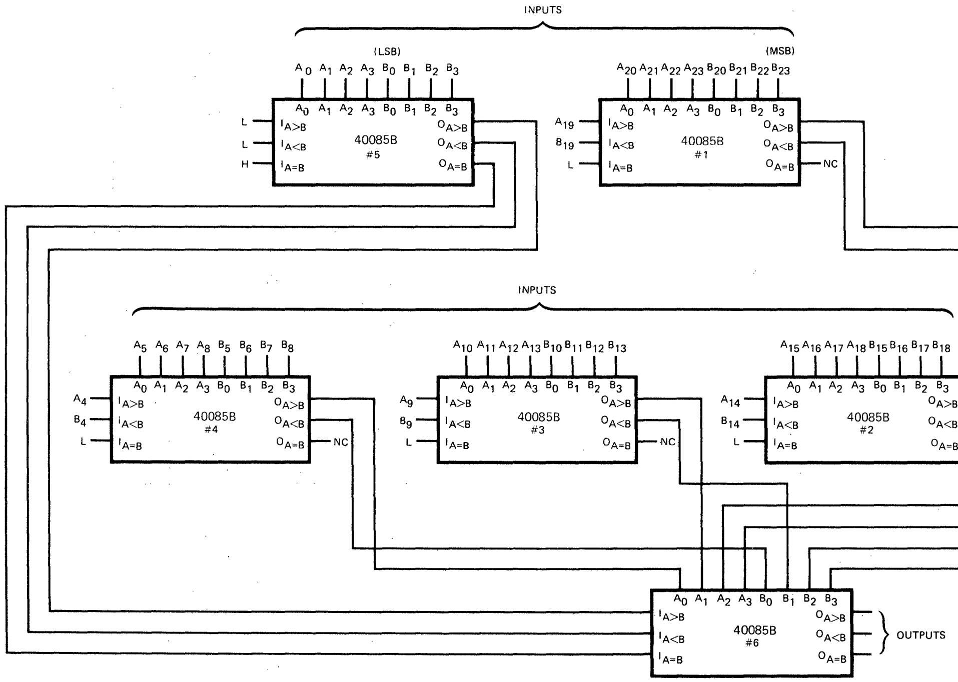
Fig. 1. COMPARING TWO n-BIT WORDS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table I.

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2 - 6
25-120 Bits	8 - 31

NOTE:
The F40085 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another 40085B as shown in Figure 2 in positions #1, 2, 3, and 4.



MSB = Most Significant Bit
LSB = Least Significant Bit

L = LOW Level
H = HIGH Level
NC = No Connection

Fig. 2. COMPARISON OF TWO 24-BIT WORDS

40097B•40098B

3-STATE HEX NON-INVERTING AND INVERTING BUFFERS

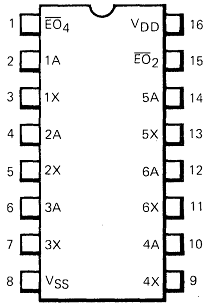
DESCRIPTION – These two CMOS buffers provide high current output capability suitable for driving high capacitance loads. The 40097B is a Non-Inverting CMOS Buffer with 3-state outputs and the 40098B is an Inverting CMOS Buffer with 3-state outputs. The 3-state outputs of each device are controlled by two Enable Inputs ($\overline{EO}_4$, $\overline{EO}_2$). A HIGH on Enable Input $\overline{EO}_4$ causes the Outputs of four of the six buffer elements to assume a high impedance or OFF state, regardless of other input conditions and a HIGH on Enable Input $\overline{EO}_2$ causes the Outputs of the remaining two buffer elements to assume a high impedance or OFF state, regardless of other input conditions.

- **3-STATE OUTPUTS**
- **TTL COMPATIBLE – FAN OUT OF ONE TTL LOAD**
- **ACTIVE LOW ENABLE INPUTS**

PIN NAMES

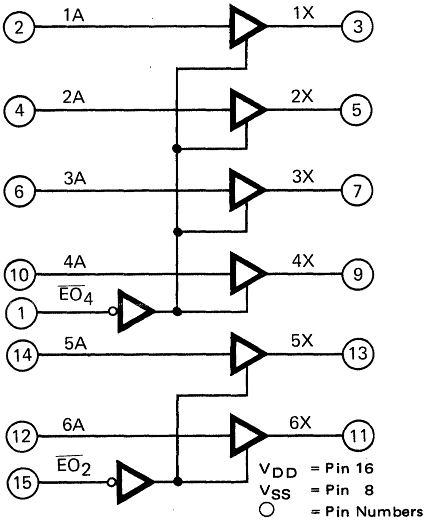
1A-6A	Buffer Inputs
$\overline{EO}_4$, $\overline{EO}_2$	Enable Inputs (Active LOW)
1X-6X	Buffer Outputs (Active HIGH for the 40097B and Active LOW for the 40098B)

CONNECTION DIAGRAM
DIP (TOP VIEW)

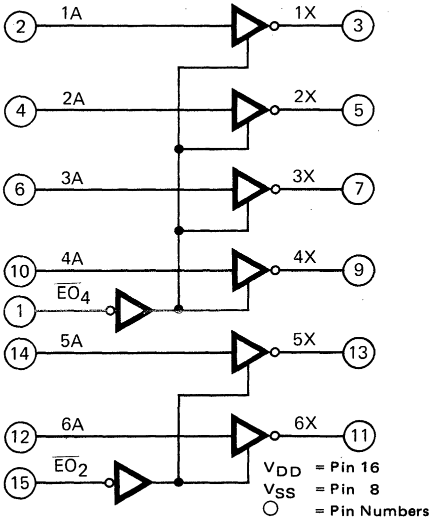


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

40097B LOGIC DIAGRAM



40098B LOGIC DIAGRAM



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OH}	Output HIGH Current		-1.0			-2.0			-3.2			mA	MIN, 25°C	V_{OUT} = 4.5 V for V_{DD} = 5 V V_{OUT} = 9.5 V for V_{DD} = 10 V V_{OUT} = 14.5 V for V_{DD} = 15 V Inputs at V_{SS} or V_{DD} Per Logic Function
			-0.7			-1.4			-2.2				MAX	
I_{OL}	Output LOW Current		2.5			6.25			11.25			mA	MIN, 25°C	V_{OUT} = 0.4 V for V_{DD} = 5 V V_{OUT} = 0.5 V for V_{DD} = 10 V V_{OUT} = 0.5 V for V_{DD} = 15 V Inputs at V_{SS} or V_{DD} Per Logic Function
			1.8			4.5			8.25				MAX	
I_{OZH}	Output OFF Current HIGH	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}_n = V_{DD}$
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}_n = V_{DD}$
											-12		MAX	
		XM									-0.4		MIN, 25°C	
											-12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			4			8			16	μA	MIN, 25°C	All Inputs at 0 V or V_{DD}
					30			60			120		MAX	
		XM			1			2			4		MIN, 25°C	
					30			60			120		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 40097B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		65	100		25	40		20	32	ns	C_L = 50 pF,
t_{PHL}	Data to Output		80	100		28	40		20	32		R_L = 200 kΩ
t_{PZH}	Output Enable Time		70	110		35	55		29	44	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			95	150		40	65		30	52		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable Time		40	65		31	55		29	44	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			60	95		35	55		30	44		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		40	65		25	40		15	30	ns	Input Transition
t_{THL}			30	60		15	30		15	30		Times ≤ 20 ns

Notes on following page.

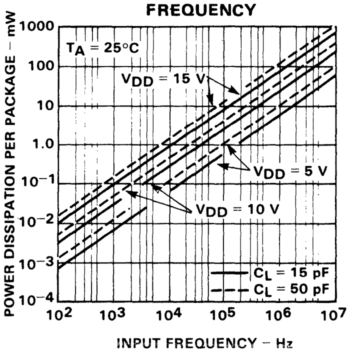
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 40098B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, Data to Output		65	120		30	55		30	44	ns	C_L = 50 pF,
t_{PHL}			85	155		35	65		30	52		R_L = 200 kΩ
t_{PZH}	Output Enable Time		70	110		35	55		29	44	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			95	170		40	60		30	48		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Outside Disable Time		40	70		31	55		29	44	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			60	105		35	55		30	44		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		40	65		25	40		15	30	ns	Input Transition
t_{THL}			30	60		15	30		15	30		Times ≤ 20 ns

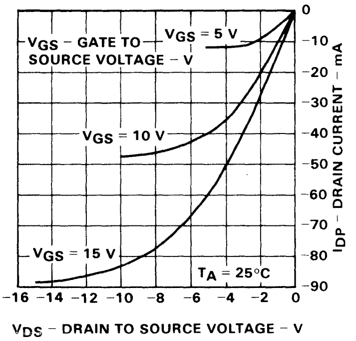
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

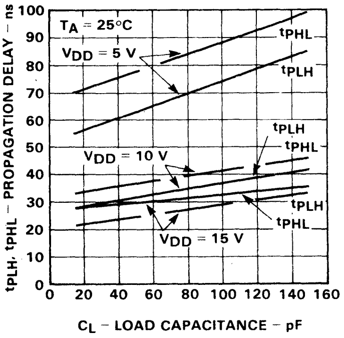
40097B/40098B
POWER DISSIPATION VERSUS FREQUENCY



40097B/40098B
P-CHANNEL DRAIN CHARACTERISTICS

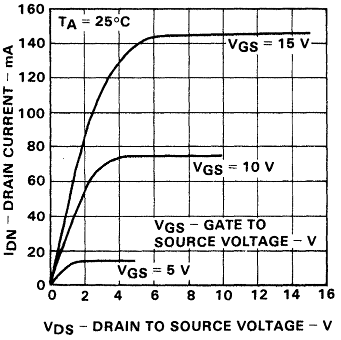


40098B
PROPAGATION DELAY VERSUS LOAD CAPACITANCE

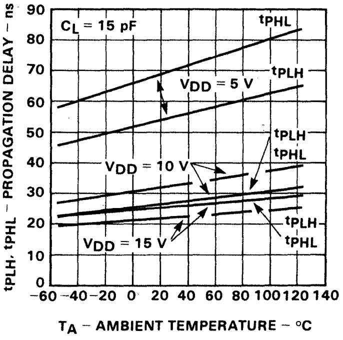


TYPICAL ELECTRICAL CHARACTERISTICS (Cont'd)

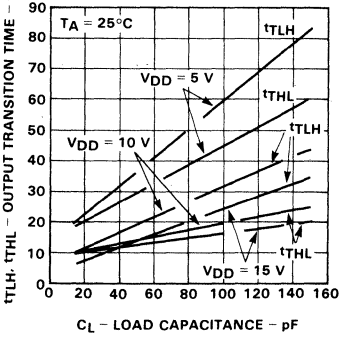
40098B
N-CHANNEL DRAIN CHARACTERISTICS



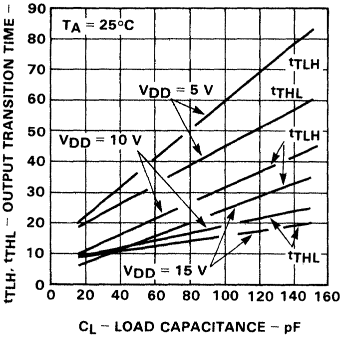
40098B
PROPAGATION DELAY VERSUS TEMPERATURE



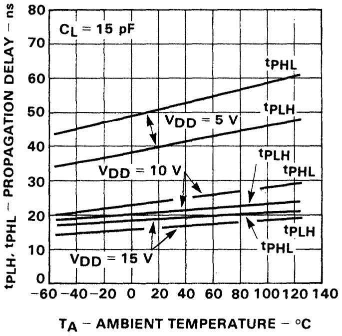
40098B
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



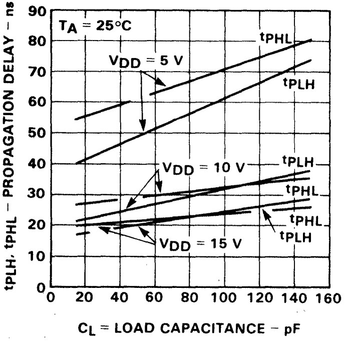
40097B
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



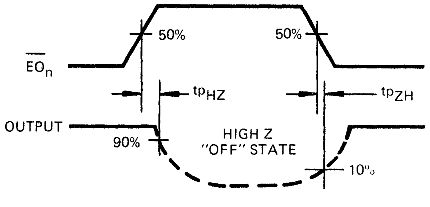
40097B
PROPAGATION DELAY VERSUS TEMPERATURE



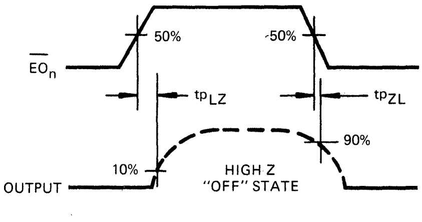
40097B
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORMS



OUTPUT ENABLE TIME
(t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME
(t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

40161B/74C161/54C161
40163B/74C163/54C163
4-BIT SYNCHRONOUS COUNTERS

DESCRIPTION – The 40161B and the 40163B are fully synchronous edge-triggered 4-Bit Binary Counters. Each device has a Clock Input (CP); four synchronous Parallel Data Inputs (P_0-P_3); three synchronous Mode Control Inputs, Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable trickle (CET); Buffered Outputs from all four bit positions (Q_0-Q_3); and a Terminal Count Output (TC). The 40163B has an additional synchronous Mode Control Input, Synchronous Reset ($\overline{SR}$). Alternately, the 40161B has an overriding asynchronous Master Reset ($\overline{MR}$).

Operation is fully synchronous except for Master Reset on the 40161B and occurs on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input ($\overline{PE}$) is LOW, the next LOW-to-HIGH transition of the Clock Input (CP) loads data into the counter from Parallel Inputs (P_0-P_3). When the Parallel Enable Input ($\overline{PE}$) is HIGH, the next LOW-to-HIGH transition of the Clock Input (CP) advances the counter to its next state only if both Count Enable Inputs (CEP and CET) are HIGH when the state of the counter is fifteen ($Q_0 = Q_1 = Q_2 = Q_3$ = HIGH) for the 40161B and 40163B and the Count Enable Trickle Input (CET) is HIGH. For the 40163B a LOW on the Synchronous Reset Input ($\overline{SR}$) sets all Outputs (Q_0-Q_3 and TC) LOW on the next LOW-to-HIGH transition of the Clock Input (CP) independent of the state of all other synchronous Mode Control Inputs (CEP, CET, $\overline{PE}$). For the 40161B, a LOW on the overriding asynchronous Master Reset ($\overline{MR}$) sets all outputs (Q_0-Q_3 and TC) LOW, independent of the state of all other inputs.

These devices perform multistage synchronous counting without additional components by using a carry look-ahead counting technique.

The 40161B, and 40163B are edge-triggered; therefore, the synchronous Mode Control Input (CEP, CET, $\overline{PE}$ for the 40161B and CEP, CET, $\overline{PE}$, $\overline{SR}$ for the 40163B) must be stable only during the set-up time before the LOW-to-HIGH transition of the Clock Input (CP).

The 40161B and 40163B are direct replacements for the 74C161/54C161 and 74C163/54C163 respectively.

- **12 MHz TYPICAL COUNT FREQUENCY AT V_{DD} = 10 V**
- **DECODED TERMINAL COUNT**
- **FULLY SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **SYNCHRONOUS (40163B) OR ASYNCHRONOUS (40161B) RESET**
- **BUILT-IN CARRY CIRCUITRY**
- **FULLY EDGE-TRIGGERED**

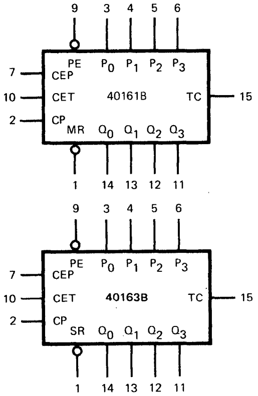
PIN NAMES

$\overline{PE}$	Parallel Enable Input (Active LOW)
P_0-P_3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Input (L → H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW) for the 40160B/40161B Only
$\overline{SR}$	Synchronous Reset Input (Active LOW) for the 40162B/40163B Only
Q_0-Q_3	Parallel Outputs
TC	Terminal Count Output

SELECTOR GUIDE

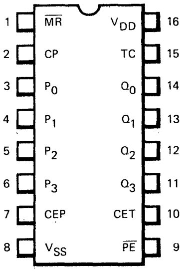
RESET	MODULUS
	BINARY
Asynchronous	40161B
Synchronous	40163B

LOGIC SYMBOL

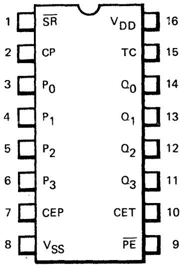


V_{DD} = PIN 16, V_{SS} = PIN 8

40161B CONNECTION DIAGRAM DIP (TOP VIEW)



40163B CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

SYNCHRONOUS MODE SELECTION 40161B

$\overline{PE}$	CEP	CET	MODE
L	X	X	Preset
H	L	X	No Change
H	X	L	No Change
H	H	H	Count

$\overline{MR}$ = HIGH

SYNCHRONOUS MODE SELECTION 40163B

$\overline{SR}$	$\overline{PE}$	CEP	CET	MODE
H	L	X	X	Preset
H	H	L	X	No Change
H	H	X	L	No Change
H	H	H	H	Count
L	X	X	X	Reset

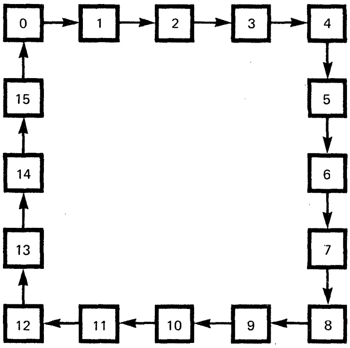
TERMINAL COUNT GENERATION

CET	40161B/40163B ($Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$)	TC
L	L	L
L	H	L
H	L	L
H	H	H

TC = CET • $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$ (40161B/40163B)

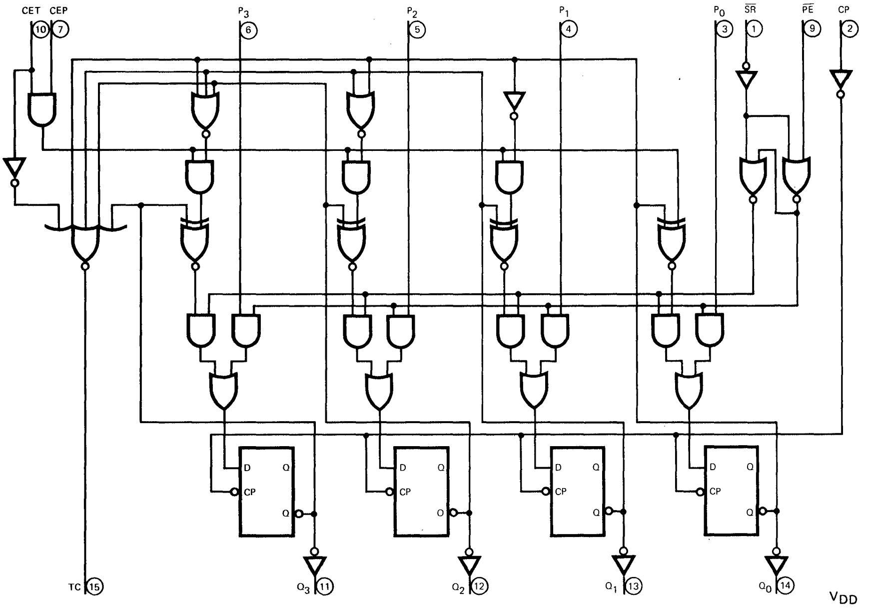
H = HIGH Level
L = LOW Level
X = Don't Care

STATE DIAGRAM 40161B • 40163B



40161B/40163B LOGIC DIAGRAM

The 40161B and 40163B binary synchronous counters are similar.



V_{DD} = PIN 16
V_{SS} = PIN 8
○ = PIN NUMBERS

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

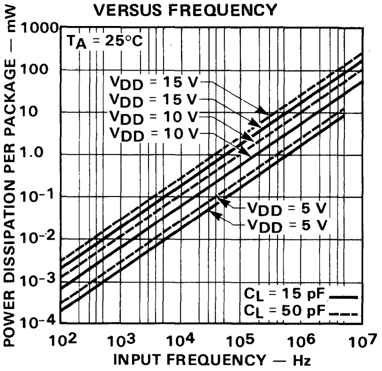
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25°C$ (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to Q		120 120	220 220		55 55	105 105		40 38	84 84	ns	$C_L = 50$ pF, $R_L = 200$ kΩ Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to TC		155 155	285 285		70 70	130 130		45 40	104 104	ns	
t_{PLH} t_{PHL}	Propagation Delay, CET to TC		95 95	165 165		40 55	80 95		27 36	64 76	ns	
t_{TLH} t_{THL}	Output Transition Time		60 70	135 135		35 30	70 70		25 23	45 45	ns	
t_wCP	CP Minimum Pulse Width	90	50		40	20		32	15		ns	
t_s t_h	Set-Up Time, Data to CP Hold Time, Data to CP	70 0	35 -30		35 0	18 -15		28 0	13 -10		ns	
t_s t_h	Set-Up Time, $\overline{PE}$ to CP Hold Time, $\overline{PE}$ to CP	110 -10	60 -57		60 -5	30 -28		48 -4	20 -18		ns	
t_s t_h	Set-Up Time, CEP, CET to CP Hold Time, CEP, CET to CP	200 -20	115 -110		95 -10	50 -48		76 -8	35 -32		ns	
f_{MAX}	Input Count Frequency (Note 3)	3	6		7	12		8	14		MHz	

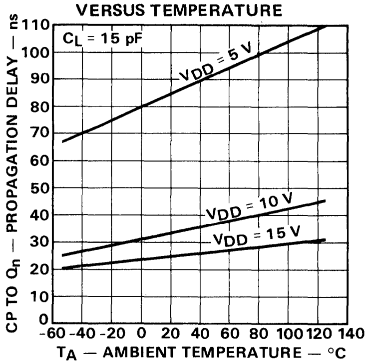
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at $V_{DD} = 5$ V, 4 µs at $V_{DD} = 10$ V, and 3 µs at $V_{DD} = 15$ V.

TYPICAL ELECTRICAL CHARACTERISTICS

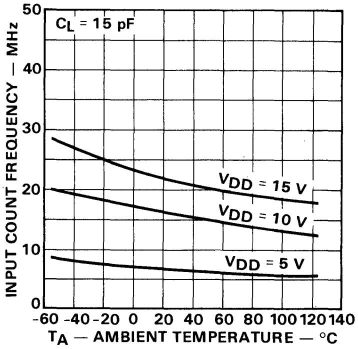
POWER DISSIPATION VERSUS FREQUENCY



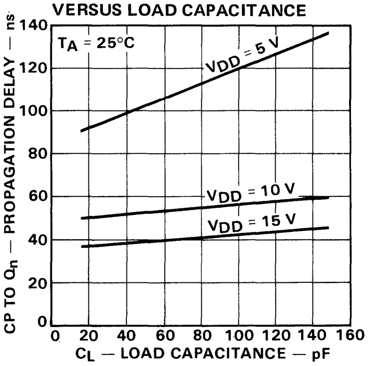
PROPAGATION DELAY VERSUS TEMPERATURE



INPUT COUNT FREQUENCY VERSUS TEMPERATURE

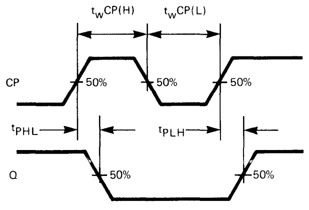


PROPAGATION DELAY VERSUS LOAD CAPACITANCE



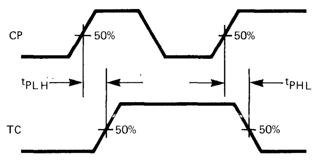
SWITCHING DIAGRAMS

CLOCK (CP) TO OUTPUT (Q) PROPAGATION DELAYS AND MINIMUM CLOCK PULSE WIDTH



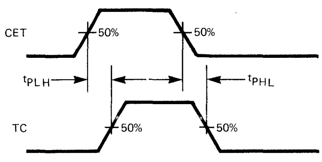
CONDITIONS: $\overline{PE}$ = $\overline{MR}$ = CEP = CET = H for 40161B and $\overline{PE}$ = $\overline{SR}$ = CEP = CET = H for 40163B.

CLOCK (CP) TO TERMINAL COUNT (TC) PROPAGATION DELAYS



CONDITIONS: See the Terminal Count Generation Table $\overline{PE}$ = CEP = CET = $\overline{MR}$ = H for 40161B and $\overline{PE}$ = CEP = CET = $\overline{SR}$ = H for 40163B.

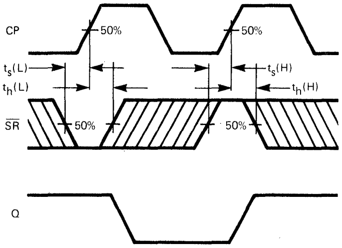
COUNT ENABLE TRICKLE INPUT (CET) TO TERMINAL COUNT OUTPUT (TC) PROPAGATION DELAYS



CONDITIONS: See the Terminal Count Generation Table. CP = $\overline{PE}$ = CEP = $\overline{MR}$ = H for 40161B and CP = $\overline{PE}$ = CEP = $\overline{SR}$ = H for 40163B.

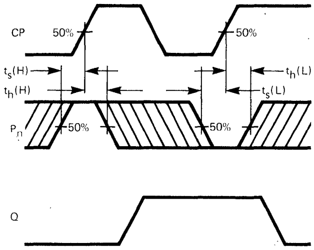
SWITCHING DIAGRAMS (Continued)

40163B
SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR SYNCHRONOUS RESET ($\overline{SR}$).



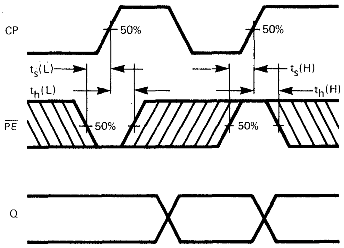
CONDITIONS: $\overline{PE}$ = L, P_0-P_3 = H.

SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR PARALLEL DATA INPUTS (P_0-P_3).



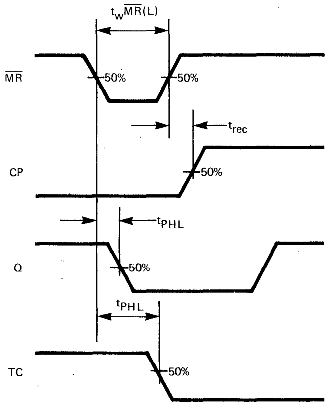
CONDITIONS: $\overline{PE}$ = L, $\overline{MR}$ = H for 40161B and $\overline{PE}$ = L, $\overline{SR}$ = H for 40163B.

SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR PARALLEL ENABLE INPUT PE.



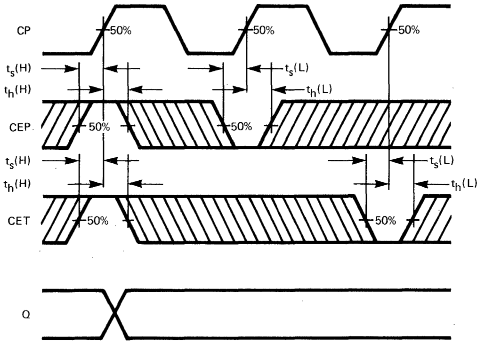
CONDITIONS: $\overline{MR}$ = H for 40161B and $\overline{SR}$ = H for 40163B.

40161B
MASTER RESET ($\overline{MR}$) TO OUTPUT (Q) DELAY, MASTER RESET PULSE WIDTH, MASTER RESET RECOVERY TIME, AND MASTER RESET TO TERMINAL COUNT (TC) DELAY.



CONDITIONS: $\overline{PE}$ = L and P_0 = P_1 = P_2 = P_3 = H.

SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR COUNT ENABLE INPUTS (CEP AND CET).



CONDITIONS: $\overline{PE}$ = $\overline{MR}$ = H for 40160B/40161B and $\overline{PE}$ = $\overline{SR}$ = H for 40162B/40163B.

NOTE:
1. Set-up Times (t_s) and Hold Times (t_h) are shown as positive values, but may be specified as negative values.

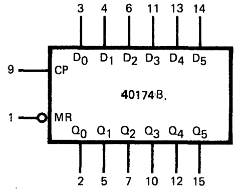
40174B/74C174/54C174

HEX D FLIP-FLOP

DESCRIPTION – The 40174B is a Hex Edge-Triggered D Flip-Flop with six Data Inputs (D_0-D_5), a Clock Input (CP) an overriding asynchronous Master Reset ($\overline{MR}$), and six Buffered Outputs (Q_0-Q_5).

Information on the Data Inputs (D_0-D_5) is transferred to the Buffered Outputs (Q_0-Q_5) on the LOW-to-HIGH transition of the Clock Input (CP) if the Master Reset Input ($\overline{MR}$) is HIGH. When LOW, the Master Reset Input ($\overline{MR}$) resets all flip-flops (Q_0-Q_5 = LOW) independent of the Clock (CP) and Data Inputs (D_0-D_5). The 40174B is a direct replacement for the 74C174/54C174.

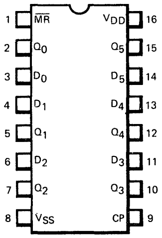
LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

- **TYPICAL CLOCK FREQUENCY OF 16 MHz AT V_{DD} = 10 V**
- **COMMON CLOCK TRIGGERED ON LOW-TO-HIGH TRANSITION**
- **COMMON ACTIVE LOW MASTER RESET**
- **FULLY EDGE-TRIGGERED CLOCK INPUT**

CONNECTION DIAGRAM
DIP (TOP VIEW)

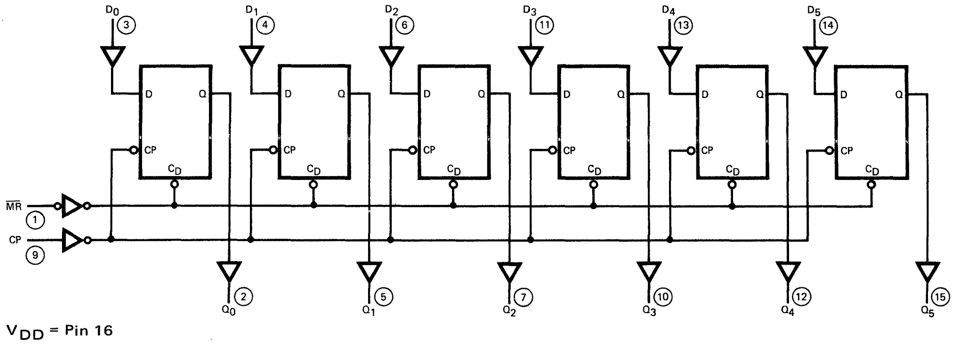


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

D_0-D_5	Data Inputs
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_5	Buffered Outputs from the Flip-Flops

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

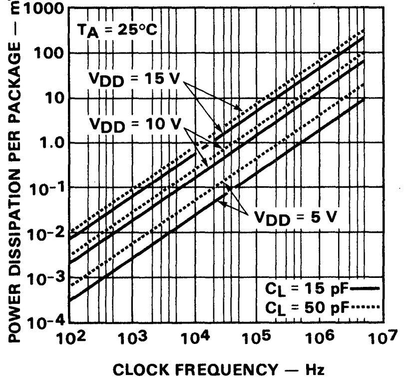
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		70	115		35	60		25	48	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			70	115		35	60		25	48		
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		80	125		40	65		25	52	ns	
t_{TLH}	Output Transition Time		65	135		35	70		15	45	ns	
t_{THL}			65	135		35	70		15	45		
$t_w CP(L)$	Minimum Clock Pulse Width	45	25		20	10		16	8		ns	
$t_w \overline{MR}(L)$	Minimum $\overline{MR}$ Pulse Width	55	35		35	20		28	15		ns	
t_{rec}	$\overline{MR}$ Recovery Time	25	6		13	5		11	2		ns	
t_s	Set-Up Time, D_n to CP	5	1		5	1		4	0		ns	
t_h	Hold Time, D_n to CP	20	10		10	2		8	1			
f_{MAX}	Max. Clock Frequency (Note 3)	5	9		8	16		9	19		MHz	

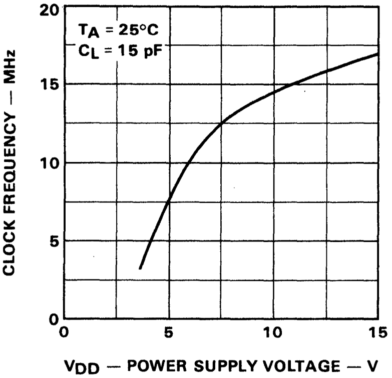
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

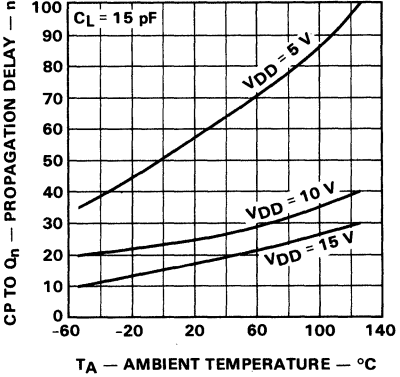
TYPICAL ELECTRICAL CHARACTERISTICS



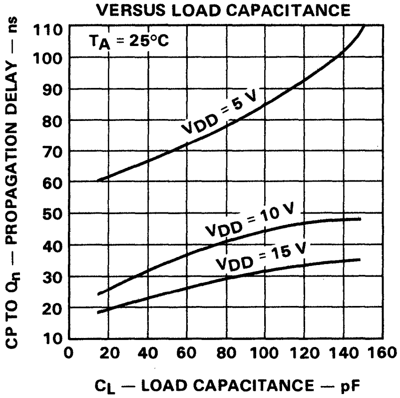
TYPICAL POWER DISSIPATION VERSUS CLOCK FREQUENCY



CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE

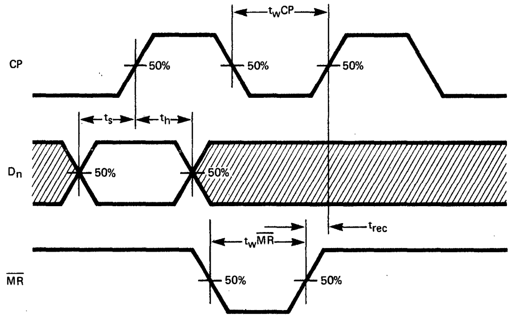


PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

SWITCHING WAVEFORM



MINIMUM PULSE WIDTHS FOR CP AND $\overline{MR}$, $\overline{MR}$ RECOVERY TIME, AND SET-UP AND HOLD TIMES, D_n TO CP

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values

40175B/74C175/54C175
QUAD D FLIP-FLOP

DESCRIPTION — The 40175B is a Quad Edge-Triggered D Flip-Flop with four Data Inputs (D_0-D_3), a Clock Input (CP) an overriding asynchronous Master Reset ($\overline{MR}$), four Buffered Outputs (Q_0-Q_3) and four Complementary Buffered Outputs ($\overline{Q}_0$-$\overline{Q}_3$).

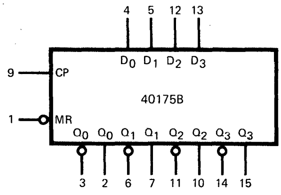
Information on the Data Inputs (D_0-D_3) is transferred to Outputs (Q_0-Q_3) on the LOW-to-HIGH Transition of the Clock Input (CP) if the Master Reset Input ($\overline{MR}$) is HIGH. When LOW, the Master Reset Input ($\overline{MR}$) resets all flip-flops (Q_0-Q_3 = LOW, $\overline{Q}_0$-$\overline{Q}_3$ = HIGH), independent of the Clock (CP) and Data (D_0-D_3) Inputs.

- **TYPICAL CLOCK FREQUENCY OF 16 MHz AT V_{DD} = 10 V**
- **COMMON CLOCK TRIGGERED ON LOW-TO-HIGH TRANSITION**
- **COMMON ACTIVE LOW MASTER RESET**
- **TRUE AND COMPLEMENTARY OUTPUTS AVAILABLE**
- **FULLY EDGE-TRIGGERED CLOCK INPUT**

PIN NAMES

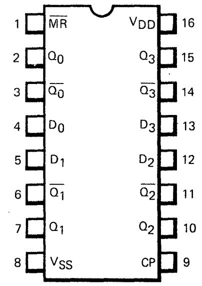
D_0-D_3	Data Inputs
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_3	Buffered Outputs from the Flip-Flops
$\overline{Q}_0$-$\overline{Q}_3$	Complimentary Buffered Outputs from the Flip-Flops

LOGIC SYMBOL



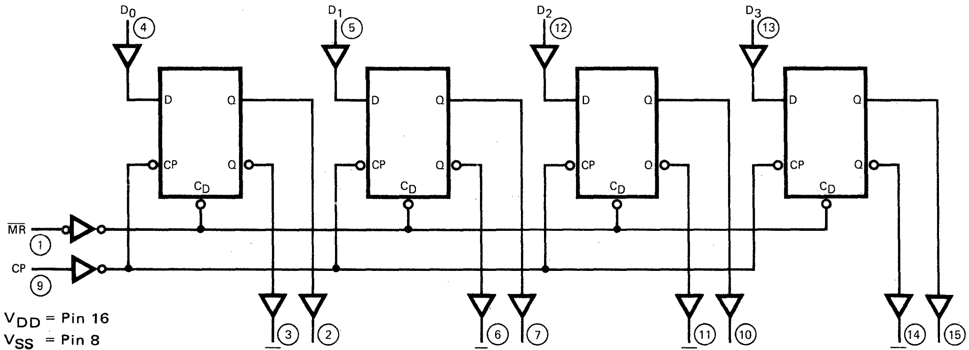
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

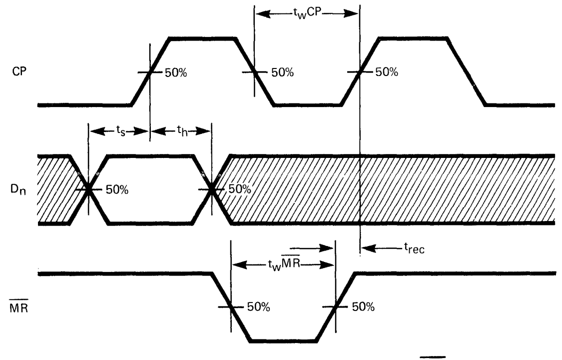
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n or $\overline{Q}_n$		70	190		35	75		25	60	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			70	190		35	75		25	60		
t_{PLH}	Propagation Delay, $\overline{MR}$ to Q_n or $\overline{Q}_n$		80	200		40	70		25	56	ns	
t_{PHL}			80	200		40	70		25	56		
t_{TLH}	Output Transition Time		65	135		35	75		15	45	ns	
t_{THL}			65	135		35	75		15	45		
t_wCP(L)	Minimum Clock Pulse Width	80	25		45	10		36	8		ns	
$t_w\overline{MR}$(L)	Minimum $\overline{MR}$ Pulse Width	60	35		30	20		24	15		ns	
t_{rec}	$\overline{MR}$ Recovery Time	0	-50		0	-25		0	-15		ns	
t_s	Set-Up Time, D_n to CP	45	20		20	7		16	3		ns	
t_h	Hold Time, D_n to CP	10	-10		5	-5		4	-3			
f_{MAX}	Max. Clock Frequency (Note 3)	4	9		10	16		12	19		MHz	

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

SWITCHING WAVEFORMS

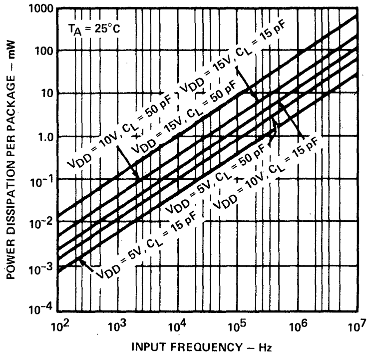


MINIMUM PULSE WIDTHS FOR CP AND $\overline{MR}$, $\overline{MR}$ RECOVERY TIME, AND SET-UP AND HOLD TIMES, D_n TO CP

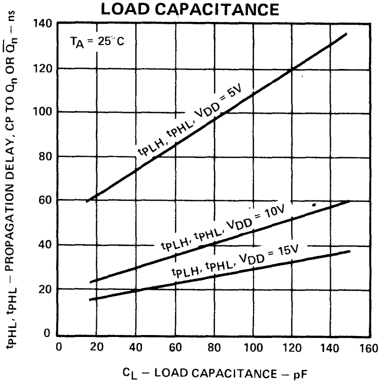
Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

TYPICAL ELECTRICAL CHARACTERISTICS

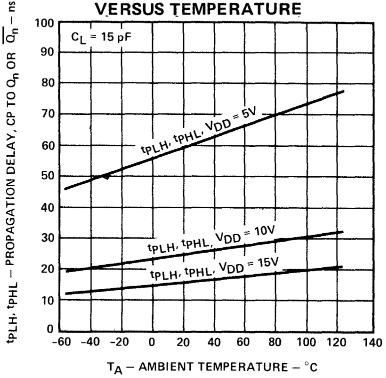
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY, CP TO Q_n OR $\overline{Q_n}$, VERSUS LOAD CAPACITANCE



PROPAGATION DELAY, CP TO $\overline{Q_n}$ OR Q_n, VERSUS TEMPERATURE



40193B/54/74C193

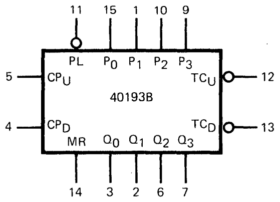
4-BIT UP/DOWN BINARY COUNTER

DESCRIPTION – The 40193B is a 4-Bit Synchronous Up/Down Binary Counter. Both operate the same except for the count sequence. Both counters have a Count Up Clock Input (CP_U), a Count Down Clock Input (CP_D), an asynchronous Parallel Load Input ($\overline{PL}$), four Parallel Data Inputs (P_0-P_3), an overriding asynchronous Master Reset (MR), four Counter Outputs (Q_0-Q_3), a Terminal Count Up (Carry) Output ($\overline{TC_U}$) and a Terminal Count Down (Borrow) Output ($\overline{TC_D}$).

When the Master Reset Input (MR) is LOW and the Parallel Load Input ($\overline{PL}$) is HIGH, the Counter Outputs change state on the LOW-to-HIGH transition of either Clock Input. However, for correct counting, both Clock Inputs cannot be LOW simultaneously. With the Master Reset Input (MR) LOW, information on the Parallel Data Inputs (P_0-P_3) is loaded into the counter when the Parallel Load Input ($\overline{PL}$) is LOW and stored in the counter when the Parallel Load Input ($\overline{PL}$) goes HIGH, independent of Clock Inputs (CP_U, CP_D). When HIGH, the Master Reset (MR) resets the counter independent of all other input conditions. See equations below for Terminal Count Outputs ($\overline{TC_U}$, $\overline{TC_D}$).

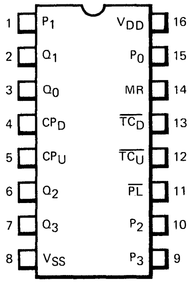
- **TYPICAL COUNT FREQUENCY OF 8 MHz AT V_{DD} = 10 V**
- **SYNCHRONOUS OPERATION**
- **INTERNAL CASCADING CIRCUITRY PROVIDED**
- **ACTIVE LOW PARALLEL LOAD**
- **ACTIVE HIGH ASYNCHRONOUS MASTER RESET**

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

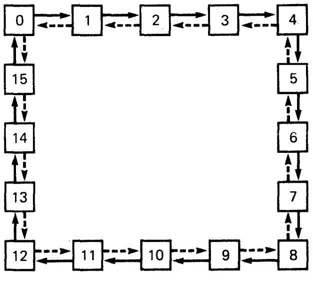
$\overline{PL}$	Parallel Load Input (Active LOW)
P_0-P_3	Parallel Data Inputs
CP_U	Count Up Clock Pulse Input (L→H Edge-Triggered)
CP_D	Count Down Clock Pulse Input (L→H Edge-Triggered)
MR	Master Reset Input (Asynchronous)
Q_0-Q_3	Buffered Counter Outputs
$\overline{TC_U}$	Buffered Terminal Count Up (Carry) Output (Active LOW)
$\overline{TC_D}$	Buffered Terminal Count Down (Borrow) Output (Active LOW)

MODE SELECTION

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	_⌐	H	Count Up
L	H	H	_⌐	Count Down

L = LOW Level
H = HIGH Level
X = Don't Care
_⌐ = Positive-Going Clock Pulse Edge

40193B STATE DIAGRAM



40193B LOGIC EQUATIONS FOR TERMINAL COUNT

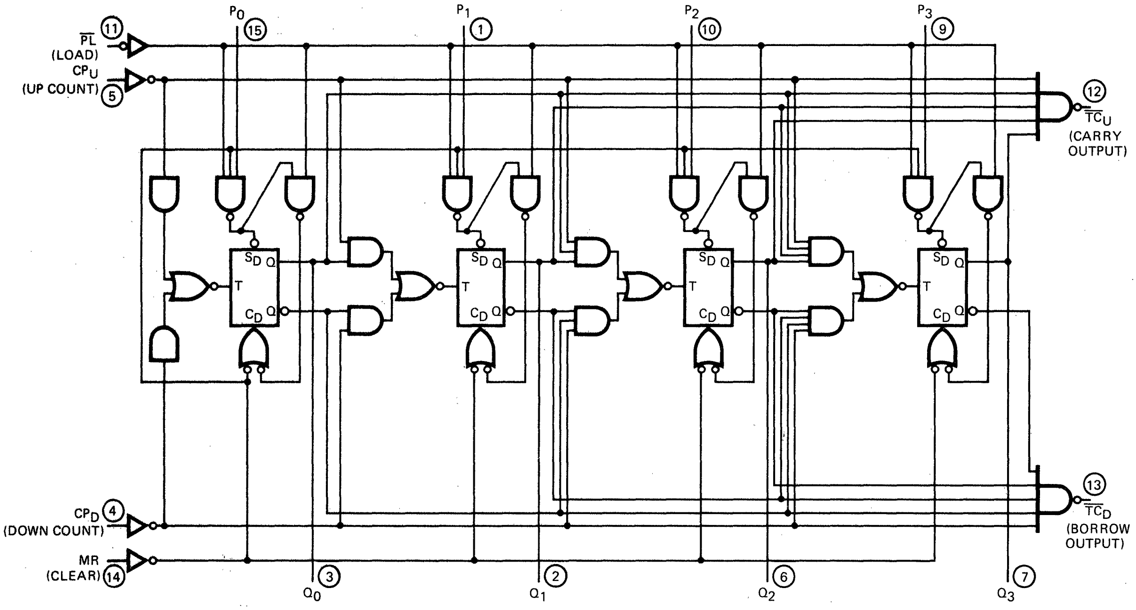
Count Up ————
Count Down -----------

$$TC_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP_U}$$

$$TC_D = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet CP_D$$

LOGIC DIAGRAMS

40193B



V_{DD} = Pin 16

V_{SS} = Pin 8

○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

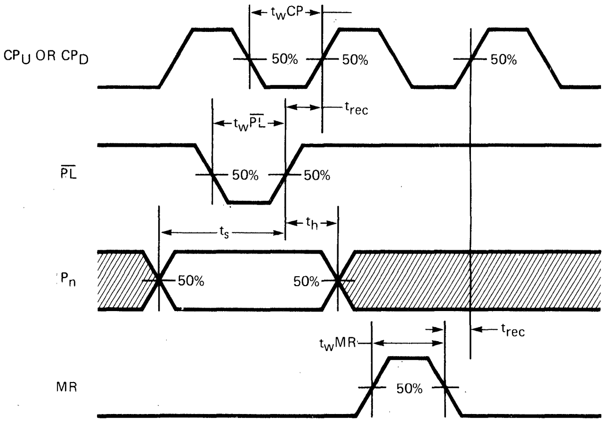
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP_U to Q_n		245	490		105	210		70	175	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			245	490		105	210		70	175		
t_{PLH}	Propagation Delay, CP_D to Q_n		245	490		105	210		70	175	ns	
t_{PHL}			245	490		105	210		70	175		
t_{PLH}	Propagation Delay, CP_U to $\overline{TC}_U$		130	260		60	120		40	96	ns	
t_{PHL}			130	260		60	120		40	96		
t_{PLH}	Propagation Delay, CP_D to $\overline{TC}_D$		145	290		60	120		40	96	ns	
t_{PHL}			145	290		60	120		40	96		
t_{PHL}	Propagation Delay, MR to Q_n		270	540		120	240		80	192	ns	
t_{PLH}	Propagation Delay, MR to $\overline{TC}_U$ or $\overline{TC}_D$		370	740		170	340		105	270	ns	
t_{PLH}	Propagation Delay, $\overline{PL}$ to Q_n		270	540		110	220		70	175	ns	
t_{PHL}			270	540		110	220		70	175		
t_{TLH}	Output Transition Time		55	135		30	75		20	45	ns	
t_{THL}			55	135		30	75		20	45		
t_wCP	Min. CP_U or CP_D Pulse Width	170	85		75	30		60	20		ns	
t_wMR	Minimum MR Pulse Width	180	60		80	30		64	20		ns	
$t_w\overline{PL}$	Minimum $\overline{PL}$ Pulse Width	150	75		85	25		52	20		ns	
t_{rec}	MR Recovery Time	150	75		65	30		52	20		ns	
t_{rec}	$\overline{PL}$ Recovery Time	150	75		65	30		52	20		ns	
t_s	Set-Up Time, P_n to $\overline{PL}$	170	85		75	30		60	20		ns	
t_h	Hold Time, P_n to $\overline{PL}$	0	-83		0	-28		0	-19			
f_{MAX}	Input Count Frequency (Note 3)	2	4		4	8		5	12		MHz	

Notes on following page.

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



RECOVERY TIMES FOR $\overline{PL}$ AND MR, MINIMUM PULSE WIDTHS FOR CP_U, CP_D, $\overline{PL}$ AND MR AND SET-UP AND HOLD TIMES P_n TO $\overline{PL}$

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

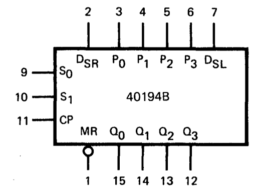
40194B

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION — The 40194B is a 4-Bit Bidirectional Shift Register with two Mode Control Inputs (S_0, S_1), a Clock Input (CP), a Serial Data Shift Left Input (D_{SL}), a Serial Data Shift Right Input (D_{SR}), four Parallel Data Inputs (P_0-P_3), an overriding asynchronous Master Reset Input ($\overline{MR}$) and four Buffered Parallel Outputs (Q_0-Q_3).

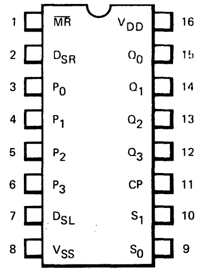
When LOW, the Master Reset Input ($\overline{MR}$) resets all stages and forces all Outputs (Q_0-Q_3) LOW, overriding all other input conditions. When the Master Reset Input ($\overline{MR}$) is HIGH, the operating mode is controlled by the two Mode Control Inputs (S_0, S_1) as shown in the Truth Table. Serial and parallel operation is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). The inputs at which the data is to be entered and the Mode Control Inputs (S_0, S_1) must be stable for a set-up time before the LOW-to-HIGH transition of the Clock Input CP).

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



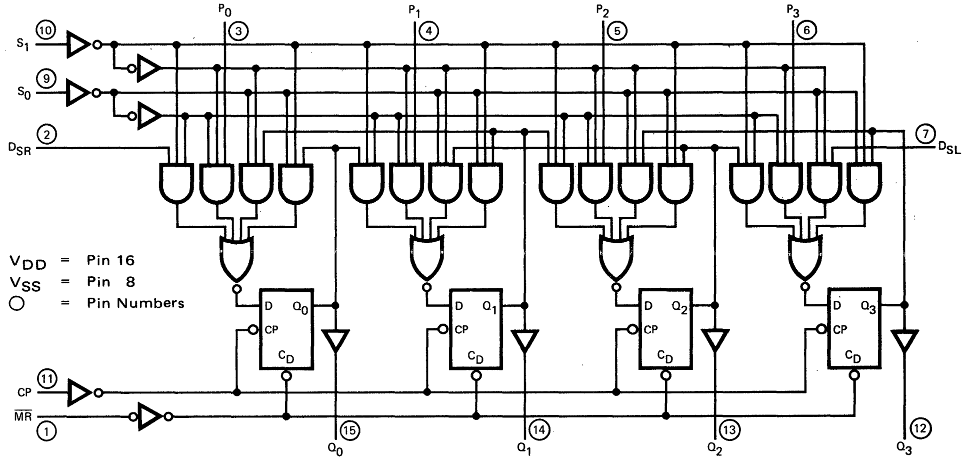
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

- TYPICAL SHIFT FREQUENCY OF 14 MHz AT V_{DD} = 10 V
- ASYNCHRONOUS MASTER RESET
- HOLD (DO NOTHING) MODE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- POSITIVE EDGE-TRIGGERED CLOCK

PIN NAMES

S_0, S_1	Mode Control Inputs
P_0-P_3	Parallel Data Inputs
D_{SR}	Serial (Shift Right) Data Input
D_{SL}	Serial (Shift Left) Data Input
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_3	Parallel Outputs

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{MR}$ = H)					OUTPUTS AT t_{n+1}			
	S_1	S_0	D_{SR}	D_{SL}	P_0,P_1,P_2,P_3	Q_0	Q_1	Q_2	Q_3
Hold	L	L	X	X	X	Q_0	Q_1	Q_2	Q_3
Shift Left	H	L	X	L	X	Q_1	Q_2	Q_3	L
	H	L	X	H	X	Q_1	Q_2	Q_3	H
Shift Right	L	H	L	X	X	L	Q_0	Q_1	Q_2
	L	H	H	X	X	H	Q_0	Q_1	Q_2
Parallel Load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(t_{n+1}) = Indicates state after next LOW-to-HIGH clock transition.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

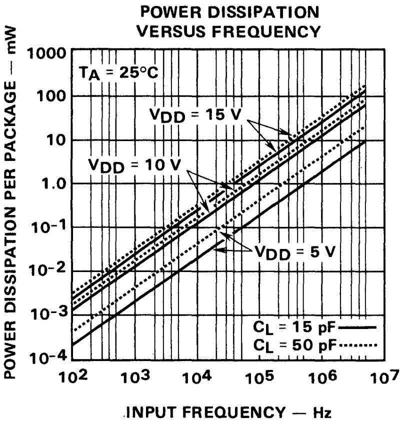
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

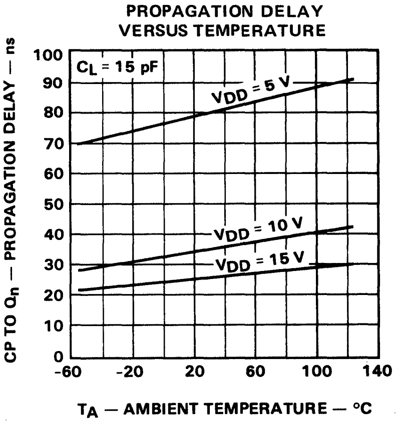
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

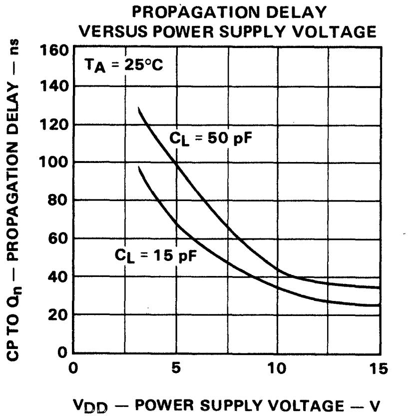
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q		100	180		45	80		35	64	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			100	180		45	80		35	64		
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		100	180		45	80		35	64	ns	
t_{THL}	Output Transition Time		75	135		40	70		25	45	ns	
t_{TLH}			75	135		40	70		25	45		
t_s	Set-Up Time, P_0-P_3, D_{SL}, D_{SR} to CP	80	40		40	20		32	15		ns	
t_h	Hold Time, P_0-P_3, D_{SL}, D_{SR} to CP	0	-10		0	-5		0	-5			
t_s	Set-Up Time, S to CP	100	60		50	30		40	20		ns	
t_h	Hold Time, S to CP	0	-10		0	-5		0	-5			
$t_W CP(L)$	Minimum Clock Pulse Width	100	60		60	35		48	25		ns	
$t_W \overline{MR}(L)$	Minimum $\overline{MR}$ Pulse Width	75	40		45	25		36	15		ns	
t_{rec}	Recovery Time for $\overline{MR}$	180	100		90	50		72	35		ns	
f_{MAX}	Maximum CP Frequency (Note 3)	4.5	9		9	14		10	16		MHz	

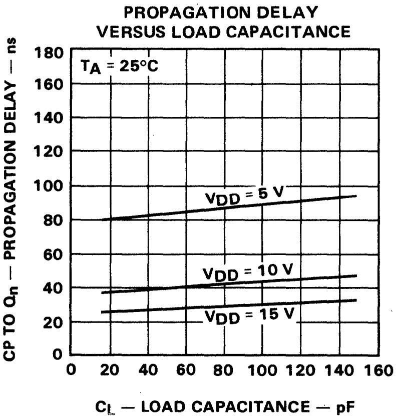
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

TYPICAL ELECTRICAL CHARACTERISTICS


POWER DISSIPATION VERSUS FREQUENCY

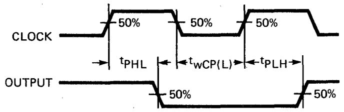

PROPAGATION DELAY VERSUS TEMPERATURE


PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE


PROPAGATION DELAY VERSUS LOAD CAPACITANCE

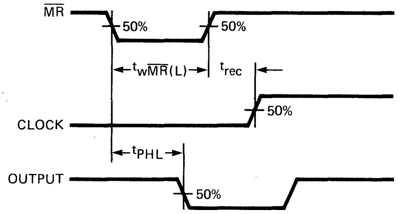
SWITCHING TIME WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



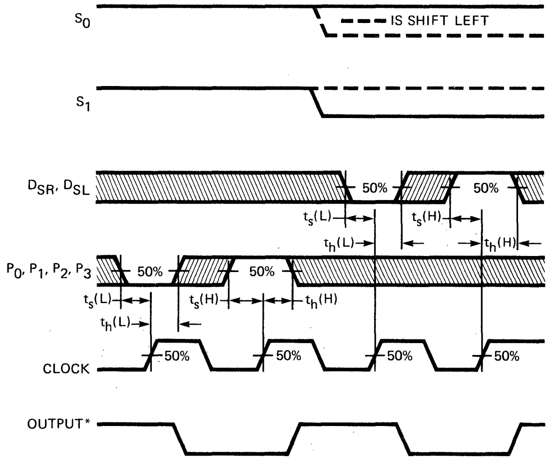
CLOCK TO OUTPUT DELAYS
CLOCK PULSE WIDTH

OTHER CONDITIONS: S_1 = L, $\overline{MR}$ = H, S_0 = H



MASTER RESET PULSE WIDTH,
MASTER RESET TO OUTPUT DELAY AND
MASTER RESET TO CLOCK RECOVERY TIME

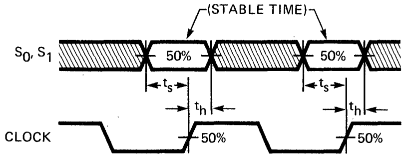
OTHER CONDITIONS: S_0, S_1 = H
$P_0 = P_1 = P_2 = P_3$ = H



SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (D_{SR}, D_{SL}) AND PARALLEL DATA (P_0, P_1, P_2, P_3)

OTHER CONDITIONS: $\overline{MR}$ = H

*D_{SR} Set-up Time Affects Q_0 Only
D_{SL} Set-up Time Affects Q_3 Only



SET-UP (t_s) AND HOLD (t_h) TIME FOR S INPUT

OTHER CONDITIONS: $\overline{MR}$ = H

40195B/74C195/54C195

4-BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION — The 40195B is a fully synchronous edge-triggered 4-Bit Shift Register with a Clock Input (CP), four synchronous Parallel Data Inputs (P_0-P_3), two synchronous Serial Data Inputs (J, $\overline{K}$), a synchronous Mode Control Input ($\overline{PE}$), Buffered Outputs from all four bit positions (Q_0-Q_3), a Buffered Inverted Output from the last bit position ($\overline{Q}_3$) and an overriding asynchronous Master Reset Input ($\overline{MR}$).

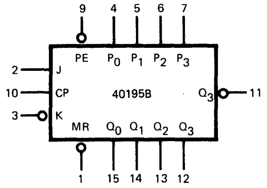
Operation is synchronous (except for Master Reset) and is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). When the Mode Control Input ($\overline{PE}$) is LOW, a LOW-to-HIGH clock transition loads data into the register from Parallel Data Inputs (P_0-P_3). When the Mode Control Input ($\overline{PE}$) is HIGH, a LOW-to-HIGH clock transition shifts data into the first register position from the Serial Data Inputs (J, $\overline{K}$), and shifts all the data in the register one position to the right. D-type entry is obtained by tying the two Serial Data Inputs (J, $\overline{K}$) together. A LOW on the Master Reset Input ($\overline{MR}$) resets all four bit positions (Q_0-Q_3 = LOW, $\overline{Q}_3$ = HIGH) independent of all other input conditions. The 40195B is a direct replacement for the 74C195/54C195.

- **TYPICAL SHIFT FREQUENCY OF 14 MHz AT V_{DD} = 10 V**
- **ASYNCHRONOUS MASTER RESET**
- **J, $\overline{K}$ INPUTS TO THE FIRST STAGE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **COMPLEMENTARY OUTPUT FROM THE LAST STAGE**
- **POSITIVE EDGE-TRIGGERED CLOCK**

PIN NAMES

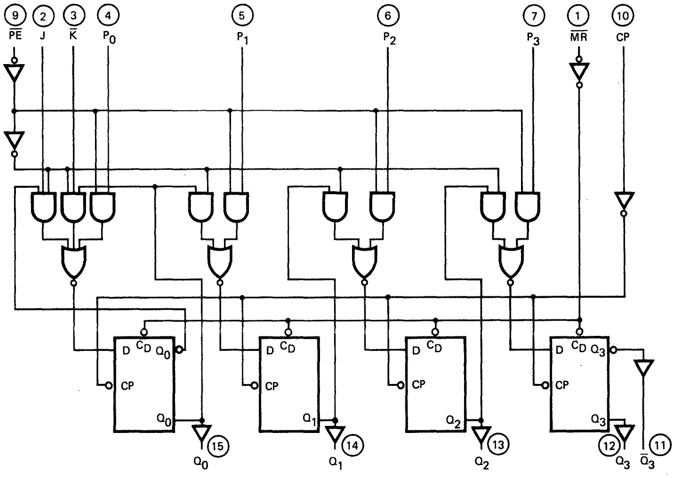
$\overline{PE}$	Parallel Enable Input (Active LOW)
P_0-P_3	Parallel Data Inputs
J	First Stage J Input (Active HIGH)
$\overline{K}$	First Stage K Input (Active LOW)
CP	Clock Input (L → H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_3	Parallel Outputs
$\overline{Q}_3$	Complementary Last Stage Output

LOGIC SYMBOL



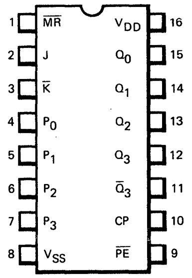
V_{DD} = Pin 16
V_{SS} = Pin 8

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{MR}$ = H)							OUTPUTS AT t_{n+1}				
	$\overline{PE}$	J	$\overline{K}$	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Shift Mode	H	L	L	X	X	X	X	L	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	L	H	X	X	X	X	Q_0	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	H	L	X	X	X	X	$\overline{Q}_0$	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	H	H	X	X	X	X	H	Q_0	Q_1	Q_2	$\overline{Q}_2$
Parallel Entry Mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(t_{n+1}) = Indicates state after next LOW to HIGH clock transition.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

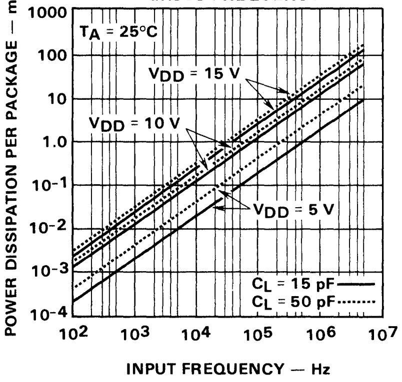
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

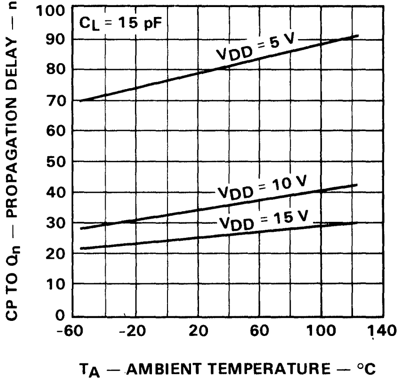
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n or $\overline{Q}_3$		100	180		45	80		35	64	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			100	180		45	80		35	64		
t_{PHL}	Propagation Delay, $\overline{MR}$ to $\overline{Q}_3$		100	180		45	80		35	64	ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		100	180		45	80		35	64	ns	
t_{THL}	Output Transition Time		75	135		40	70		25	45	ns	
t_{TLH}			75	135		40	70		25	45		
t_s	Set-Up Time, J, $\overline{K}$, P_0-P_3 to CP	80	40		40	20		32	15		ns	
t_h	Hold Time, J, $\overline{K}$, P_0-P_3 to CP	0	-10		0	-5		0	-5			
t_s	Set-Up Time, $\overline{PE}$ to CP	100	60		50	30		40	20		ns	
t_h	Hold Time, $\overline{PE}$ to CP	0	-10		0	-5		0	-5			
$t_wCP(L)$	Minimum Clock Pulse Width	100	60		60	35		48	25		ns	
$t_wMR(L)$	Minimum $\overline{MR}$ Pulse Width	75	40		45	25		36	15		ns	
t_{rec}	Recovery Time for $\overline{MR}$	180	100		90	50		72	35		ns	
f_{MAX}	Maximum CP Frequency (Note 3)	4.5	9		9	14		10	16		MHz	

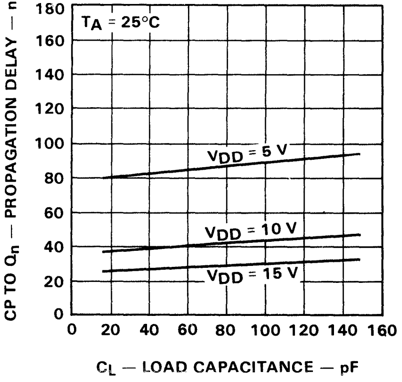
NOTES:

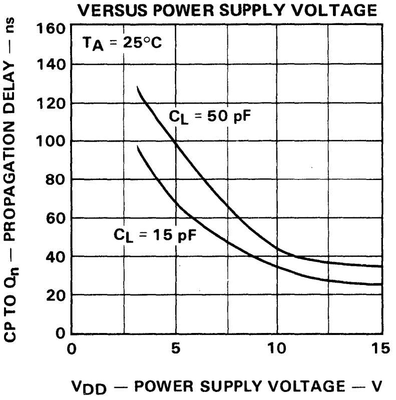
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 µs at V_{DD} = 5 V, 4 µs at V_{DD} = 10 V, and 3 µs at V_{DD} = 15 V.

TYPICAL ELECTRICAL CHARACTERISTICS


POWER DISSIPATION VERSUS FREQUENCY


PROPAGATION DELAY VERSUS TEMPERATURE

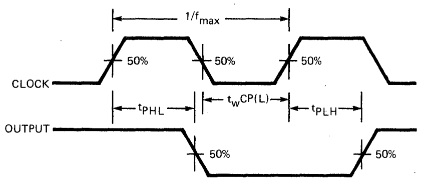

PROPAGATION DELAY VERSUS LOAD CAPACITANCE


PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE

SWITCHING TIME WAVEFORMS

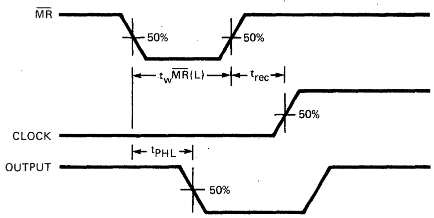
The shaded areas indicate when the input is permitted to change for predictable output performance.

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



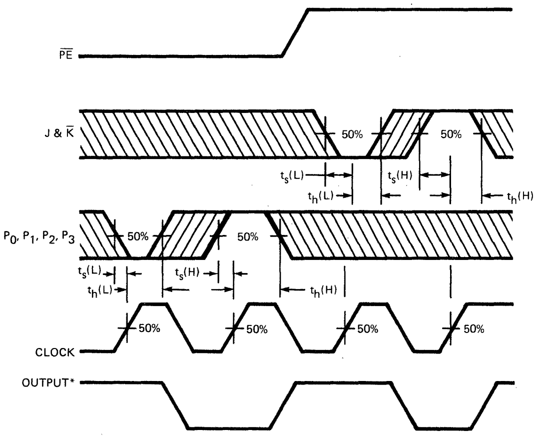
OTHER CONDITIONS: $J = \overline{PE} = \overline{MR}$ = HIGH
$\overline{K}$ = L & W

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



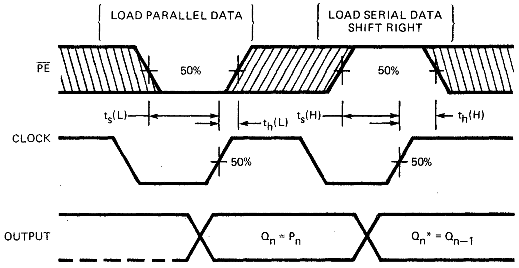
OTHER CONDITIONS: $\overline{PE}$ = LOW
$P_0 = P_1 = P_2 = P_3$ = HIGH

SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J & $\overline{K}$) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



OTHER CONDITIONS: $\overline{MR}$ = HIGH
*J & $\overline{K}$ Set-up Time Affects Q_0 Only

SET-UP (t_s) AND HOLD (t_h) TIME FOR $\overline{PE}$ INPUT



OTHER CONDITIONS: $\overline{MR}$ = HIGH
*Q_0 State will be Determined by J & $\overline{K}$ Inputs

NOTE:
Set-up Times (t_s) and Hold Times (t_h) are shown as positive values but may be specified as negative values.

6508B/6518B

1024-BIT (1024 X 1) CMOS
RANDOM ACCESS MEMORY WITH 3-STATE OUTPUT

DESCRIPTION – The 6508B/6518B are high-speed, low-power silicon-gate CMOS static RAMs organized as 1024 words by 1 bit. These RAMs are designed with all inputs and outputs TTL compatible. These devices operate off a single 5 V power supply with a worst case access time of 250 ns. Data retention is guaranteed at 2.0 V V_{CC} minimum. Output data has the same polarity as the input data. The addresses are latched by on-chip address registers. These registers are controlled by the high-to-low transition of chip select input $\overline{CS}$ ($\overline{CS_1}$ on F6518). Chip select input $\overline{CS}$ ($\overline{CS_1}$) and $\overline{WE}$ are designed such that common I/O operation can be implemented easily for maximum design flexibility. The 6518B has three chip select inputs for better access control. The 6508B has all the three chip select inputs tied together as a single $\overline{CS}$.

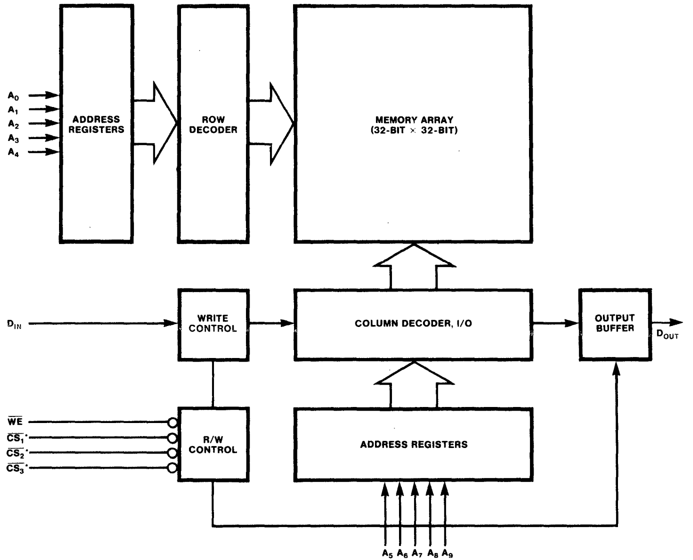
The device is ideally suited for memory systems requiring low-power, high-performance, and non-volatile (backup) operation.

- FAST ACCESS – 250 ns MAX
- LOW STANDBY POWER – 20 μA MAX
- DATA RETENTION TO V_{CC} = 2.0 V
- TTL COMPATIBLE I/O
- 3-STATE OUTPUT
- SINGLE 5 V SUPPLY
- ON-CHIP ADDRESS REGISTERS
- THREE CHIP-SELECT (6518B)

MODE OF OPERATION

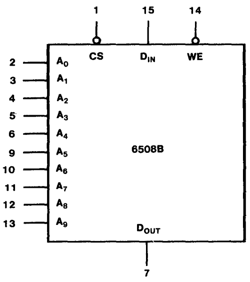
MODE	INPUTS				OUTPUTS
	$\overline{WE}$	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{CS_3}$	D_{OUT}
Standby	X	1	1	1	HIGH Z
Unselected	X	0	0	1	HIGH Z
	X	0	1	0	HIGH Z
	X	1	0	0	HIGH Z
Write	0	0	0	0	HIGH Z
Read	1	0	0	0	Data

BLOCK DIAGRAM

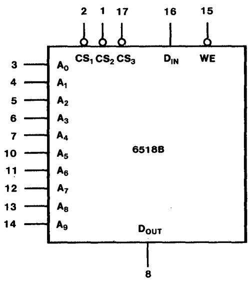


*$\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_3}$ on 6508B are all tied together to become $\overline{CS}$.

LOGIC SYMBOLS



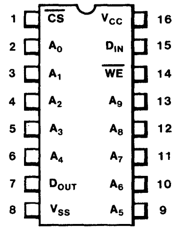
V_{CC} = Pin 16
V_{SS} = Pin 8



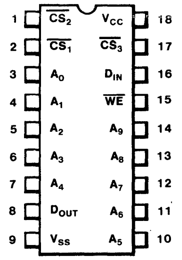
V_{CC} = Pin 18
V_{SS} = Pin 9

CONNECTION DIAGRAMS

6508B



6518B



ABSOLUTE MAXIMUM RATING

Supply Voltage V_{CC}	8 V
Input/Output Voltage Applied	V_{SS} −0.5 V to V_{CC} +0.5 V
Storage Temperature	−65°C to 150°C
Operating Temperature	−25°C to +85°C

AC CHARACTERISTICS: V_{CC} = 5 V ± 10%, T_A = −25°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
T_C	Cycle Time	350		ns	C_L = 50 pF (One TTL Load)
T_{ACC}	Access Time From CS		250	ns	
T_{AS}	Address Set-up Time	15		ns	
T_{AH}	Address Hold Time	50		ns	
T_{EO}	Output Enable Time		150	ns	
T_{DO}	Output Disable Time		150	ns	
T_{CSL}	$\overline{CS}$ LOW	200		ns	
T_{CSH}	$\overline{CS}$ HIGH	150		ns	
T_{WP}	Write Pulse Width	150		ns	
T_{DS}	Data Set-up Time	150		ns	
T_{DH}	Data Hold Time	10		ns	

DC CHARACTERISTICS: V_{CC} = 5 V ± 10%, T_A = −25°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	V_{CC} −2.0	V_{CC}	V	
V_{IL}	Logical "0" Input Voltage	0	0.8	V	
I_{IL}	Input Leakage	−1.0	+1.0	μA	0 V ⩾ V_{IN} ⩾ V_{CC}
V_{OH1}	Logical "1" Output Voltage	V_{CC} −0.01		V	I_{OUT} = 0
V_{OH2}	Logical "1" Output Voltage	V_{CC} −2.0		V	I_{OUT} = −0.2 mA
V_{OL1}	Logical "0" Output Voltage		V_{SS} + 0.01	V	I_{OUT} = 0
V_{OL2}	Logical "0" Output Voltage		V_{SS} + 0.4	V	I_{OUT} = 2.0 mA
I_O	Output Leakage	−1.0	+1.0	μA	0 V ⩾ V_{OUT} ⩾ V_{CC} $\overline{CS}$ = V_{IH}
I_{CC} STD	Supply Current (Standby)		20	μA	V_{IH} = V_{CC} or V_{SS}
I_{CC}	Supply Current (Operating)		2.0	mA	f = 1 MHz
VDR	V_{CC} for Data Retention	2.0		V	
C_{IN}	Input Capacitance		7	pF	
C_{OUT}	Output Capacitance		10	pF	

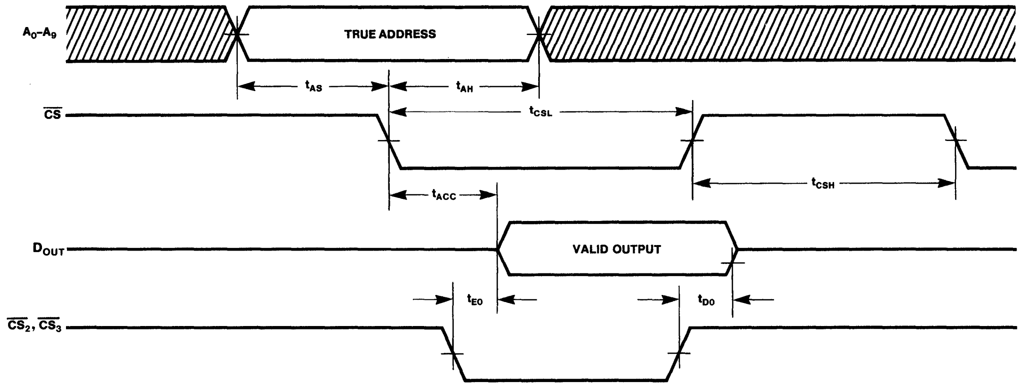
AC WAVEFORMS

Conditions: V_{CC} = 5 V ± 10%
C_L = 50 pF (One TTL Load)
T_A = −25°C to +85°C

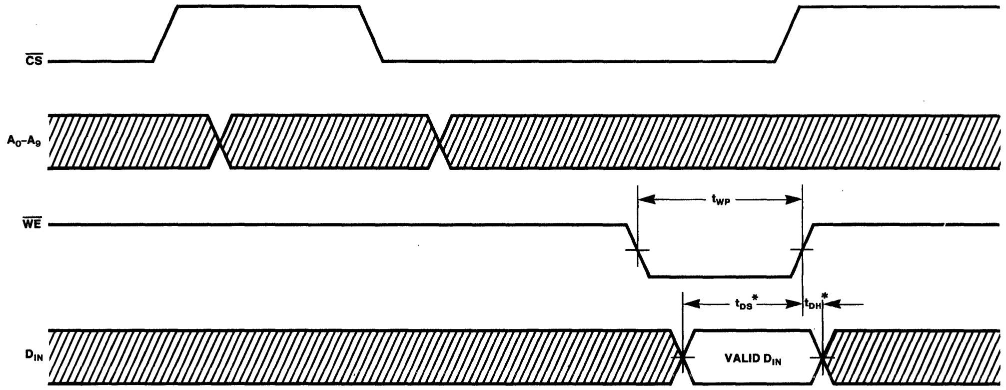
Input Level: LOW = V_{IL}
HIGH = V_{IH}
t_r, t_f = 20 ns

Measurement Reference to 1/2 V_{CC}

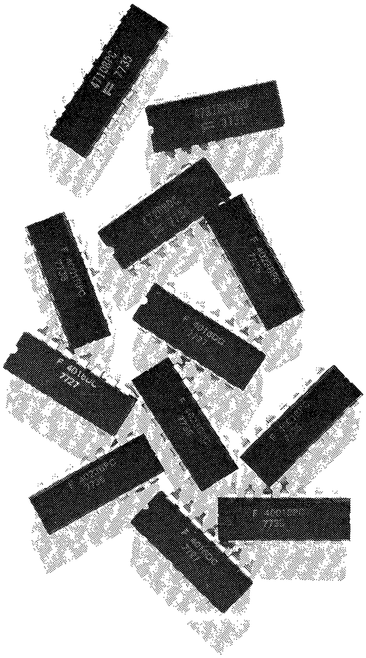
A. READ CYCLE



B. WRITE CYCLE



*D_{IN} input is reference to HIGH-to-LOW edge of $\overline{WE}$, $\overline{CS}$ ($\overline{CS_1}$), $\overline{CS_2}$, $\overline{CS_3}$, which ever switches first.



APPLICATIONS INFORMATION CONTENTS

INTERFACE CIRCUITS FOR CMOS

Fairchild manufactures one of the broadest varieties of Integrated Circuits in the world. In an effort to aid the designer in his search for compatible interface alternatives, listed below are a number of circuits manufactured by different divisions of Fairchild Semiconductor and easily compatible with the Fairchild line of Isoplanar CMOS.

Fairchild F54LSXX/74LSXX LOW POWER SCHOTTKY TTL
(Reference: Fairchild Low Power Schottky Data Book and Fairchild Low Power Schottky Designer's Guide)

When Multi-TTL drive capability is required, the CMOS 4049B and 4050B Hex Buffers can be used to drive two standard TTL Loads with typical delay of 45 ns (V_{DD} = 5 V). These devices, because of the deletion of the V_{DD} input diode, allow High Voltage CMOS to 5 Volt TTL translation. For higher performance and additional drive capability each of the following Fairchild Low Power Schottky devices may be used as interface/logic translating elements with capability of driving up to five standard TTL Loads. Although the Low Power Schottky devices must be operated from a 5 V TTL supply, they can accept input voltages up to 15 V, allowing direct interface with CMOS operated up to 15 V.

F54LS00/74LS00
F54LS02/74LS02
F54LS04/74LS04
F54LS08/74LS08
F54LS09/74LS09
F54LS10/74LS10
F54LS11/74LS11

F54LS13/74LS13
F54LS14/74LS14
F54LS15/74LS15
F54LS20/74LS20
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F54LS30/74LS30
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F54LS38/74LS38
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F54LS42/74LS42
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F54LS48/74LS48
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F54LS54/74LS54
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F54LS73/74LS73
F54LS75/74LS75
F54LS76/74LS76
F54LS77/74LS77
F54LS78/74LS78
F54LS83/74LS83A

F54LS85/74LS85
F54LS86/74LS86
F54LS89/74LS89
F54LS95/74LS95B
F54LS107/74LS107
F54LS125/74LS125
F54LS126/74LS126

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F54LS133/74LS133
F54LS136/74LS136
F54LS138/74LS138
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F54LS195/74LS195
F54LS196/74LS196*
F54LS197/74LS197*
F54LS240/74LS240
F54LS241/74LS241
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F54LS256/74LS256
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F54LS258/74LS258
F54LS259/74LS259
F54LS260/74LS260
F54LS266/74LS266
F54LS273/74LS273
F54LS279/74LS279
F54LS283/74LS283
F54LS289/74LS289
F54LS295/74LS295A
F54LS298/74LS298
F54LS299/74LS299
F54LS323/74LS323

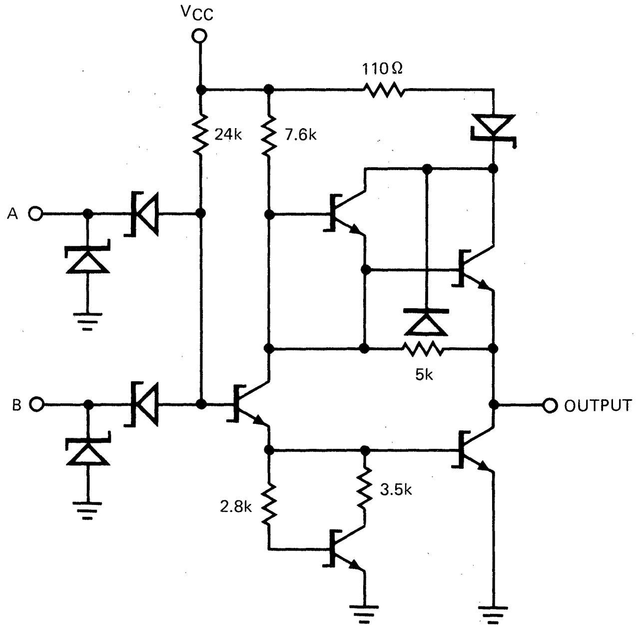
F54LS352/74LS352
F54LS353/74LS353
F54LS365/74LS365
F54LS366/74LS366
F54LS367/74LS367
F54LS368/74LS368
F54LS373/74LS373

F54LS374/74LS374
F54LS375/74LS375
F54LS377/74LS377
F54LS378/74LS378
F54LS379/74LS379
F54LS386/74LS386
F54LS395/74LS395
F54LS398/74LS398
F54LS399/74LS399
F54LS502/74LS502
F54LS540/74LS540
F54LS541/74LS541
F54LS568/74LS568
F54LS569/74LS569
F54LS573/74LS573
F54LS574/74LS574
F54LS670/74LS670

*Except For Clock Inputs.

Fairchild Low Power Schottky devices also incorporate a unique Schottky Diode in series with the collector of the output transistor. This diode allows the output to be pulled substantially higher than V_{CC}. Although the Low Power Schottky devices must be operated from a 5 V TTL supply, a simple external pullup resistor between the LS output and the CMOS V_{DD} power supply will allow direct interface between Low Power Schottky Logic (V_{CC} = 5 V) and high voltage CMOS logic, up to V_{DD} = 10V. With the exception of the F74LS00, F74LS02, F74LS04, F74LS10, F74LS11, F74LS20, and the F74LS32, each of the devices listed above will perform the low voltage to high voltage translation.

FAIRCHILD LOW POWER SCHOTTKY
2-Input NAND Gate



75491 • 75492

MOS TO LED SEGMENT AND DIGIT DRIVERS

(Reference: Fairchild Linear Integrated Circuits Data Book)

The 75491 and 75491A, LED Quad Segment Digit Drivers interface MOS signals to common cathode LED displays. High output current capability makes the devices ideal in time multiplex systems using segment address or digit scan method of driving LEDs to minimize the number of drivers required.

The 75492 and 75492A Hex LED/Lamp Drivers convert MOS signals to high output currents for LED display digit select or lamp select. The high output current capability makes the devices ideal in time multiplex systems using segment address or digit scan method of driving LEDs to minimize the number of drivers required.

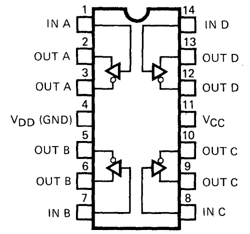
75491 • 75491A

- **50 mA SOURCE OR SINK CAPABILITY**
- **LOW INPUT CURRENTS FOR CMOS COMPATIBILITY**
- **LOW STANDBY POWER**
- **FOUR HIGH GAIN DARLINGTON CIRCUITS**
- **10 V and 20 V OPERATION**

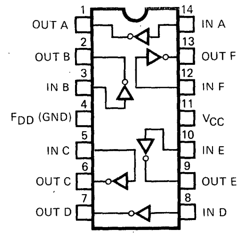
75492 • 75492A

- **250 mA SINK CAPABILITY**
- **CMOS COMPATIBLE INPUTS**
- **LOW STANDBY POWER**
- **SIX HIGH GAIN DARLINGTON CIRCUITS**
- **10 V AND 20 V OPERATION**

75491 • 75491A
CONNECTION DIAGRAM
(TOP VIEW)



75492 • 75492A
CONNECTION DIAGRAM
(TOP VIEW)



9665 • 9667 • 9668

HIGH VOLTAGE HIGH CURRENT DARLINGTON DRIVERS

(Reference: Fairchild 9665 • 9666 • 9667 • 9668 Data Sheet)

The 9665, 9667 and 9668 are comprised of seven high voltage, high current npn Darlington Transistor pairs. All units feature common emitter, open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads and appropriate emmiter-base resistors for leakage.

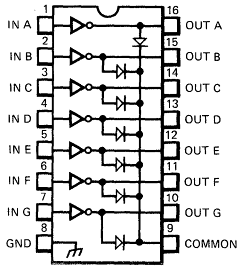
The 9665 is a general purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. Input current limiting is done by connecting an appropriate discrete resistor to each input.

The 9667 has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V.

The 9668 has an appropriate input resistor to allow direct operation from CMOS or PMOS outputs operating from supply voltages of 6 to 15 V.

- **SEVEN HIGH GAIN DARLINGTON TRANSISTOR PAIRS**
- **HIGH OUTPUT VOLTAGE (V_{CE} = 50 V)**
- **HIGH OUTPUT CURRENT (I_C ≑ 350 mA)**
- **CMOS COMPATIBLE INPUTS**
- **SUPPRESSION DIODES FOR INDUCTIVE LOADS**
- **2 WATT PLASTIC DIP PACKAGE ON COPPER PIN FRAME**

9665 • 9667 • 9668
CONNECTION DIAGRAM
(TOP VIEW)



96L02

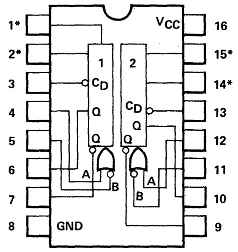
LOW POWER DUAL ONE-SHOT MULTIVIBRATOR

Retriggerable Resettable Monostable Multivibrator
(Reference: Fairchild Low Power TTL Book)

The 96L02 is pin and function compatible with the F4528 Dual Monostable and exhibits improved stability and speed. It is usable in 5 V CMOS systems.

- TYPICAL POWER DISSIPATION OF 25 mW/ONE SHOT
- 50 ns TYPICAL PROPAGATION DELAY
- RETRIGGERABLE 0 TO 100% DUTY CYCLE
- FAIRCHILD 4000B COMPATIBLE INPUTS
- OPTIONAL RETRIGGER LOCK-OUT CAPABILITY
- PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS
- RESETTABLE

96L02 LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



* Leads for external timing

μA775

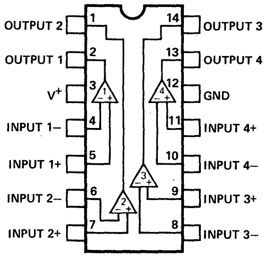
QUAD COMPARATOR VOLTAGE COMPARATOR

(Reference: Fairchild μA775 Data Sheet)

In a CMOS system it may be necessary to detect differences between two voltage levels and convert to logic levels. The μA775 Quad Comparator is capable of operating over the CMOS power supply range. These comparators have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage. Applications include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators and wide range V_{CO}.

- SINGLE SUPPLY OPERATION—+2.0 V TO +36 V
- COMPARES VOLTAGES NEAR GROUND POTENTIAL
- LOW CURRENT DRAIN—700 μA TYPICAL
- COMPATIBLE WITH ALL FORMS OF CMOS
- LOW INPUT BIAS CURRENT—25 nA TYPICAL
- LOW INPUT OFFSET CURRENT—25 nA
- LOW OFFSET VOLTAGE—5 mV MAX

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



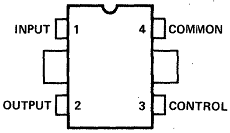
POWER SUPPLY REGULATOR

μA78MG 4-Terminal Regulator
(Reference: Fairchild μA78 MG • μA79 MG Data Sheet)

This single compact regulator with its 500 mA capability is sufficient for all but the very largest CMOS systems. The adjustable output voltage feature allows fine tuning of system speed power product.

- OUTPUT CURRENT IN EXCESS OF 0.5 A
- POSITIVE OUTPUT VOLTAGE 5 TO 30 V
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT PROTECTION
- OUTPUT SAFE AREA PROTECTION
- POWER MINI DUAL IN-LINE PACKAGE

μA78 MG CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: Heat sink tabs connected to common

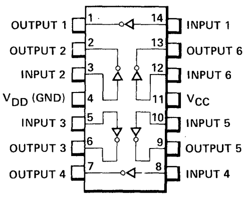
9664
MOS TO LED DIGIT DRIVER

(Reference: Fairchild 9664 Data Sheet)

This driver is ideal for driving high current devices such as LEDs, relays and lamps. High input impedance allows direct drive from Fairchild 4000B CMOS devices; however, there is some degradation in logic level at the CMOS output. The 9664 is specified to 10 V operation, the 9664A to 20 V.

- **150 mA SINK CAPABILITY**
- **CMOS COMPATIBLE INPUTS**
- **VERY LOW STANDBY POWER**
- **SIX HIGH GAIN DARLINGTON CIRCUITS**
- **10 AND 20 V OPERATION**

9664/9664A LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



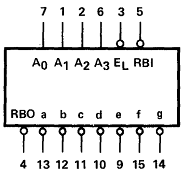
9374
DECODER/DRIVER/LATCH CMOS TO 7-SEGMENT LED DISPLAY

(Reference: Fairchild 9374 Data Sheet)

This bipolar device contains latches for storage, a 7-segment decoder and 15 mA constant current drivers. The 9374 must operate at 5 V; its inputs are also limited to 5 V.

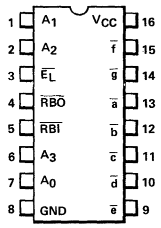
- **FAIRCHILD 4000B SERIES COMPATIBLE INPUTS**
- **HIGH SPEED INPUT LATCHES FOR DATA STORAGE**
- **15 mA CONSTANT CURRENT SINK CAPABILITY TO DIRECTLY DRIVE COMMON ANODE LED DISPLAYS**
- **INCREASES INCANDESCENT DISPLAY LIFE**
- **DATA INPUT LOADING ESSENTIALLY ZERO WHEN LATCH DISABLED**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZEROS**

9374
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

9374
CONNECTION DIAGRAM
DIP (TOP VIEW)



CMOS OSCILLATORS

This application note describes several square-wave oscillator circuits implemented with standard CMOS gates. In each case, appropriate timing equations, simplifying assumptions, and advantages and disadvantages are listed.

In general, because of the characteristically high input impedance of CMOS logic elements, more cost effective oscillators can be constructed offering relatively large timing constants without large capacitors. In addition, the CMOS oscillator offers:

- Very low power dissipation
- Operation over a wide power supply voltage range of 3 to 15 volts
- Operation over a frequency range of less than 1 Hz to over 23 MHz
- Easy interface to other logic families
- Relatively good stability with respect to variations in power supply voltage and operating temperature range

Generally, the use of buffered CMOS gates in oscillator applications is not recommended. Problems occur because of excessive gain through the buffered element (in excessive of 10^6) compounded by the slow edge rates, characteristic of the oscillator circuit. Ringing at the thresholds is very likely, creating false clocks in the system. This problem is, of course, overcome with the Schmitt Trigger and its associated hysteresis. Fairchild recommends the 4007UB, 4069UB, 40014B, 4093B and 4583B for all oscillator applications. For simplication, all applications in this note will be implemented using the 4069UB and 40014B.

Before describing any specific oscillator circuits and in an effort to clear some confusion and a few misconceptions, *Figure 1* illustrates the basic logical oscillator. Any odd number of inverting logic elements will oscillate naturally when connected in a ring as shown in *Figure 1*. This is easily seen by treating the inverters as ideal switches or inverters exhibiting finite propagation delays and ideal switching characteristics. The basic result is that a HIGH logic level chases itself around the ring. In this case the frequency of oscillation is dependent upon the total propagation delay through the ring and is given by:

$$f = \frac{1}{2nT_p} \quad \text{where:}$$

f = frequency of oscillation (Hz)
n = number of inverting gates in the ring
T_p = propagation delay per gate (seconds)

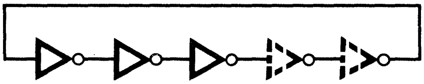
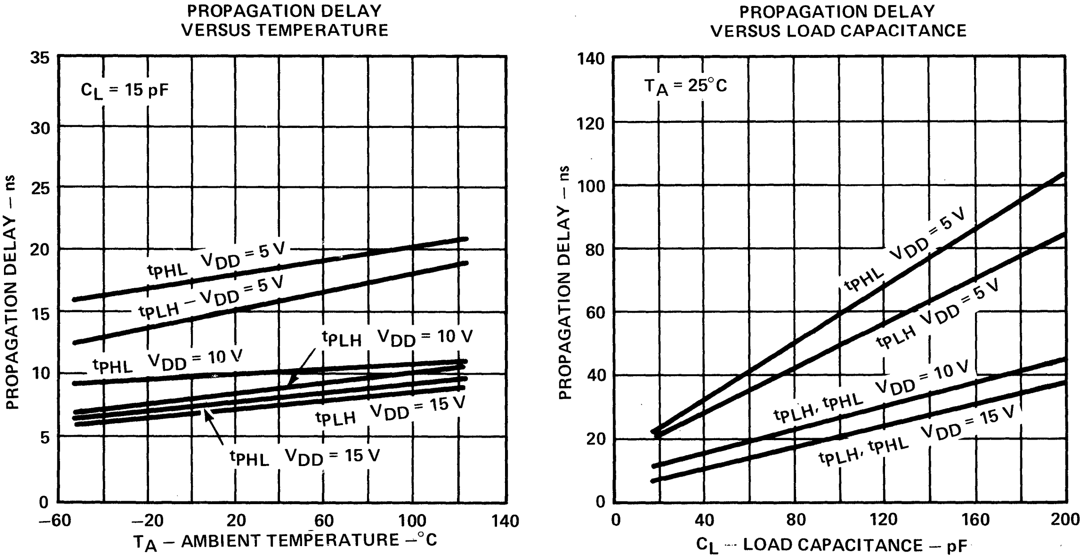


FIGURE 1. ANY ODD NUMBER OF INVERTING GATES WILL ALWAYS OSCILLATE

The practicality of such a circuit is limited by the fact that the frequency of oscillation is dependent upon T_p and therefore limited to a few specific values determined by T_p. Furthermore, stability of such a circuit is heavily dependent upon T_p's variation with temperature, power supply voltage and output loading. *Figure 2* illustrates expected variations in propagation delay for the 4069UB.


PROPAGATION DELAY VERSUS TEMPERATURE

PROPAGATION DELAY VERSUS LOAD CAPACITANCE

FIGURE 2. PROPAGATION DELAY VERSUS TEMPERATURE, LOAD CAPACITANCE AND POWER SUPPLY VOLTAGE FOR THE 4069UB

The Logical RC Oscillator

To overcome the disadvantages of the logical oscillator it is necessary to add other circuit elements that increase loop delay and thus reduce the effect of T_p variation on frequency. This increase in loop delay necessarily reduces the upper frequency limit for a given configuration, but lends the more important advantages of frequency predictability and stability.

Figure 3 illustrates a useful three gate oscillator incorporating a resistor capacitor network which does, in effect, slow the natural frequency of the ring oscillator and, assuming that the RC time constant is large enough, minimizes any effects of propagation delay and thus any dependence upon temperature, load capacitance, or operating voltage. With this in mind, it is assumed, hereafter in the analysis, that the logic elements are ideal, exhibiting negligible propagation delay. If very high oscillation frequencies are required, this assumption may not be valid.

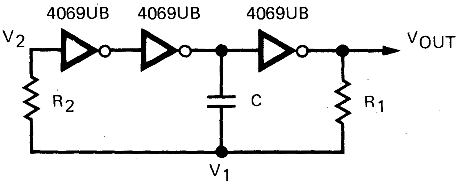


FIGURE 3. A THREE GATE RC OSCILLATOR

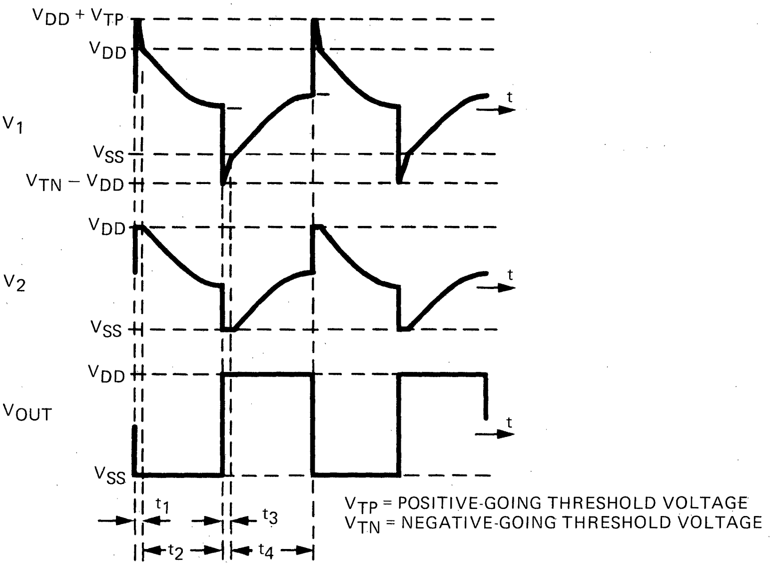


FIGURE 4. VOLTAGE WAVEFORMS FOR THE RC OSCILLATOR

As a means of determining a timing equation, *Figure 4* illustrates the voltage waveforms at specific points in the oscillator circuit. As shown, the voltage waveform at V_1 does, for short intervals of time, extend outside the power supply rails. These excursions are clipped at V_2 by the standard input protection diodes found on all Fairchild CMOS logic inputs *(Figure 5)*. At this point another simplifying assumption is made; input protection diodes D_1 and D_2 exhibit ideal characteristics. Since this assumption tends to have little overall effect on the voltage waveforms, the error is acceptably small.

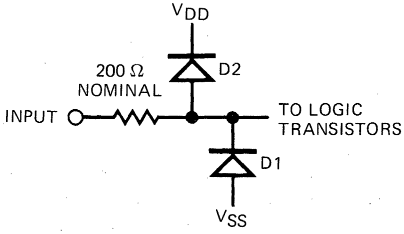


FIGURE 5. INPUT PROTECTION CIRCUIT

From *Figure 4*, the time period T for one cycle is:

$$T = t_1 + t_2 + t_3 + t_4$$

Once again, input protection diodes conduct only during t_1 and t_3. Similarly, except for input leakage current, Resistor R_2 conducts only during t_1 and t_3. Since input impedance is generally very large ($> 10^6\Omega$) compared to typical values for R_1 and R_2, input leakage currents are negligible and it is assumed they can be ignored. For resistor values greater than a few megohms, this may not be valid (note 1).

From basic electronics, the timing equation for exponential decay of an RC network *(Figure 6)* is.

$$t = -RC \ln (v/V_O)$$

$$\text{Thus: } t_1 \approx -R_1C \left[\frac{R_2}{R_1 + R_2}\right]\left[\ln \left(\frac{V_{DD}}{V_{DD} + V_{TP}}\right)\right]$$

$$t_2 \approx -R_1C \ln \left(\frac{V_{TN}}{V_{DD}}\right)$$

$$t_3 \approx -R_1C \left[\frac{R_2}{R_1 + R_2}\right]\left[\ln \left(\frac{V_{DD}}{2V_{DD} - V_{TN}}\right)\right]$$

$$t_4 \approx -R_1C \ln \left(\frac{V_{TP}}{V_{DD}}\right)$$

$$\text{and: } T \approx -R_1C \left\{\left[\frac{R_2}{R_1 + R_2}\right] \left[\ln \left(\frac{V_{DD}}{V_{DD} + V_{TP}}\right) + \ln \left(\frac{V_{DD}}{2V_{DD} - V_{TN}}\right)\right] + \ln \left(\frac{V_{TN}}{V_{DD}}\right) + \ln \left(\frac{V_{TP}}{V_{DD}}\right)\right\}$$

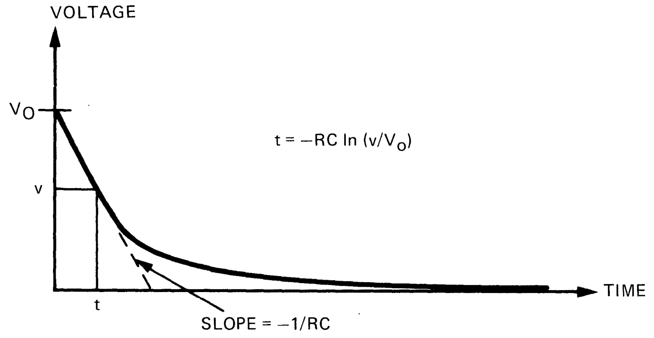


FIGURE 6. TIMING FOR THE EXPONENTIAL DECAY OF AN RC NETWORK

For those who prefer their timing equations not to be cluttered with details, several simplifying assumptions can be made. First, it is assumed that negative and positive threshold voltages are equal ($V_{TN} = V_{TP}$). This is a fairly safe assumption since standard gates will generally exhibit very little hysteresis (< 200 mV). Of course, this assumption is not valid for Schmitt Triggers.

The timing equation simplifies to:

$$T \approx -R_1C \left\{\left[\frac{R_2}{R_1 + R_2}\right] \left[\ln \left(\frac{V_{DD}}{V_{DD} + V_T}\right) + \ln \left(\frac{V_{DD}}{2V_{DD} - V_T}\right)\right] + 2 \ln \left(\frac{V_T}{V_{DD}}\right)\right\}$$

Next, it is assumed that CMOS is the ideal logic family with ideal transfer characteristics and thus, $V_T = V_{DD}/2$. As will be shown later, this can be a very misleading assumption. Nevertheless:

$$T \approx 2R_1C\left[\frac{0.405\ R_2}{R_1 + R_2} + 0.693\right]$$

and:

$$f \approx \frac{1}{2R_1C\left[\dfrac{0.405\ R_2}{R_1 + R_2} + 0.693\right]}$$

Furthermore:

If $R_1 = R_2$, $f \approx 0.559/R_1C$
If $R_1 >> R_2$, $f \approx 0.722/R_1C$
If $R_1 << R_2$, $f \approx 0.455/R_1C$

The last assumption is a very attractive one, greatly simplifying the timing equations, but can create correlation problems between paper calculations and actual results. CMOS is not, generally, an ideal logic family exhibiting ideal transfer characteristics and, in fact, guaranteed threshold limits allow variations in the timing equation constants which are much greater than those created by variations in R_2/R_1 as implied above.

Standard guarantees for CMOS circuits allow the actual switching threshold to lie in range from roughly 30% of V_{DD} to 70% of V_{DD} ($V_{IH} = 0.7\ V_{DD}$ and $V_{IL} = 0.3\ V_{DD}$). If, in fact, actual thresholds are not near 0.5 V_{DD} the above simplifications can be grossly invalid. As a means of illustration, simplified timing equations have been generated assuming that $V_T = 0.7\ V_{DD}$ and $V_T = 0.3\ V_{DD}$. The results are shown in *Figure 7*. Also shown are the results of actual tests performed on the 4069UB with manufacturing date codes from over three years of production. Actual data implies that more accurate timing equations for the 4069UB would be:

$$\left.\begin{array}{ll} \text{For } R_1 = R_2, & f \approx 0.482/R_1C \\ \text{For } R_1 = 10\ R_2, & f \approx 0.580/R_1C \\ \text{For } 10\ R_1 = R_2, & f \approx 0.368/R_1C \end{array}\right\} \text{ With expected error} = \pm 5\%$$

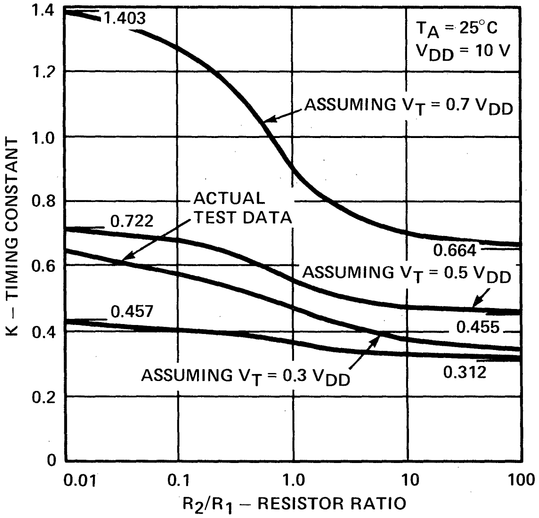


FIGURE 7. TIMING CONSTANT VERSUS RESISTOR RATIO FOR THE RC OSCILLATOR ASSUMING VARIOUS THRESHOLD VOLTAGES

Furthermore, it should be noted that the duty cycle of V_{OUT} will depend directly upon the actual threshold voltage. When $V_T = 0.5\ V_{DD}$, a 50% duty cycle results.

In summary, for better comparison between software and hardware, it may be necessary for the designer to more accurately determine actual threshold voltages.

The Two Gate Oscillator

A popular two gate RC Oscillator circuit is shown in *Figure 8*. Coincidentally, all of the RC oscillator timing equations, RC waveforms, assumptions and arguments thus far also apply to the circuit in *Figure 8*. The only real problem with this circuit is that it may not oscillate for certain values of capacitance. Unlike the logical oscillator circuit of *Figure 1* which oscillates naturally and the frequency of oscillation is only slowed and stabilized by an RC network, the two gate circuit is forced to oscillate by the RC network. To illustrate this point, allow C to go to zero. The result is a circuit as shown in *Figure 9* which obviously will not oscillate in an acceptible manner. However, gate count may be a critical factor in a design and the two gate oscillator circuit is often employed.

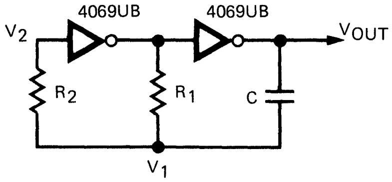


FIGURE 8. A TWO GATE RC OSCILLATOR

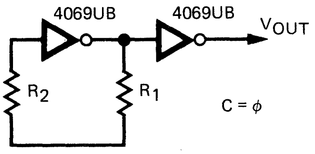


FIGURE 9. A TWO GATE RC OSCILLATOR MAY NOT OSCILLATE FOR SOME VALUES OF CAPACITANCE

The Schmitt Trigger Oscillator

Where gate count is a critical factor, *Figure 10* shows an Oscillator constructed from a single Inverting Schmitt Trigger. This circuit consumes only 1/6 of a package allowing the other five inverters to be utilized elsewhere in the system. It should be noted that the single stage oscillator is only practical where substantial hysteresis is provided by the logic element (i.e., Schmitt Triggers). It should, also, be noted that switching thresholds of the Schmitt Trigger are not as insensitive to variations in the power supply voltage. This circuit is best in those applications with relaxed requirements on frequency stability or where power supply voltages are well regulated.

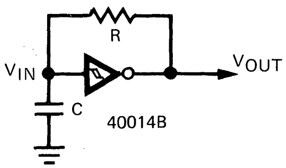


FIGURE 10. A SIMPLE SCHMITT TRIGGER OSCILLATOR

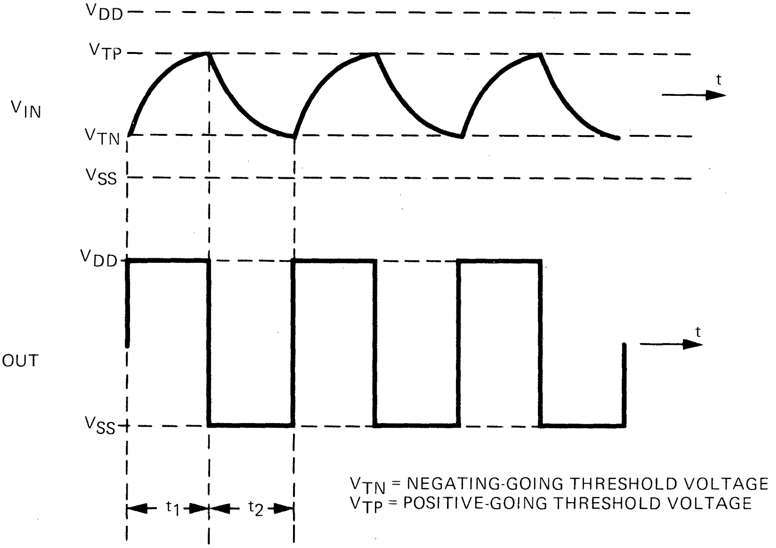


FIGURE 11. VOLTAGE WAVEFORMS FOR THE SINGLE SCHMITT TRIGGER OSCILLATOR

Figure 11 illustrates the voltage waveforms on the input and output pins of the Schmitt Trigger. Assuming that $t_1 + t_2 >> t_{PLH} + t_{PHL}$ the time period T for one cycle is:

$$T \approx t_1 + t_2$$

Where: $t_1 \approx -RC \ln \left(\frac{V_{DD} - V_{TP}}{V_{DD} - V_{TN}} \right)$

$$t_2 \approx -RC \ln \left(\frac{V_{TN}}{V_{TP}} \right)$$

or: $T \approx -RC \left[\ln \left(\frac{V_{TN}}{V_{TP}} \right) + \ln \left(\frac{V_{DD} - V_{TP}}{V_{DD} - V_{TN}} \right) \right]$

or: $T \approx RC \left[\ln \left(\frac{V_{TP}}{V_{TN}} \right) + \ln \left(\frac{V_{DD} - V_{TN}}{V_{DD} - V_{TP}} \right) \right]$

To simplify the equation, we can assume from the 40014B data sheet that at $V_{DD} = 10$ V, $V_{TN} = 6.8$ V and $V_{TP} = 3.2$ V, typically.

Thus: $T \approx 1.5\ RC$

or: $f \approx 0.667/RC$

Once again, from *Figure 12*, it can be determined that the simplification above may not be valid because of possible variations in actual thresholds within the guaranteed worst case limits versus the typical thresholds assumed above.

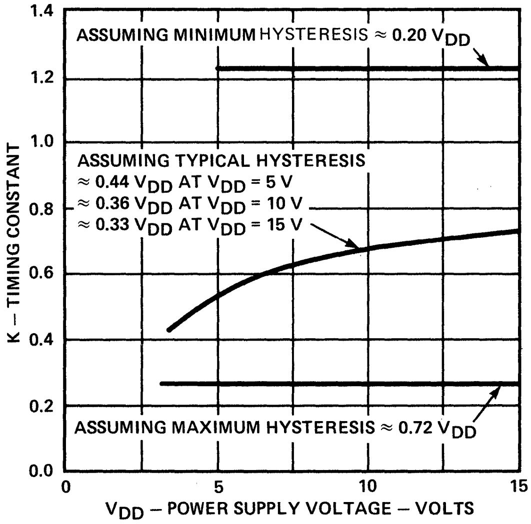


FIGURE 12. TIMING CONSTANT VERSUS POWER SUPPLY VOLTAGE ASSUMING VARIOUS HYSTERESIS LEVELS FOR THE 40014B

Based on actual test data performed on 40014B devices with a variety of manufacturing date codes, the following equation was determined:

$f \approx 0.631/RC$ For $R = 1\ K\Omega$ to $1\ M\Omega$
and: $C = 10\ \mu F$ to 100 pF

with expected error ≈ ±10%

The Gated Oscillator

Often the designer will have a need to enable or disable the free running oscillator at will. This is easily accomplished by adding a diode to the RC Oscillator circuit as shown in *Figure 13*. In one direction the diode provides an active HIGH Enable input and in the other an active LOW Enable input. With proper selection of the RC components, power dissipation in the disabled state can be minimized.

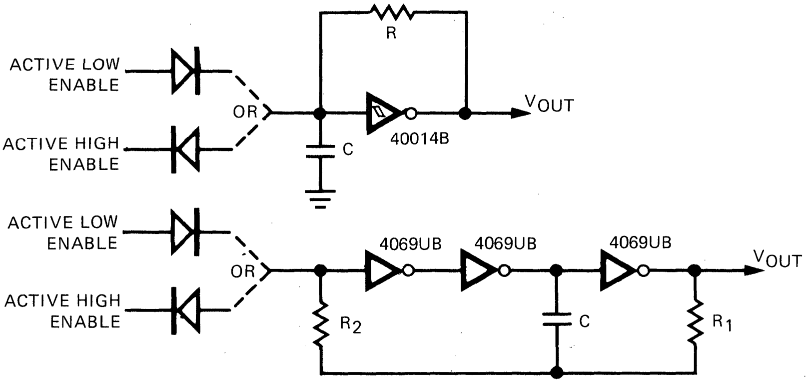


FIGURE 13. GATED OSCILLATORS

A CMOS Crystal Oscillator

For those applications requiring extreme stability of the oscillation frequency, a CMOS Crystal Oscillator circuit is shown in *Figure 14*. Actual resistor and capacitor component values are determined by the desired output frequency and characteristics of the crystal employed. Any odd number of inverting gates may be used in the circuit. However, maximum operating frequency will be limited by total propagation delay through the oscillator ring.

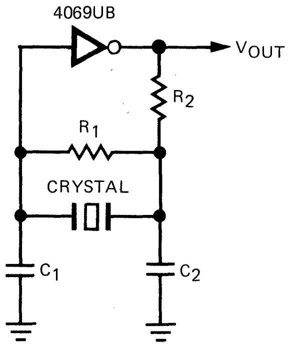


FIGURE 14. A CMOS CRYSTAL OSCILLATOR

Finally, in applications demanding such stringent stability, it is not uncommon for the designer, for reasons of both accuracy and cost, to select highest possible operating frequency. The result is an often critical tradeoff between tolerable power dissipation and acceptable accuracy. For the circuit of *Figure 14*, as operating frequency is increased by a factor of ten, power dissipation will also approximately increase by a factor of ten. Only the designer can acceptably resolve this tradeoff.

Summary

Simple CMOS inverting gates provide an attractive solution to oscillator applications providing better stability (especially at low frequency), very low power dissipation, wide operating power supply voltage range and relatively easy interface to other logic families.

This note has offered several alternative designs for CMOS oscillators each with its own advantages, disadvantages and simplifying assumptions. From the information presented herein, the designer has the capability of selecting the circuit and the characteristic tradeoffs best suited to his specific application.

Note 1. As a general rule, assuming worst case data sheet limits, input leakage current will have approximately a 10% affect upon the timing equation when $R_1 = 1.5\ M\Omega$ at $V_{DD} = 15\ V$, $10\ M\Omega$ at $V_{DD} = 10V$ and $5\ M\Omega$ at $V_{DD} = 5\ V$.

APPLICATION OF THE 4702B, PROGRAMMABLE BIT-RATE GENERATOR

The industry standard Universal Asynchronous Receiver/Transmitter (UART), an MOS/LSI subsystem, has had a considerable impact on data-communication system design. Not only has the UART dramatically reduced chip counts and increased reliability, etc., but it has also provided an incentive to integrate the remaining support functions.

One such subsystem is the 4702B programmable bit-rate generator, designed to provide the necessary clocking signals to operate asynchronous transmitter and receiver circuits. Several standardized signaling rates are used for start-stop communication depending on the transmission medium and other system requirements. The equipment must be capable of generating all the necessary frequencies and provide a way to select the desired one. In the past, this required several SSI/MSI circuits. Now, the 4702B can perform the task more easily and economically.

The 4702B provides any one of the 13 common bit rates on a selectable basis using an on-board oscillator and an external crystal; it also is expandable for multichannel applications. In its most general form, multichannel clocking requires that any of the possible frequencies must be available on any channel. Expansion up to eight channels is accomplished without device duplication. In multiple-device systems, there is no need to use a crystal with every device. *Figure 1* shows the block diagram of the 4702B which consists of the following major parts:

- Oscillator and associated gating
- Scan counter
- Count chains
- Initialization circuit
- Multiplexer and output storage

Oscillator and Associated Gating

The oscillator circuit together with an external crystal generates the master timing. A 2.4576 MHz crystal provides 16 times the frequency of the baud values marked; for example, 9600 baud corresponds to 153.6 kHz. If the External Clock Enable ($\overline{E}_{CP}$) is HIGH, the oscillator output signal drives the count chain. On the other hand, if it is LOW, the External Clock (CP) signal is enabled and is then the timing source. The External Clock input also participates in the device initialization scheme. The master timing signal, either from the external source or the local oscillator, is available on the Clock Output pin (CO). This signal can be used to drive other 4702B's in a multiple device system, thus eliminating the need to provide more than one crystal.

Scan Counter

The master timing drives a 3-bit binary scan counter which, in turn, drives the remaining counter chains on the chip. The scan counter allows expansion to eight channels as described later. The prescaling feature of this counter provides another benefit, i.e., it moves the input frequency to 2.4576 MHz which is ideal for low-cost crystals. If it were not for the scan counter, the 4702B would require a more expensive crystal of about 300 kHz.

Count Chains

The scan counter output drives an 8-bit binary counter which provides the frequencies corresponding to 9600, 4800, 2400, 1200, 600, 300, 150 and 75 baud. The 1800-baud signal is generated by dividing 9600 by 16/3. The 110 and 134.5 baud signals are approximated by dividing 2400 by 22 and 18 respectively. Dividing 1200 by 6 gives the 200 baud signal, while 50 baud is generated by dividing 200 baud by 4. All division factors except 16/3 are even; thus, all outputs except 1800 baud have a 50% duty cycle.

The actual division by 16/3 is achieved by using a sequence of integers 5 and 6 such that cumulative error after every three cycles is zero. This scheme, in conjunction with the divide by 16 performed in the UART, achieves good timing accuracy demanded by high speed communication equipment. Calculations indicate that the maximum distortion introduced does not exceed 0.78% regardless of the number of elements in a character.

Initialization Circuit

This circuit generates a Master Reset signal to initialize the flip-flops on the 4702B to a known state. If the External Clock Enable ($\overline{E_{CP}}$) is LOW, the local oscillator output is inhibited and timing is derived from the External Clock (CP). The first positive half cycle of the External Clock is used to generate the Master Reset and all succeeding clock signals are used for timing. This initialization scheme allows software-controlled diagnosis for fault isolation.

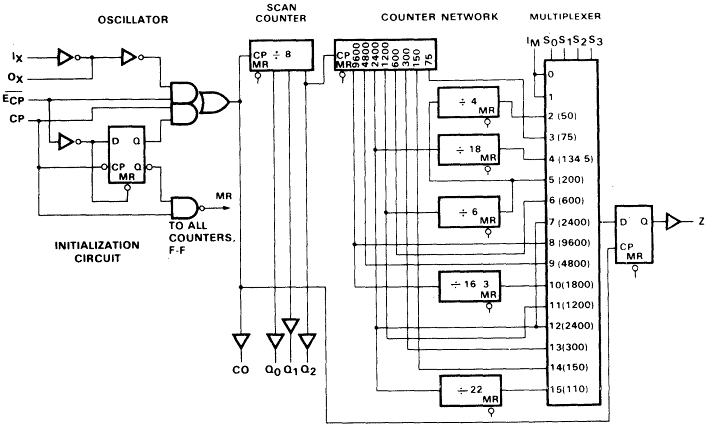


Fig. 1. 4702B Block Diagram

Multiplexer and Output Storage

All the desired outputs from the count chains are fed as data inputs to a multiplexer. The select inputs for this multiplexer are brought out as Rate Select input ($S_0 - S_3$). *Table 1* shows the correspondence between this code and the resulting frequency. The multiplexer output is fed as data input to a resynchronizing flip-flop that is clocked by the leading edge of the master timing.

If only single-channel applications of the 4702B were considered, the output flip-flop would be unnecessary. In multichannel applications, however, the Rate Select inputs change as a function of the Scan Counter output ($Q_0 - Q_2$). The resynchronizing flip-flop assures a fixed timing relationship between $Q_0 - Q_2$ and the Bit Rate output (Z).

Three important features should be noted from *Table 1.* First, two of the select codes specify Multiplexed Input (I_M) signal as the data source to the multiplexer. The user can feed a signal into this input, however, the primary intent was to feed a static logic level to achieve a "zero baud" situation. Secondly, the codes corresponding to 110, 150, 300, 1200 and 2400 baud each have a maximum of only one LOW level. These are the most commonly used rates in contemporary data terminals. Thus the rate select mechanism on these terminals need only be a single-pole 5-position switch with the common terminal grounded. Thirdly, 2400 baud is select by two different codes so that the whole spectrum of modern communication rates will have a HIGH code in the most significant bit position.

Typical Applications

In those applications where the Rate Select inputs are static levels, operation of the 4702B is rather straightforward. The multiplexer connects the specified counter output to the data input of the output flip-flop. Because the flip-flop is clocked by the master timing, its output reflects the selected frequency.

Single-Channel Bit-Rate Generator

Figure 2 shows the simplest of all 4702B applications. This circuit provides one of five possible bit rates as determined by the setting of the 5-position switch. The generated frequencies correspond to 110, 150, 300, 1200, and 2400 baud depending on the switch setting. For many low cost terminal applications, these five selectable bit rates are adequate. The 4702B is not only intended for single-channel but also for multichannel operation, as illustrated in the following applications.

S_3	S_2	S_1	S_0	OUTPUT RATE (Z)
L	L	L	L	MULTIPLEXED INPUT (I_M)
L	L	L	H	MULTIPLEXED INPUT (I_M)
L	L	H	L	50 BAUD
L	L	H	H	75 BAUD
L	H	L	L	134.5 BAUD
L	H	L	H	200 BAUD
L	H	H	L	600 BAUD
L	H	H	H	2400 BAUD
H	L	L	L	9600 BAUD
H	L	L	H	4800 BAUD
H	L	H	L	1800 BAUD
H	L	H	H	1200 BAUD
H	H	L	L	2400 BAUD
H	H	L	H	300 BAUD
H	H	H	L	150 BAUD
H	H	H	H	110 BAUD

Table 1. Truth Table for Rate Select Inputs

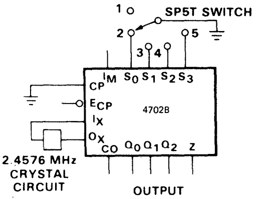


Fig. 2. Switch Selectable Bit-Rate Generator Configuration Providing 5 Bit Rates

Multichannel Bit-Rate Generation

Figure 3 illustrates a fully programmable 8-channel bit-rate generator system. Two 4 x 4 register file devices (9LS170) can be loaded with information (rate select codes from *Table 1)* relating to the desired frequency on a per-channel basis. For clarity, circuits for writing into the files are not shown.

The least significant Scan Counter outputs (Q_0, Q_1) control the Read Address of the 9LS170s while the most significant output (Q_2) controls the Read Enable (RE) inputs. Thus, as the counter advances, file locations are read out sequentially. The Scan Counter outputs are also the Address inputs for the 93L34 addressable latch. The Bit Rate output (Z) of the 4702B is the Data input to the 93L34 while the Clock Output is the Enable input.

To understand the operation, consider the instant when the Scan Counter outputs become Zero (Q_0 – Q_2 = LOW). The same clock that incremented this counter to Zero also clocked the counter output, corresponding to the selected frequency for channel 7 into the output flip-flop, and disabled the 93L34 latch via the Clock Output (CO), thus preventing any change in the latch outputs while the Scan Counter outputs and the Bit Rate output (Z) are changing.

During the second half of the clock cycle, when the Clock Output (CO) is LOW, the counter output representing the selected frequency for channel 7 is loaded into the 93L34 latch and is locked up on the Q_0 output.

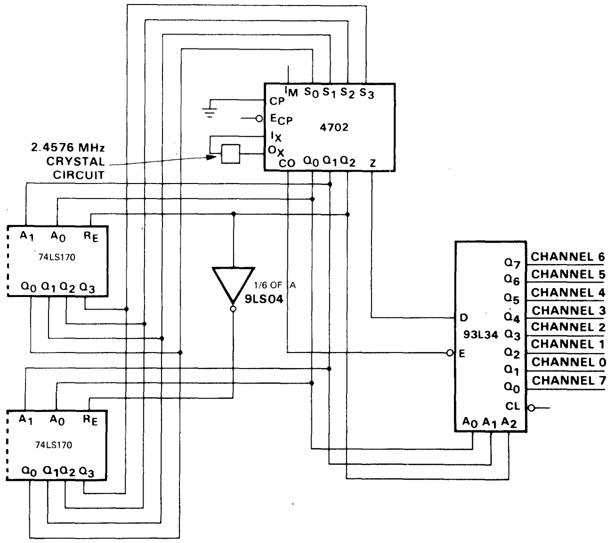


Fig. 3. A Fully Programmable 8-Channel Bit-Rate Generator System

The Scan Counter outputs ($Q_0 - Q_2$), which represent the selected channel, are used to interrogate the register file to determine the assigned bit rate for channel 0. The stored code for channel 0 is routed to the Rate Select inputs ($S_0 - S_3$) to select the appropriate internal frequency, so that during the next LOW-to-HIGH clock transition, the state of this internal signal is clocked into the output flip-flop. Thus, each channel is sequentially interrogated and the 93L34 latch is updated at least once during each half cycle of the highest output frequency (9600 baud).

By connecting the Scan Counter output Q_2 to the Multiplexed input (I_M) a similar technique can be used to implement a system with a maximum output frequency of 19,200 baud, however, the number of channels must be limited to four. This ensures that the output will be interrogated and updated at least once during each half cycle of the highest output frequency (19,200 baud).

Jumper Programmable 8-Channel Bit-Rate Generator

In systems where channel-speed assignments remain relatively fixed, software-controlled channel assignment is not necessary or practical. It may be simpler to program with "jumpers" at appropriate places in the system. See *Figure 4.*

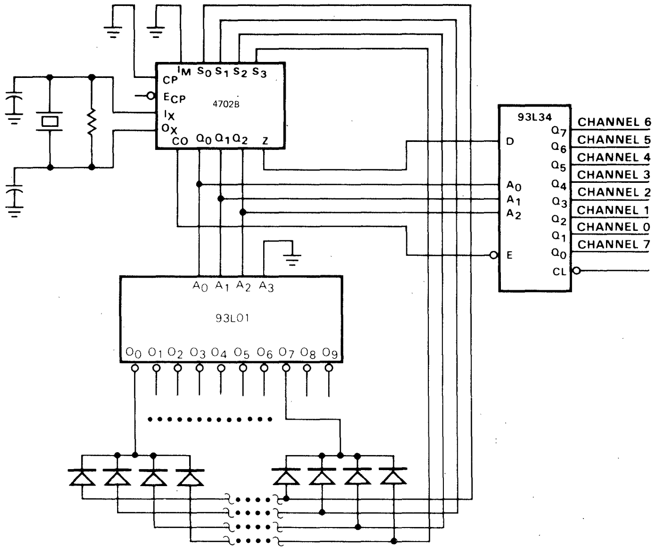


Fig. 4. Jumper Programmable 8-Channel Bit-Rate Generator

In the jumper programmable 8-channel bit-rate generator, the scan counter outputs ($Q_0 - Q_2$) are fed as Address inputs to a 93L01 decoder and a 93L34 addressable latch. The decoder outputs drive the diode clusters which contain four diodes for each channel. All four diode cathodes in a cluster are connected together to a decoder output; the anodes of corresponding diodes in every cluster are connected together to the appropriate Rate Select inputs of the 4702B. Presence of a diode results in a LOW on the particular 4702B input; when a diode is absent, a HIGH results. As the scan counter advances, the decoder outputs activate the desired bit-rate code for that channel. The 93L34 synchronously demultiplexes the 4702B output (Z) and reconstructs the specified bit rates at its output.

32 Times Frequency Bit Rates

The 4702B is designed to generate all the common communication bit rates at actual frequencies of 16 times the selected bit rate. The 16 times frequency is sufficient to operate UARTs. However, some recent LSI devices intended as UART replacements require 32 times frequency on their clock inputs. This note describes an elegant scheme to achieve this without a corresponding increase of the crystal frequency.

Figure 5 illustrates a fully programmable 8-channel system. Two 9LS170 devices are used to store the channel frequency selection information. These devices can be loaded with information on a per channel basis. For clarity, circuitry for writing into these devices is not drawn. The least significant SCAN counter outputs (Q_0 and Q_1) of the 4702B are used as the read address inputs of the 9LS170s. The most significant bit (Q_2) is used to control the read enable (RE) inputs of the 9LS170s. The $Q_0 - Q_2$ outputs of the 4702B are also the inputs to a 9LS138 decoder. The clock output (CO) of the 4702B is used to control one enable input ($\overline{E_1}$) of the 9LS138. The CO output is also the clock input (CP) for the 9LS164 shift register. The Z output of the 4702B is the data input (A) to the 9LS164. The Z output of the 4702B is also tied into an exclusive NOR gate (4077B) as one input. The second input to the exclusive-NOR gate is the Q_7 output of the 9LS164. The output of the exclusive NOR gate controls the second enable input ($\overline{E_2}$) of the 9LS138. The outputs ($\overline{O_0} - \overline{O_7}$) of the 9LS138 are the desired output clock signals.

To understand the operation of this circuit, consider the LOW-to-HIGH transition of the CO output of the 4702B when the SCAN counter outputs change from "7" (HHH) to "0" (LLL). From this transition to the next LOW-to-HIGH transition of the CO, the Z output of the 4702B reflects the state of the channel 7 counter output. The $Q_0 - Q_2$ outputs of the 4702B are LOW and hence information for channel 0 will be available on the 9LS170 outputs. The $S_0 - S_3$ inputs of the 4702B are connected to the 9LS170 outputs. On the LOW-to-HIGH transition of the CO output channel 0 counter will be clocked to the Z output. This transition also clocks the 9LS164. The SCAN counter also increments on this transition and will point to channel 1. As the clocking continues, 9LS170 locations will be read out sequentially and information will be shifted into the 9LS164. After eight clock transitions the previous channel 7 output will be at the Q_7 output of the 9LS164, and the current channel 7 output will be on the Z output of the 4702B. The output of the exclusive NOR gate will be LOW if the inputs differ; i.e. whenever the channel 7 output is to make a transition the output of the exclusive NOR gate will be LOW. The CO output is connected to the $\overline{E_2}$ input of the 93LS138 and during the negative half cycle of the clock the $\overline{O_0}$ output of the 9LS138 will be LOW. The 4702B internal counters generate 16 times the selected bit rate. The exclusive NOR gate is generating a signal whenever the selected counter is making a transition. This scheme will result in 32 times the selected bit rate. As the clocking continues each channel is serially appearing on the Q_7 output of the 9LS164 and will be compared with the corresponding current channel output. The 9LS138 will then represent the appropriate frequency at its output as shown in *Figure 5.*

Clock Expansion

The basic 4702B can be expanded to a maximum of eight channels. In applications where more than eight channels are needed, the 4702B must be duplicated. The device is designed with a clock-expansion feature; therefore only one crystal is required to operate all the channels.

The most economical expansion scheme provides one 4702B with a crystal and all other devices derive their timing from this master. The device wiring is such that the External Clock Enable input and I_X input of all but the master device feeds into the External Clock input of all the other devices. The Clock output of each device is connected to its associated 93L34 Enable input as before. An alternative scheme is shown in *Figure 6.*

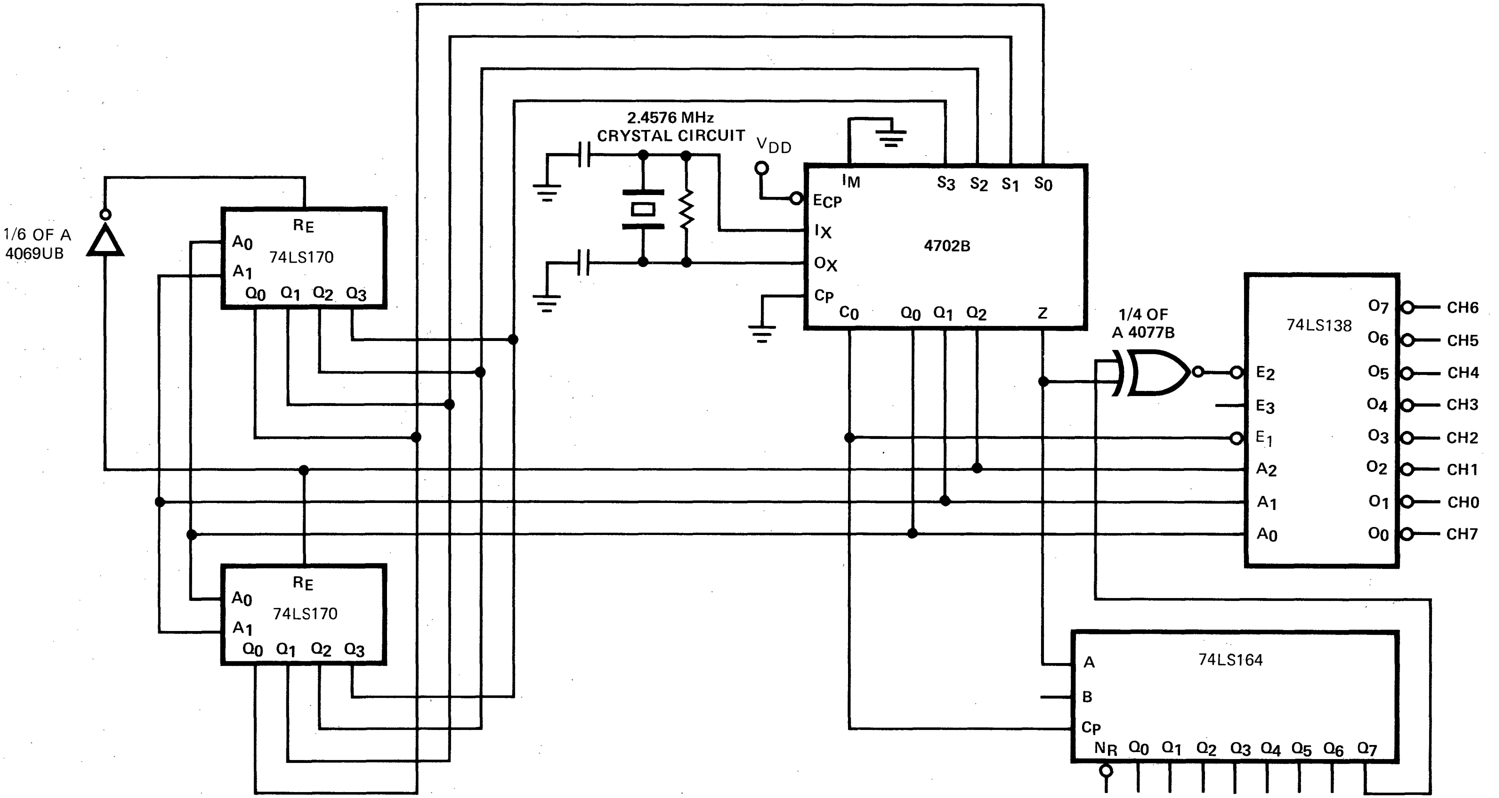


Fig. 5. A Fully Programmable 32 Times Frequency Bit Rate Generator System

The advantage of this scheme is that it can be conveniently used to implement the software external clock feature mentioned previously. Imagine that the External Clock Enable ($\overline{E}_{CP}$) inputs of all the 4702B's in the system are controlled by the output of a flip-flop (mode) and the External Clock inputs (CP) of all the devices are tied together and software driven, possibly by operating another flip-flop. During normal operation, the mode control is HIGH, thus selecting the crystal oscillator for timing. Also, the external Clock input of each device is held LOW. When the External Clock Enable goes LOW, in preparation for the diagnostic mode, all devices receive their timing from the External Clock input. When this input goes HIGH for the first time, all devices generate an internal Master Reset signal clearing their counter chains. The next HIGH-to-LOW transition sets the internal control flip-flop and thus terminates the Reset; all counters are free to start counting in response to the External Clock signal.

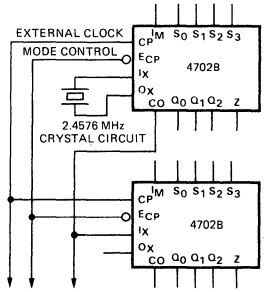


Fig. 6. Tandem Clock Expansion Scheme

USING THE 4703B FIFO

The First-In First-Out (FIFO) memory is read/write memory which automatically stacks the words in the same order as they were entered and makes them available at the output in the same sequence, thus its name first-in first-out.

Description

The 4703B FIFO is a 16 x 4 parallel/serial memory consisting of the following *(Figure 1).*

- An input register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
- A 4-bit wide, 14-word deep fall-through stack with self-contained control logic.
- An output register with parallel and serial data outputs, control inputs and outputs for output handshaking and expansion.

Parallel data is entered into the input register by using D_0 through D_3 as data inputs and Parallel Load (PL) as the strobe. A HIGH at the PL input operates the direct set and clear inputs of the input-register flip-flops. The quiescent state of the PL input is LOW.

To enter data serially, D_S is used as the data input and $\overline{\text{CPSI}}$ as the clock. The input register responds to the HIGH-to-LOW clock transition and the quiescent state of the CPSI input is LOW. For the CPSI to effect shifting, the Input Expand Serial ($\overline{\text{IES}}$) input must be LOW.

Whenever the input register receives four data bits whether by serial or parallel entry, the status output signal, Input Register Full ($\overline{\text{IRF}}$), goes LOW. If the Transfer to Stack ($\overline{\text{TTS}}$) input is activated with a LOW pulse, data from the input register is transferred into the first stack location (provided it is empty). As soon as data is transferred, the control logic attempts to initialize the input register so that it can accept another word; however, the initialization is postponed until the PL input is LOW. The device is designed so that the $\overline{\text{IRF}}$ output can be connected to the $\overline{\text{TTS}}$ input. Thus, when a data word is received by the input register, it automatically enters the stack and falls through toward the output, pausing only as needed for an "empty" location.

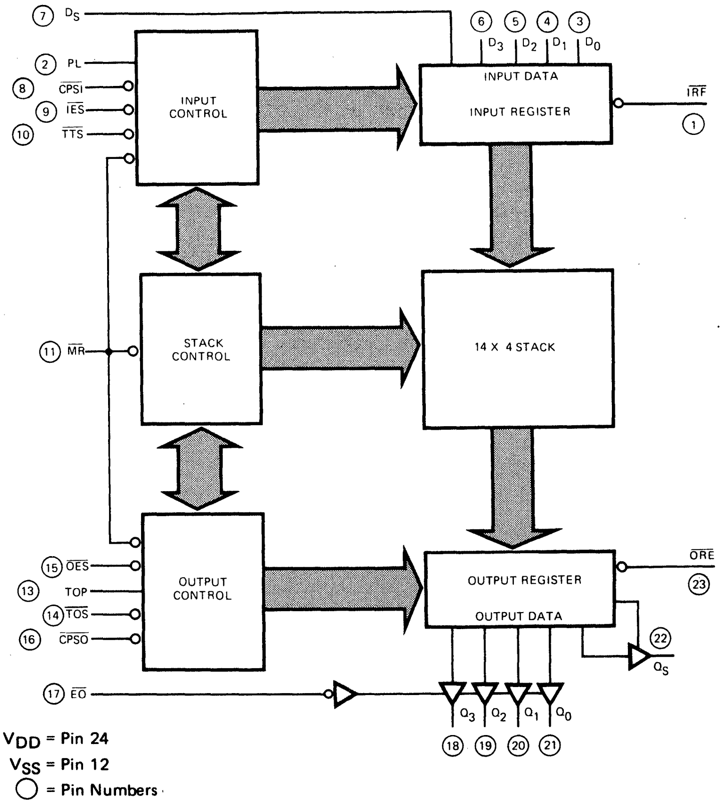
Normally, the Output Register Empty ($\overline{\text{ORE}}$) is LOW, indicating that the output register does not contain valid data. As soon as a data word arrives in the register, the $\overline{\text{ORE}}$ output goes HIGH, indicating the presence of valid data. If the Output Enable ($\overline{\text{EO}}$) input is LOW, the 3-state buffers are enabled and data is available on the O_0 through O_3 outputs.

Data can be extracted either serially or in parallel. The Q_S is used for serial data output and $\overline{\text{CPSO}}$ for the clock input. The Q_S output is also available through a 3-state buffer; however its enabling is controlled internally. Output register shifting occurs on the HIGH-to-LOW transition of the $\overline{\text{CPSO}}$ whose quiescent state is LOW. As soon as the last data bit is shifted out, the $\overline{\text{ORE}}$ output goes LOW, indicating that the output register is empty.

The quiescent state of the $\overline{\text{TOS}}$ input is LOW. A HIGH-to-LOW transition on this input causes new data to be loaded from the stack into the output register (provided data is available). The $\overline{\text{ORE}}$ output can be connected to the $\overline{\text{TOS}}$ input so that as soon as the last bit is shifted out, new data is automatically demanded.

The quiescent state of the TOP input is HIGH and a LOW-to-HIGH transition causes new data to be loaded into the output register. Moreover, a HIGH level on the TOP input causes the $\overline{\text{ORE}}$ to go LOW. The TOP input can be connected to the $\overline{\text{EO}}$ input so that the output data can be enabled when $\overline{\text{EO}}$ is LOW. When the output is disabled, new data is automatically demanded. It should be noted that the $\overline{\text{TOS}}$ input does not affect the $\overline{\text{ORE}}$ output.

The FIFO is initialized by a LOW signal on the Master Reset ($\overline{\text{MR}}$). This causes the status outputs, $\overline{\text{IRF}}$ and $\overline{\text{ORE}}$, to assume an empty state; i.e., $\overline{\text{IRF}}$ is then HIGH and $\overline{\text{ORE}}$ LOW. It is important to remember that the $\overline{\text{MR}}$ does not clear all the data flip-flops; it only initializes the control. Specifically, the O_0 – O_3 outputs are not affected by the Master Reset.



D_0 - D_3	Parallel Data Inputs
D_S	Serial Data Input
PL	Parallel Load Input
$\overline{\text{CPSI}}$	Serial Input Clock Input (HIGH-toLOW Triggered)
$\overline{\text{CPSO}}$	Serial Output Clock Input (HIGH-to-LOW Triggered)
$\overline{\text{IES}}$	Serial Input Enable (Active LOW)
$\overline{\text{TTS}}$	Transfer to Stack Input (Active LOW)
$\overline{\text{TOS}}$	Transfer Out Serial Input (Active LOW)
TOP	Transfer Out Parallel Input
$\overline{\text{OES}}$	Serial Output Enable Input (Active LOW)
$\overline{\text{EO}}$	Output Enable Input (Active LOW)
$\overline{\text{MR}}$	Master Reset Input (Active LOW)
$\overline{\text{IRF}}$	Input Register Full Output (Active LOW)
$\overline{\text{ORE}}$	Output Register Empty Output (Active LOW)
Q_0 - Q_3	Parallel Data Outputs
Q_S	Serial Data Output

Fig. 1. 4703B Block Diagram

Expansion

The 4703B can be vertically expanded to store more words or horizontally expanded to store longer words (in multiples of four bits) without external logic. Also, the expansion scheme fully preserves the parallel/serial data features. To illustrate the expansion connections, a FIFO array consisting of eight devices is shown in *Figure 2.* If there are m devices in a row and n rows, the array provides (15n + 1) words of storage with 4m bits in each word. The reduction in storage to (15n + 1) words instead of 16n is quite common in such expansion (see explanation at end of this section). Data is entered into devices 1 through 4 and extracted from devices 5 through 8.

The D_S inputs of the first four devices are bussed together and serial data is entered on this line. The $\overline{\text{CPSI}}$ inputs are also connected together for clocking the serial data. The $\overline{\text{IES}}$ input of device 1 is connected to ground, while the $\overline{\text{IES}}$ inputs of devices 2, 3 and 4 are each connected to the $\overline{\text{IRF}}$ output of the preceding device. The $\overline{\text{IRF}}$ output of device 4 feeds into the $\overline{\text{TTS}}$ inputs of all four devices.

After initialization by a LOW level on the $\overline{\text{MR}}$ input, the $\overline{\text{IRF}}$ outputs of all four devices are HIGH. Under these conditions, only device 1 responds to the $\overline{\text{CPSI}}$ because its $\overline{\text{IES}}$ input is LOW. The first four clock pulses shift four data bits into the device 1 input register; its $\overline{\text{IRF}}$ output then becomes LOW. The first data bit is located in a flip-flip corresponding to the D_0 input of device 1. Control logic inhibits the $\overline{\text{CPSI}}$ from further affecting this device.

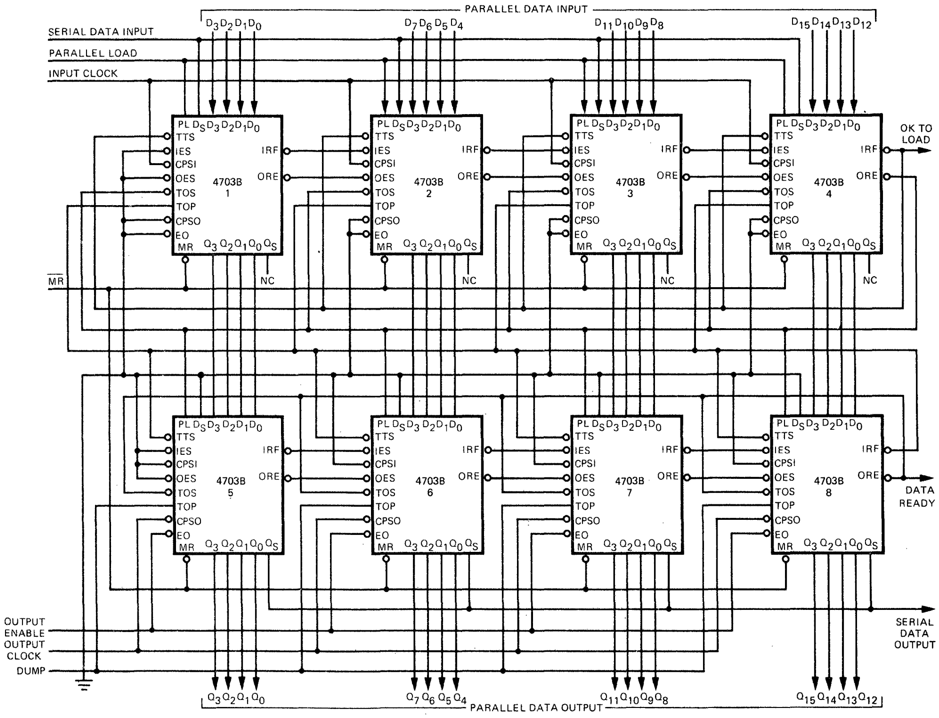


Fig. 2. 31 x 16 FIFO Array

Because the $\overline{\text{IES}}$ input of device 2 is now LOW, the clock starts shifting data into the input register of device 2. On the eighth clock pulse, the $\overline{\text{IRF}}$ output of device 2 goes LOW and disables shifting of device 2. This process continues on devices 3 and 4. Therefore, on the 16th clock pulse, the $\overline{\text{IRF}}$ output of device 4 becomes LOW and activates the $\overline{\text{TTS}}$ inputs of all devices. The stack control logic in each device responds by transferring data into each stack from the respective input register, and the input registers are initialized. Thus the $\overline{\text{IRF}}$ outputs of all devices become HIGH once again. An automatic priority scheme assures that if the $\overline{\text{IRF}}$ output of device 4 is HIGH, the input registers of all four devices have been initialized. The timing diagram for 16 bits of serial entry into the array is shown in *Figure 3.*

Parallel entry into the array is made with a HIGH level on the PL inputs. The same conditions prevail in the input section that exist after the 16th clock pulse in the serial entry mode. The stack controls do not initialize the input registers until the PL inputs are LOW to assure proper device operation.

Data loaded into the stacks eventually arrives at the output registers of the first four devices. Normally, the $\overline{\text{ORE}}$ outputs are LOW due to initialization; however, as soon as data is loaded into each output register, the $\overline{\text{ORE}}$ goes HIGH. An automatic priority scheme, similar to the one for data entry, also exists at the output. Thus a HIGH level on the $\overline{\text{ORE}}$ output of device 4 guarantees that valid data is present in all the output registers.

The $\overline{\text{ORE}}$ output of device 4 is connected to the PL inputs of devices 5 through 8, as well as to the $\overline{\text{TOS}}$ inputs of the first four devices. It should be noted that if serial extraction from the output is not desired, the $\overline{\text{TOS}}$ inputs can be connected to ground instead. The $\overline{\text{EO}}$ inputs of the first four devices are connected to ground; thus the contents of an output register are available on the appropriate outputs.

The HIGH level on the $\overline{\text{ORE}}$ outputs of device 4 activates the PL inputs of devices 5 – 8, thus forcing the data outputs from each device in the first row into the input register of the corresponding device in the second row. The $\overline{\text{IRF}}$ output of device 8 is connected to the TOP inputs of devices 1 – 4 and to the $\overline{\text{TTS}}$ inputs of devices 5 – 8. Because the PL inputs are HIGH, the $\overline{\text{IRF}}$ outputs of devices 5 – 8 are LOW, therefore establishing a LOW on the TOP inputs of devices 1 – 4. This causes the $\overline{\text{ORE}}$ of devices 1 – 4 to

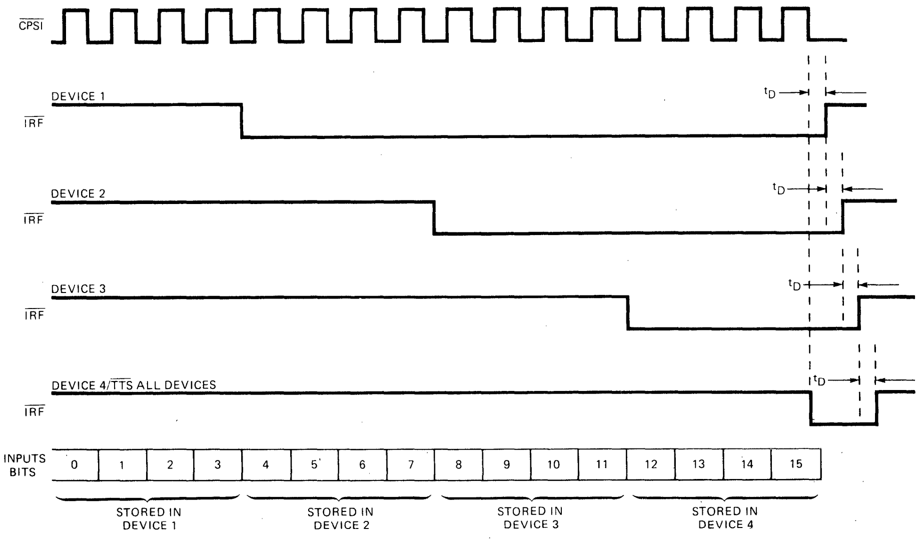


Fig. 3. Serial Data Entry for FIFO Array

go LOW and hence the PL inputs to devices 5 – 8. Furthermore, the LOW on the $\overline{IRF}$ output of device 8 also activates the $\overline{TTS}$ inputs of devices 5 – 8, thus initiating a fall-through action. The stack controls in devices 5 – 8 initialize their respective registers and the $\overline{IRF}$ outputs go HIGH. An automatic priority scheme is also present at the inputs of devices 5 – 8. The HIGH on the $\overline{IRF}$ output of device 8 restores the TOP inputs of devices 1 – 4 to the quiescent state.

If the stacks of devices 5 – 8 are full, activating the $\overline{TTS}$ inputs by the LOW $\overline{IRF}$ output of device 8 would not initiate a data transfer from the input registers. The $\overline{IRF}$ output of device 8 would remain LOW until the data can be successfully transferred into the stacks. Thus, as long as devices 5 – 8 are holding 16 words, the $\overline{IRF}$ output of device 8 remains LOW. This also holds the TOP inputs of devices 1 – 4 LOW. As long as they remain LOW, data cannot be loaded into the output registers from the stacks because a LOW-to-HIGH transition at the TOP inputs is needed to demand new data. Under these circumstances, devices 1 – 4 temporarily lose the ability to use their output registers and hence can hold only 15 words. As a result, the two rows have a storage capacity of 31 words instead of 32; and, for the general case, the storage capacity of an n-row array is (15n + 1) instead of 16n.

The data loaded into the stacks eventually arrives at the output registers of devices 5 – 8, at which time the $\overline{ORE}$ outputs go HIGH from the LOW state originally initialized by the $\overline{MR}$ input. The automatic priority scheme is still in effect, and the data from the output can be extracted either in serial or parallel format.

The Q_S outputs of devices 5 – 8, each available through a 3-state buffer, are connected together and the serial data output from the array appears on this line. The $\overline{CPSO}$ inputs are also connected together and the line driven by the output clock. When there is no valid data in the output register, Q_S is disabled and is therefore in a high impedance state.

The $\overline{OES}$ input of device 5 is connected to ground and device 6, 7 and 8 each receive its $\overline{OES}$ input from the preceding device. As soon as data arrives in the output registers of devices 5 – 8, the $\overline{ORE}$ outputs go HIGH and the 3-state buffer of device 5 is enabled so that its Q_S output becomes identical to its Q_0 output. The Q_S outputs of devices 5 – 8 are in a high impedance state. The clock on the $\overline{CPSO}$ input shifts the device 5 output register and data is shifted out in the same bit order as entered at the array input. After the fourth clcok pulse, the $\overline{ORE}$ output of device 5 goes LOW and its Q_S output is disabled into the high impedance state.

The $\overline{ORE}$ output of device 5 establishes a LOW on the $\overline{OES}$ input of device 6. This enables its Q_S output buffer and a signal, corresponding to that of the Q_0 output, appears on the serial output line. Device 6 now responds to the clock inputs and, after shifting the data out, its Q_S output goes into a high impedance mode. The LOW on the $\overline{ORE}$ output of device 6 enables device 7. This process continues until the last data bit has been shifted out of device 8, at which time its $\overline{ORE}$ output goes LOW. This activates the $\overline{TOS}$ inputs of devices 5 – 8 and new data can then be loaded from the stack when available. The timing diagram for 16 bits of serial data extraction is shown in *Figure 4.*

Data can be extracted from the array in parallel by activating the TOP inputs of devices 5 – 8 LOW. New data is loaded into the output registers on the LOW-to-HIGH transition of this input. The TOP and $\overline{EO}$ inputs can be connected together so that data can be automatically extracted.

Automatic Priority Scheme

Most conventional FIFO designs provide status signals analogous to the $\overline{IRF}$ and $\overline{ORE}$ outputs. However, when these devices are operated in arrays, unit-to-unit delay variations require external gating to avoid transient false-status indications. This is commonly referred to as composite-status signal generation. The design of the 4703B FIFO eliminates this problem. An automatic priority feature is built in to assure that a slow device will automatically predominate, irrespective of location in the array.

In *Figure 3,* devices 1 and 5 are defined as "row masters". Devices 2, 3 and 4 are "slaves" to device 1 while devices 6, 7 and 8 are slaves to device 5. The row master is established by sensing the $\overline{IES}$ input during the period when the $\overline{MR}$ input is LOW. Because of the initialization, the $\overline{IRF}$ outputs of all devices are HIGH for a short time after the HIGH-to-LOW transition of the $\overline{MR}$ input. Thus $\overline{IES}$ inputs of all devices except 1 and 5 are HIGH. This condition is sensed by the device logic to establish the row mastership.

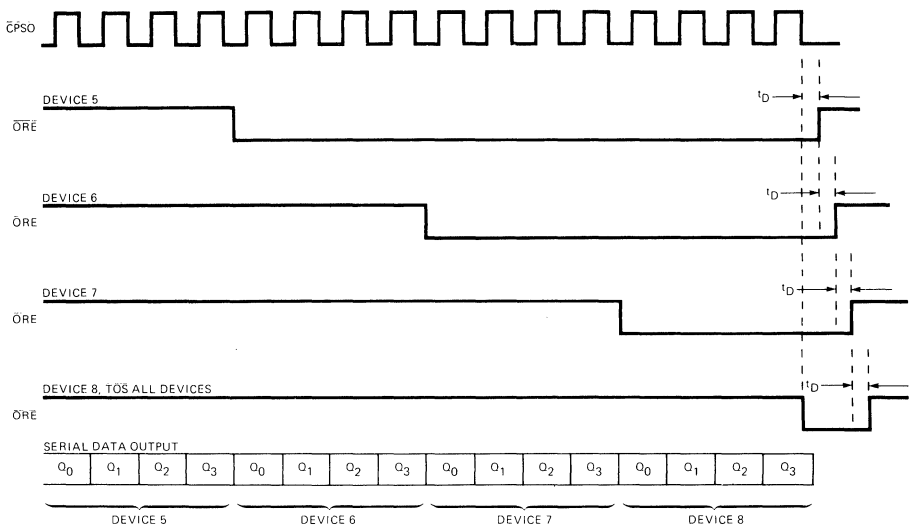


Fig. 4. Serial Data Extraction for FIFO Array

All devices in any given row transfer data from their input registers into the corresponding stacks simultaneously. However, no slave can initialize its input register until its $\overline{\text{IES}}$ input goes HIGH. Thus initialization starts with the row master and eventually ends at the last slave in the row.

A similar situation occurs at the output registers of all devices in a row. They are loaded simultaneously from corresponding stacks; however, the $\overline{\text{ORE}}$ ouput of a slave cannot go HIGH until its $\overline{\text{OES}}$ input is HIGH. Thus the row master is the first to indicate a HIGH on its $\overline{\text{ORE}}$ and eventually the slaves will follow. It should be pointed out that this automatic priority scheme reduces the maximum operation speed of the array. If speed is essential, the master-slave hierarchy can be replaced by the traditional composite-status signal-generation scheme, which requires external gating.

Other Expansion Schemes

The expansion scheme illustrated in *Figure 3* is quite simple and straightforward. It does not require any external support logic to achieve the desired expansion and retains all the serial/parallel features. However, these advantages are not without sacrifice—one storage location is eliminated at the interface between rows—and the n-row array has a storage capacity of 15n + 1 instead of 16n words. Moreover, the automatic priority scheme results in a ripple action from row master to the last slave in that row for the status signaling. This reduces the maximum operation frequency of an array and the inherent speed of the individual devices is not fully utilized.

The 4703B FIFO, because of its versatility, can be used to overcome both above disadvantages with minimum external logic. A vertically expended array, consisting of three FIFOs, yields 16n words of storage for an n-row array *(Figure 5).* After initialization by a LOW level on the $\overline{\text{MR}}$ inputs, the $\overline{\text{IRF}}$ outputs of all three devices are HIGH and the $\overline{\text{ORE}}$ outputs LOW. The AND gates (4081B) at the row interface are thus disabled. The PL inputs of devices 2 and 3 are LOW. Now, if the input register of device 1 receives four bits of data, then $\overline{\text{IRF}}$ output goes LOW. This activates the $\overline{\text{TTS}}$ input and the data falls through into the output register of device 1 and the $\overline{\text{ORE}}$ output becomes HIGH. Since the $\overline{\text{IRF}}$ output of device 2 is HIGH from initialization, the AND gate between devices 1 and 2 is enabled and the PL input of device 2 becomes HIGH. Data from device 1 is loaded into the input register of device 2 causing the $\overline{\text{IRF}}$ output of device 2

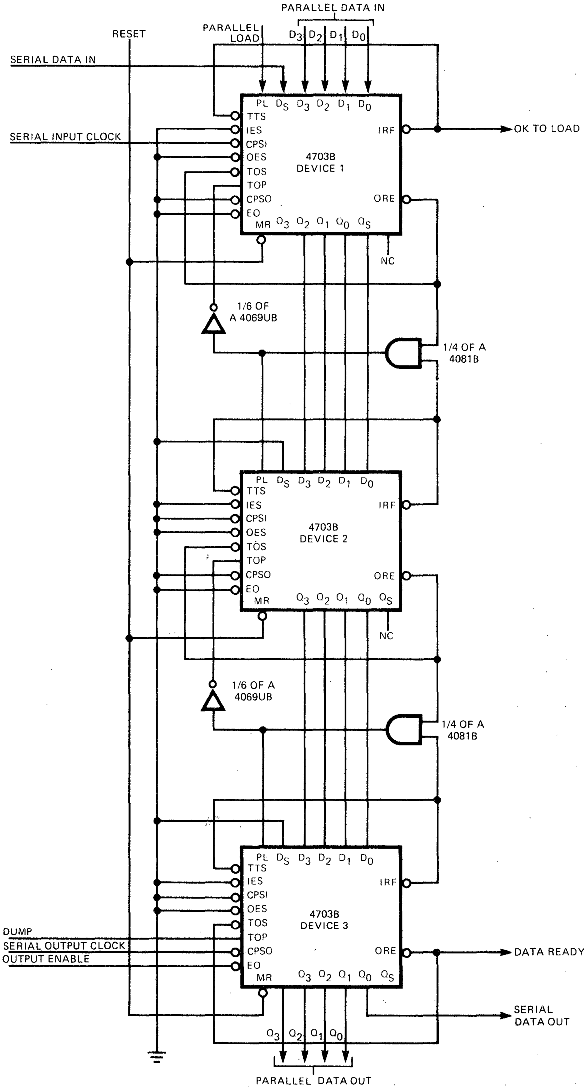


Fig. 5. Expansion without Sacrificing a Storage Location at the Interface

to go LOW. Moreover, a HIGH level on the PL input of device 2 results in a LOW level on the TOP input of device 1. As a result, the $\overline{\text{ORE}}$ output of device 1 also becomes LOW. Either way, the AND gate is disabled and the PL input of device 2 goes LOW and the TOP input of device 1 becomes HIGH.

The LOW level on the $\overline{\text{IRF}}$ output of device 2 activates its $\overline{\text{TTS}}$ input and initiates a fall-through action; the data appears at the output register. Because the TOP input of device 1 is HIGH, new data arrives at the device 2 output register. When data appears at the output of device 2, the AND gate at the interface of devices 2 and 3 is enabled. By a similar action described above, device 3 takes the data word into its input register and passes it on to the output. Thus, if 16 words are loaded at the input to the array, the 1st word is located in the output and the 16th word is in the input register of device 3. Device 3 is full now and its $\overline{\text{IRF}}$ output remains LOW until data is extracted. This LOW level disables the AND gate between devices 2 and 3 and hence any arrival of new data into the output register of device 2 does not activate the PL input of device 3. As new data is received, it is arranged in devices 1 and 2 so that the 17th data word falls into the device 2 output register and the 48th word remains in the input register of device 1. Forty-eight data words fill all devices in the array. Under these conditions, the status output is as follows: the $\overline{\text{IRF}}$ outputs of devices 1, 2 and 3 are LOW and the $\overline{\text{ORE}}$ outputs of devices 1, 2 and 3 HIGH.

The data extraction takes place when the TOP input of device 3 is activated; normally it is HIGH. To extract data, TOP is made LOW and then HIGH. When the TOP input is LOW, the $\overline{\text{ORE}}$ of device 3 goes LOW. When TOP is returned HIGH, data is demanded from the stack.

The internal control in device 3 loads the second data word into the output register and the $\overline{\text{ORE}}$ goes HIGH. The internal control also initiates a fall-through action in device 3. Thus, the 16th data word that was located in the input register is transferred into the device 3 stack and the input register is initialized. Thus, the $\overline{\text{IRF}}$ output of device 3 becomes HIGH.

The 17th data word is located in the output register of device 2, hence the $\overline{\text{ORE}}$ output is HIGH. When the $\overline{\text{IRF}}$ output of device 3 becomes HIGH, the AND gate at the interface causes the PL input of device 3 to go HIGH and the TOP input of device 2 LOW. The 17th data word then goes into the input register of device 3. The internal control of device 2 initiates fall-through action so that the 18th word falls into the output and the 32nd word is transferred into the stack. This results in a HIGH at the $\overline{\text{IRF}}$ output of device 2. Similar action takes place between devices 1 and 2 with the net result that all data has fallen one location creating a vacancy in the input register of device 1. It is now clear that this FIFO array has a 48-word capacity without affecting the serial/parallel data feature at the input or the output. It can then be concluded that if an array of n rows is constructed using the proposed scheme, the effective storage capacity of the FIFO is 16n words.

The array of *Figure 6* has all the features and yet operates at a higher speed than the array shown in *Figure 2.* Whenever the $\overline{\text{IRF}}$ output of device 1 is HIGH, the $\overline{\text{IES}}$ inputs of devices 2, 3 and 4 are also HIGH. Therefore, when the array is initialized by a LOW level on the $\overline{\text{MR}}$ inputs, device 1 is the row master and devices 2, 3 and 4 are the slaves. In the second row of devices, the $\overline{\text{IRF}}$s and $\overline{\text{IES}}$s are interconnected so that device 5 is also a row master and devices 6, 7 and 8 are slaves.

When serial data is entered into the array, device 1 receives the first four bits of data. Devices 2, 3 and 4 do not respond to the clock since all three $\overline{\text{IES}}$ inputs are HIGH. After the 4th bit, the $\overline{\text{IRF}}$ output of device 1 is LOW. This disables device 1 from responding to the clock and enables device 1 so that the next four bits are entered into device 2. Devices 3 and 4 remain disabled by a HIGH level on the $\overline{\text{IES}}$ inputs. After the 8th bit, the $\overline{\text{IRF}}$ of device 2 becomes LOW, thus disabling device 2 and enabling device 3. After the 12th bit, the $\overline{\text{IRF}}$ output of device 3 is LOW and thus device 4 is enabled. After the 16th bit, the $\overline{\text{IRF}}$ output of device 4 is LOW. So far, the serial data entry into this array is identical to that for the array in *Figure 2.*

The LOW level on the $\overline{\text{IRF}}$ output of device 4 activates the $\overline{\text{TTS}}$ inputs of all 4 devices, causing the transfer of data into the stacks. Although all devices transfer data into the stack simultaneously, device 1 (row master) is the first to initialize its input register. Since devices 2, 3 and 4 are slaves, they need a HIGH on their $\overline{\text{IES}}$ inputs for input-register initialization. As soon as the $\overline{\text{IRF}}$ output of device 1 goes HIGH due to initialization, the $\overline{\text{IES}}$ inputs of devices 2, 3 and 4 become HIGH and their input registers are initialized simultaneously. This is in contrast to *Figure 2* where device 3 has to wait for device 2 to initialize, etc. The ripple action of input initialization has been overcome by simple gating. The $\overline{\text{IRF}}$ outputs of devices 1,

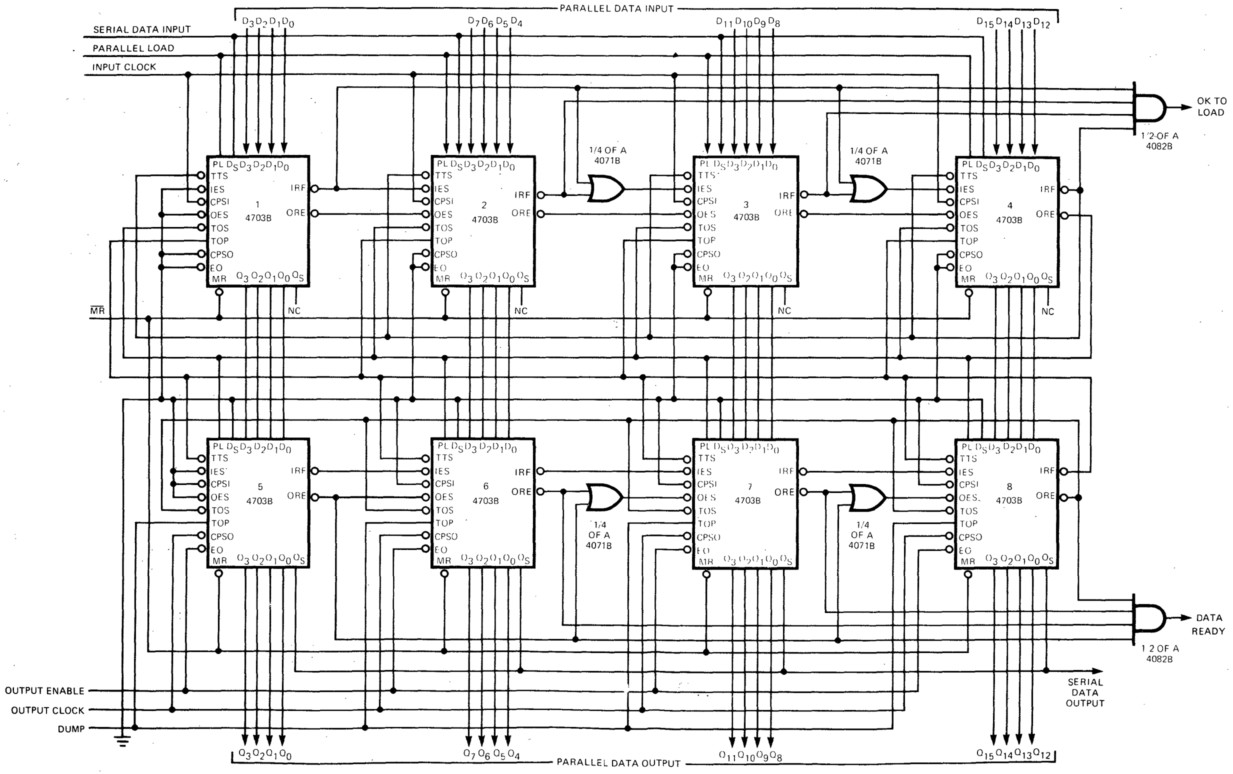


Fig. 6. Expansion with Priority Defeated for Faster Operation

2, 3 and 4 are fed into 4-input AND gates (4082B) to generate the composite input status. To obtain an indication that the input register of the array is empty, the input register of each device in the first row should be empty.

The $\overline{\text{ORE}}$ and $\overline{\text{OES}}$ interconnections for the second row are essentially similar to the input section. This gating at the output section eliminates the rippling effect of the output status indication. If the gating arrangement used in *Figure 5* is incorporated into the array of *Figure 6,* the result is a 32 word x 16-bit FIFO network.

As shown in *Figure 8,* higher FIFO speeds may also be attained by adding one 4518B and implementing a multiplexed expansion scheme. *Figure 7* shows the conventional horizontally expanded 8-bit array with 16 words of storage.

Serial data is entered using the D_S as the data input and $\overline{\text{CPSI}}$ as the clock input. Shifting takes place on the HIGH-to-LOW transition of the $\overline{\text{CPSI}}$ input. When the first four bits of data are entered into device 1, its $\overline{\text{IRF}}$ output goes LOW indicating that its input register is full. The LOW on the $\overline{\text{IRF}}$ output of device 1 enables device 2 and disables device 1. Device 2 will shift the next four data bits into its input register. When the input register of device 2 is full, its $\overline{\text{IRF}}$ output goes LOW. The LOW on the $\overline{\text{IRF}}$ output of device 2 activates the $\overline{\text{TTS}}$ inputs of both devices. Thus, data from the input registers of both devices is loaded into their respective stacks simultaneously. The control logic in each device then initializes its input register in preparation to accept more incoming data.

In *Figure 7,* device 1 is called the row master and is privileged to initialize its input register first. This results in a HIGH on its $\overline{\text{IRF}}$ output. Device 2 (slave) senses this and allows its $\overline{\text{IRF}}$ to go HIGH. This master/slave scheme is built into the 4703B so that device to device speed variations do not cause transient false status indications. However, this is effectively a ripple action and limits the ultimate operating speed of the array. A multiplexing scheme is proposed that achieves much higher operating speeds.

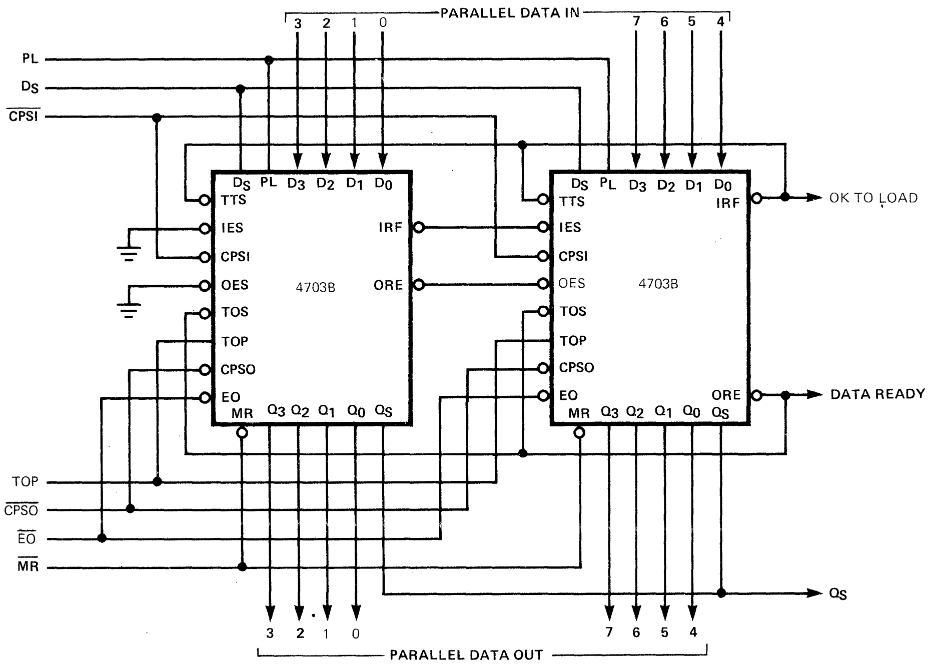


Fig. 7. Conventional 8 Bit Array

Figure 8 shows another 8-bit network incorporating one 4518B counter. The Q_3 output of the input counter controls the $\overline{\text{IES}}$ inputs of the FIFO's. When the array is reset by a LOW pulse on the Master Reset input ($\overline{\text{MR}}$), the $\overline{\text{IES}}$ input of device 1 is LOW and that of device 2 is HIGH. This establishes device 1 as the master and device 2 as the slave. The first four bits of data are entered into device 1. On the fourth HIGH-to-LOW transition of the clock, the Q_3 output of the counter changes. The $\overline{\text{IES}}$ input of device 1 goes HIGH and disables its input register from shifting. The $\overline{\text{IES}}$ input of device 2 goes LOW and enables its input register to shift allowing the next four data bits to be shifted into device 2. While shifting into device 2 is occuring, the $\overline{\text{IRF}}$ output of device 1 will become LOW some propagation delay after the fourth clock transition. The $\overline{\text{TTS}}$ input of device 1 is activated. This causes the data to fall through into the stack. Device 1, being the row master, will initialize its input register. On the eighth clock transition the Q_3 output of the counter changes again. The $\overline{\text{IES}}$ input of device 1 will be LOW and the $\overline{\text{IES}}$ input of device 2 will be HIGH. While device 1 is receiving data, device 2 can transfer its data into the stack and intialize its input register.

A similar scheme is used at the output. The other half of a 4518B counter is used to control the $\overline{\text{OES}}$ inputs. A HIGH-to-LOW transition of the $\overline{\text{CPSO}}$ input shifts data out on the Q_S output. A connection between the $\overline{\text{ORE}}$ output and the $\overline{\text{TOS}}$ input provides automatic data extraction after shifting out four bits of data from a device.

Figure 9 illustrates another multiplexed expansion scheme using a 4027B Dual JK Flip-Flop. Referring back to *Figure 7,* the propagation delays are as follows:

(a) T_1 is the delay from the HIGH-to-LOW transition of $\overline{\text{CPSI}}$ to $\overline{\text{IRF}}$ going LOW at device 2. Typical value is 81 nsec at $V_{DD} = 10$ V.

(b) T_2 is the delay from $\overline{\text{TTS}}$ going LOW to $\overline{\text{IRF}}$ going HIGH at device 1. Typical value is 131 nsec at $V_{DD} = 10$ V.

(c) T_3 is the delay from $\overline{\text{IES}}$ going HIGH to $\overline{\text{IRF}}$ going HIGH at device 2. Typical value is 112 nsec at $V_{DD} = 10$ V.

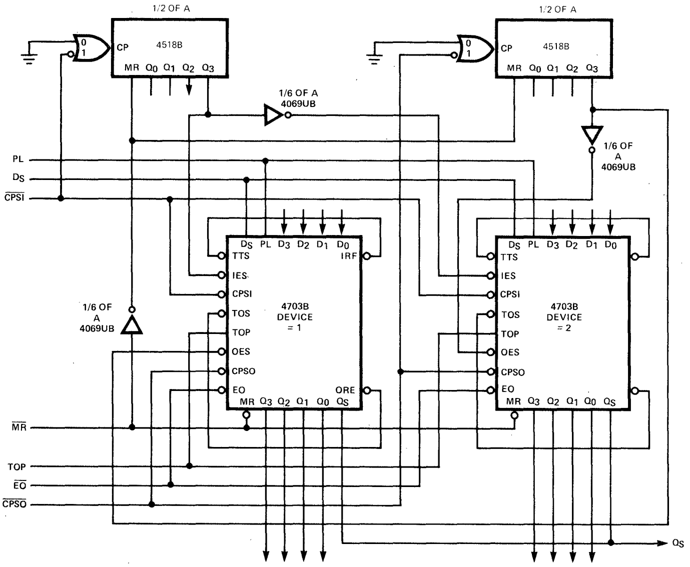


Fig. 8. A Multiplexed Expansion Scheme

A new data word cannot begin shifting into device 1 until the $\overline{\text{IRF}}$ output of device 2 is HIGH. Thus, the $\overline{\text{CPSI}}$ clock period is $T_1 + T_2 + T_3$ or 324 nsec typical at $V_{DD} = 10$ V.

Figure 9 shows another 8-bit network using multiplexed $\overline{\text{IES}}$ inputs. When the array is reset by a LOW pulse on the Master Reset input ($\overline{\text{MR}}$), the $\overline{\text{IES}}$ input of device 1 is LOW and the $\overline{\text{IES}}$ input of device 2 is HIGH. This establishes device 1 as the row master and device 2 as the slave. The first HIGH-to-LOW $\overline{\text{CPSI}}$ transition shifts the first data bit into device 1. This transition complements the flip-flop also. The $\overline{\text{IES}}$ of device 1 goes HIGH and the $\overline{\text{IES}}$ of device 2 goes LOW. The second data bit will shift into device 2 and the flip-flop toggles again. The third data bit will shift into device 1 and so on. When the seventh data bit is shifted into device 1, its input register becomes full. The $\overline{\text{IRF}}$ output becomes LOW; thus, the $\overline{\text{TTS}}$ input of device 1 is activated. This causes the device 1 to transfer its data into its stack and initialize its input register. In the meantime device 2 can receive the eighth data bit. In *Figure 9* the propagation delays are as follows:

(a) T_1 is the delay from the HIGH-to-LOW $\overline{\text{CPSI}}$ transition to $\overline{\text{IRF}}$ going LOW at both devices 1 and 2. Typical value is 81 nsec at $V_{DD} = 10$ V.

(b) T_2 is the delay from $\overline{\text{TTS}}$ going LOW to $\overline{\text{IRF}}$ going HIGH for both devices 1 and 2. Typical value is 131 nsec at $V_{DD} = 10$ V.

The $\overline{\text{CPSI}}$ clock period in *Figure 9* is then $T_1 + T_2$ or 212 nsec typical at $V_{DD} = 10$ V. This is a significant improvement over that calculated for *Figure 7.*

A similar flip-flop scheme is used at the output to control the $\overline{\text{OES}}$ inputs. The HIGH-to-LOW transition of the $\overline{\text{CPSO}}$ shifts out the data on the Q_S output. Note that serial data bits come out in the same order as they are entered at the input. The connection between the $\overline{\text{ORE}}$ and $\overline{\text{TOS}}$ of the devices is to accomplish automatic data extraction after shifting their four bits of data.

It should be noted that if any attempt is made to clock data at the input when both $\overline{\text{IRF}}$ outputs are LOW, a data overrun conditon exists. A LOW on the $\overline{\text{IRF}}$ input indicates that the input register is full. Similarly, if the $\overline{\text{ORE}}$ outputs are LOW and an attempt is made to shift out data, then an overrun condition exists, also. A LOW on the $\overline{\text{ORE}}$ indicates that no valid information is present in the output register.

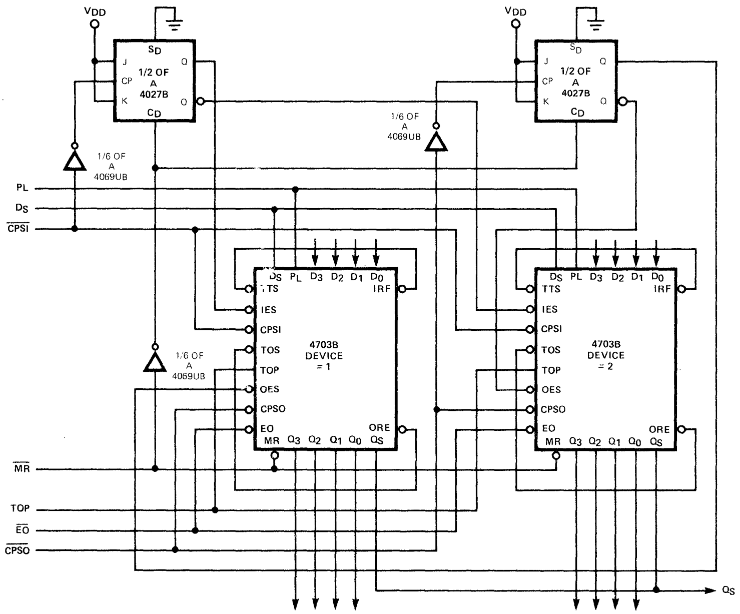
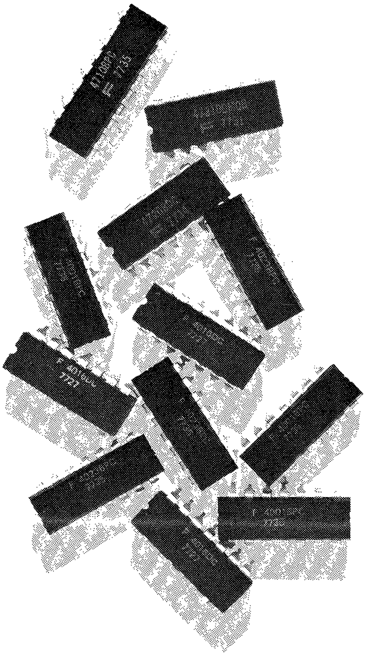


Fig. 9. A Multiplexed Expansion Scheme

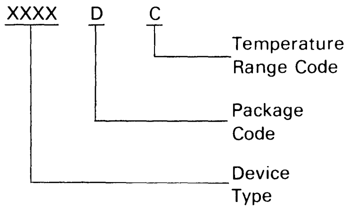


ORDER AND PACKAGE INFORMATION

Fairchild integrated circuits may be ordered using a simplified purchasing code where the package style and temperature range are defined as follows:

PACKAGE STYLE

D = Dual In-line – Ceramic (hermetic)
P = Dual In-line – Plastic
F = Flatpak



In order to accommodate varying die sizes and numbers of pins (14, 16, 24, etc.), a number of different package forms are required. The Package Information list on the following pages indicates the specific package codes currently used for each device type. The detailed package outline corresponding to each package code is shown at the end of this section.

Temperature Range

Two basic temperature grades are in common use: C = Commercial-Industrial, –40°C to +85°C; M = Military, –55°C to +125°C. Exact values and conditions are indicated on the data sheets.

Examples

(a) 4014BFM
This number code indicates a 4014B Register in a Flatpak with military temperature rating.

(b) 4720BDC
This number code indicates a 4720B 256 x 1 RAM in a ceramic Dual In-line Package with commercial temperature rating.

(d) 40014BPC
This number code indicates a 40014B Hex Schmitt Trigger in a plastic package with a commercial temperature rating.

Device Identification/Marking

All Fairchild standard catalog integrated circuits will be marked as follows:

ORDER AND PACKAGE INFORMATION

CMOS PACKAGE INFORMATION

DEVICE	MILITARY (M) −55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL −40°C to +85°C	
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)
4001B	6A	3I	6A	9A
4002B	6A	3I	6A	9A
4006B	6A	3I	6A	9A
4007UB	6A	3I	6A	9A
4008B	6B	4L	6B	9B
4011B	6A	3I	6A	9A
4012B	6A	3I	6A	9A
4013B	6A	3I	6A	9A
4014B	6B	4L	6B	9B
4015B	6B	4L	6B	9B
4016B	6A	3I	6A	9A
4017B	6B	4L	6B	9B
4019B	6B	4L	6B	9B
4020B	6B	4L	6B	9B
4021B	6B	4L	6B	9B
4022B	6B	4L	6B	9B
4023B	6A	3I	6A	9A
4024B	6A	3I	6A	9A
4025B	6A	3I	6A	9A
4027B	6B	4L	6B	9B
4028B	6B	4L	6B	9B
4029B	6B	4L	6B	9B
4030B	6A	3I	6A	9A
4031B	6B	4L	6B	9B
4034B	6N	4M	6N	9N
4035B	6B	4L	6B	9B
4040B	6B	4L	6B	9B
4042B	6B	4L	6B	9B
4044B	6B	4L	6B	9B
4045B	6B	4L	6B	9B
4046B	6B	4L	6B	9B
4047B	6A	3I	6A	9A
4049B	6B	4L	6B	9B
4050B	6B	4L	6B	9B
4051B	6B	4L	6B	9B
4052B	6B	4L	6B	9B
4053B	6B	4L	6B	9B
4066B	6A	3I	6A	9A
4067B	6N	4M	6N	9N
4069UB	6A	3I	6A	9A
4070B	6A	3I	6A	9A
4071B	6A	3I	6A	9A
4076B	6B	4L	6B	9B
4081B	6A	3I	6A	9A
4086B	6A	3I	6A	9A
4093B	6A	3I	6A	9A

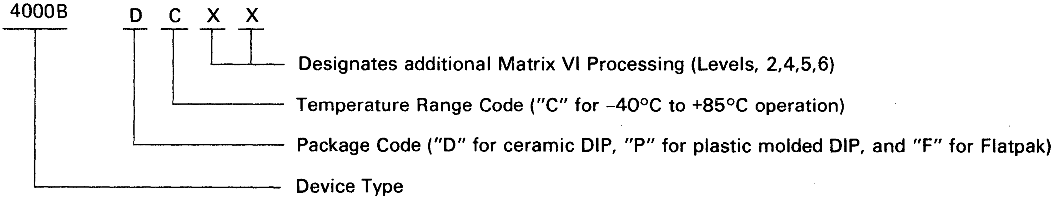
CMOS PACKAGE INFORMATION (Cont'd)

DEVICE	MILITARY (M) −55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL −40°C to +85°C	
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)
4104B	6B	4L	6B	9B
4510B	6B	4L	6B	9B
4511B	6B	4L	6B	9B
4512B	6B	4L	6B	9B
4514B	6N	4M	6N	9N
4515B	6N	4M	6N	9N
4516B	6B	4L	6B	9B
4518B	6B	4L	6B	9B
4520B	6B	4L	6B	9B
4521B	6B	4L	6B	9B
4522B	6B	4L	6B	9B
4526B	6B	4L	6B	9B
4527B	6B	4L	6B	9B
4528B	6B	4L	6B	9B
4539B	6B	4L	6B	9B
4543B	6B	4L	6B	9B
4555B	6B	4L	6B	9B
4556B	6B	4L	6B	9B
4557B	6B	4L	6B	9B
4702B	6B	4L	6B	9B
4703B	6Q	4M	6Q	9U
4710B	7D		7D	9M
4720B	7B	4L	7B	9B
4722B	6B	4L	6B	9B
4723B	6B	4L	6B	9B
4724B	6B	4L	6B	9B
4725B	6B	4L	6B	9B
4727B	6A	3I	6A	9A
4731B	6A	4L	6A	9A
4741B	6B	4L	6B	9B
40014B	6A	3I	6A	9A
40085B	6B	4L	6B	9B
40097B	6B	4L	6B	9B
40098B	6B	4L	6B	9B
40161B	6B	4L	6B	9B
40163B	6B	4L	6B	9B
40174B	6B	4L	6B	9B
40175B	6B	4L	6B	9B
40193B	6B	4L	6B	9B
6508B	6B	4L	6B	9B
6518B	7D	TBA	7D	9M

MATRIX VI PROGRAM ORDERING INFORMATION

Matrix VI is a full spectrum/cost effective reliability and quality program for commercial/industrial ICs only. It features six levels of screening/package flows, each tailored to a user's field application/environment and his incoming quality/equipment reliability requirements.

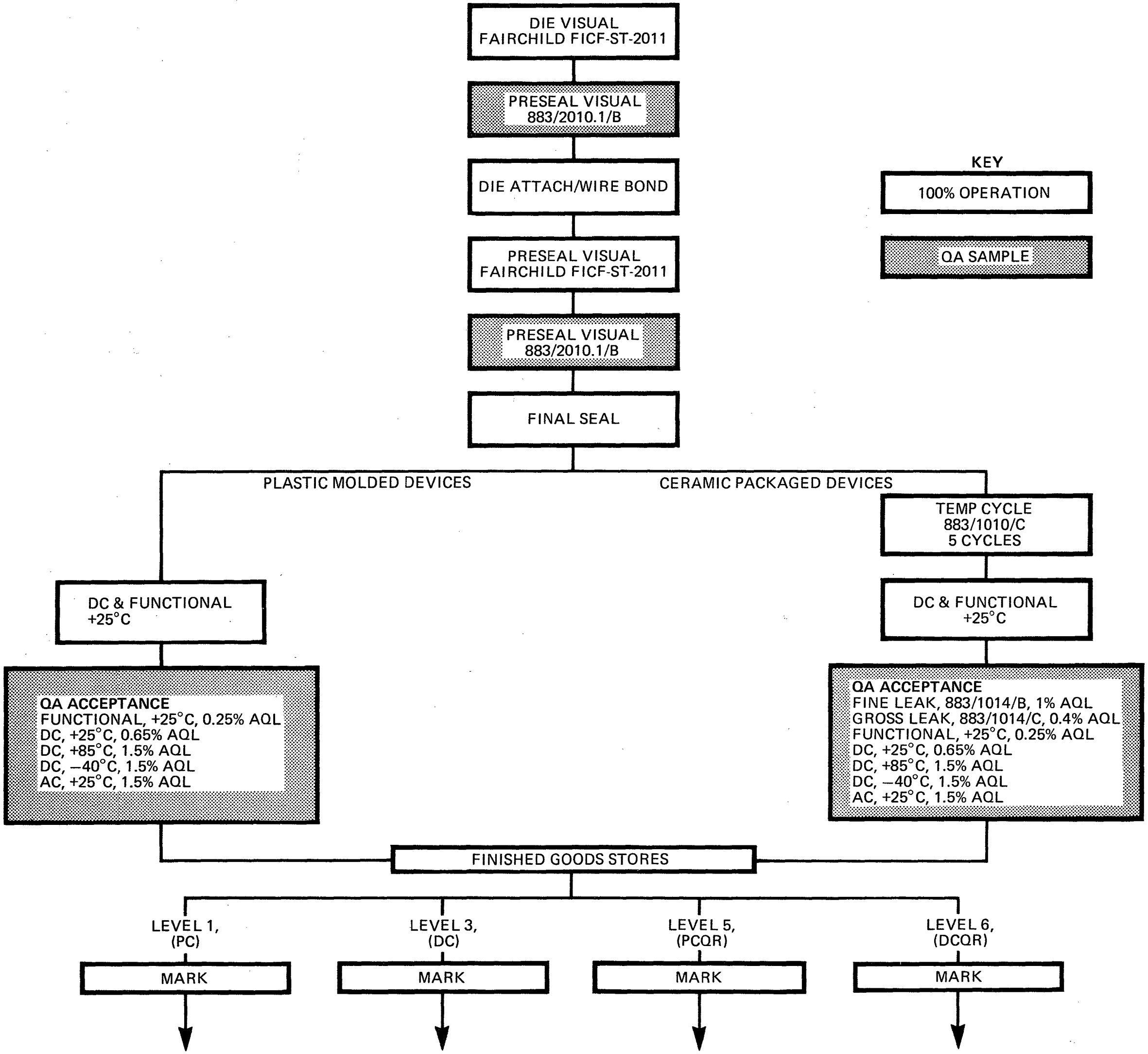
A Matrix VI part number consists of the device type followed by the package code letter, the temperature range code letter, and the Matrix VI code letter (as applicable, see flow chart).

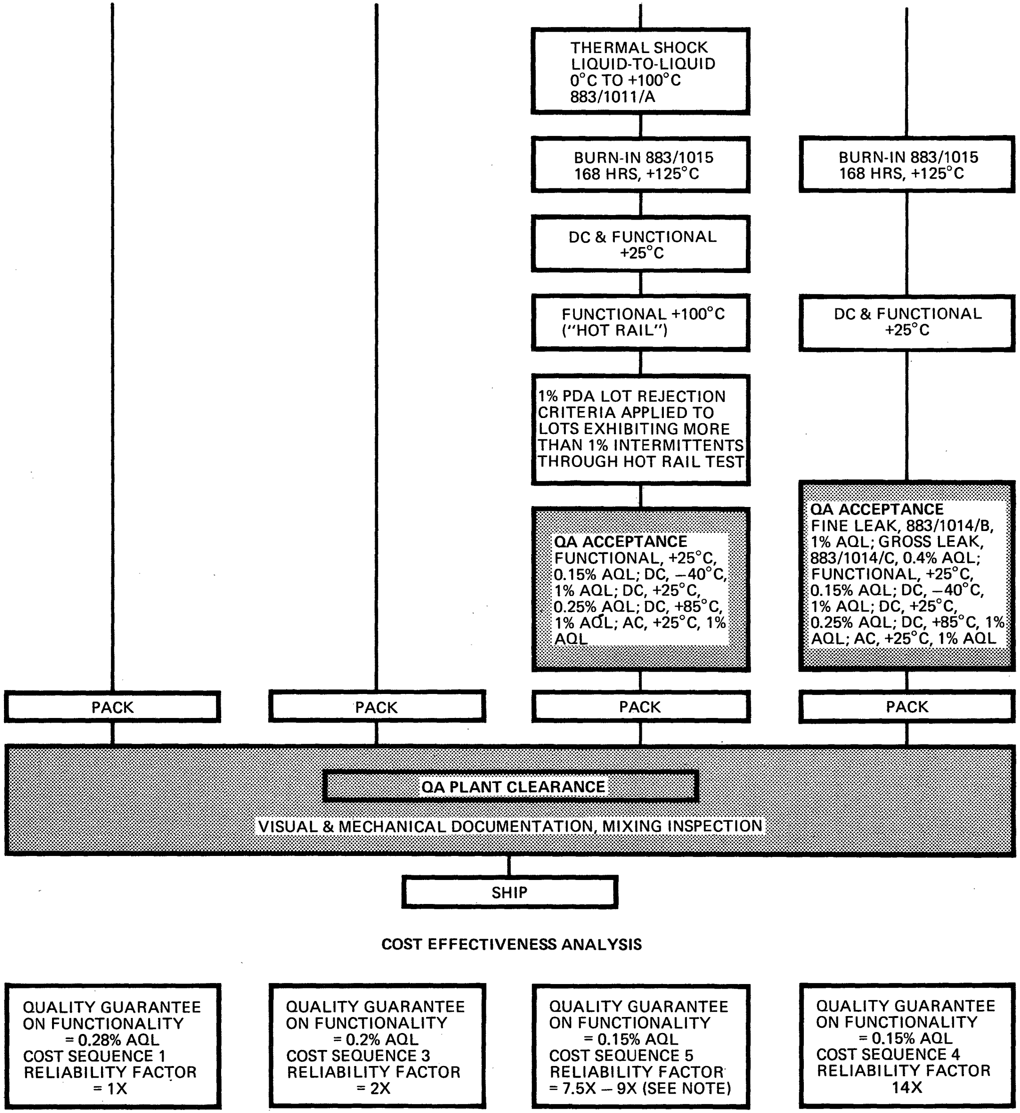


EXAMPLES

(a)	4001BPC	Device type 4001B, packaged in plastic Dual In-line (P), in commercial temperature range (C) and processed to Matrix VI Level 1.
(b)	4001BDC	Device type 4001B, packaged in ceramic Dual In-line (D), in commercial temperature range and processed to Matrix VI Level 3.
(c)	4001BPCQR	Device type 4001B, packaged in Dual In-line, in commercial temperature range (C) with supplemental Matrix VI Level 5 screening including 100% thermal shock, "hot rail" test, 168 hours 125°C burn-in and 0.15% AQL functional testing.
(d)	4001BDCQR	Device type 4001B, packaged in ceramic Dual In-line, in commercial temperature range with supplemental Matrix VI Level 6 screening including burn-in, three 100% DC/functional tests and 0.15% AQL functional testing.

MATRIX VI PROCESS FLOW OPTIONS & COST EFFECTIVENESS





Note: Burn-In has the same relative effectiveness for plastic molded devices as for ceramic/hermetic packaged devices. Assuming a controlled (air conditioned and constant power) field application/environment, the reliability factor would be approximately 9X. But should the field application be in a less controlled and power ON/OFF application, the reliability factor would be approximately 7.5X.

UNIQUE 38510 PROGRAM ORDERING INFORMATION

The Fairchild Unique 38510 Program is written in accordance with MIL-M-38510 and MIL-STD-883

To meet the need of improved reliability in the military market, CMOS Integrated Circuits are available with special processing. Devices ordered to this program are subjected to the 100% screening as outlined in the Process. Devices will be marked in accordance with unique 38510 unless otherwise specified under number Option 6.

UNIQUE 38510 devices are not normally stocked by distributors.

Customer procurement documents should specify the following:

(a) Fairchild Product Code indicating the basic device type and package combination.
(b) The Unique 38510 Device Class. (A, B*, B, C)
(c) Number and/or Letter Options required.
(d) Special Marking requirements.

The order code number consists of (a) and (b) as shown above. The order code detailed format is shown below.

4001B	D	M	QX
↑	↑	↑	↑
DEVICE TYPE	PACKAGE TYPE D = CERAMIC DIP P = PLASTIC DIP F = CERAMIC FLAT	TEMPERATURE RANGE C = –40°C TO +85°C(59X) M = –55°C TO +125°C(51X)	DESIGNATES UNIQUE 38510 PROCESSING IF REQUIRED. SEE DESCRIPTION OF SCREENING REQUIREMENTS

Order code examples are:

4029BFMQB Class QB Unique 38510	4007UBDMQS Class QS Unique 38510

Number Options: These options apply to operations performed on each unit delivered:

OPTION 1	Lead form to dimensions in detail specifications, followed by hermetic seal tests.
OPTION 2	Hot solder dip finish.
OPTION 3	Read and record critical parameters before and after burn-in.
OPTION 4	Initial qualification, Group B, C & D quality conformance not required.
OPTION 5	Radiographic inspection shall be performed on all devices.
OPTION 6	Special marking required.
OPTION 7	Non-conforming variation – refer to procurement documents for details (must be negotiated with factory).

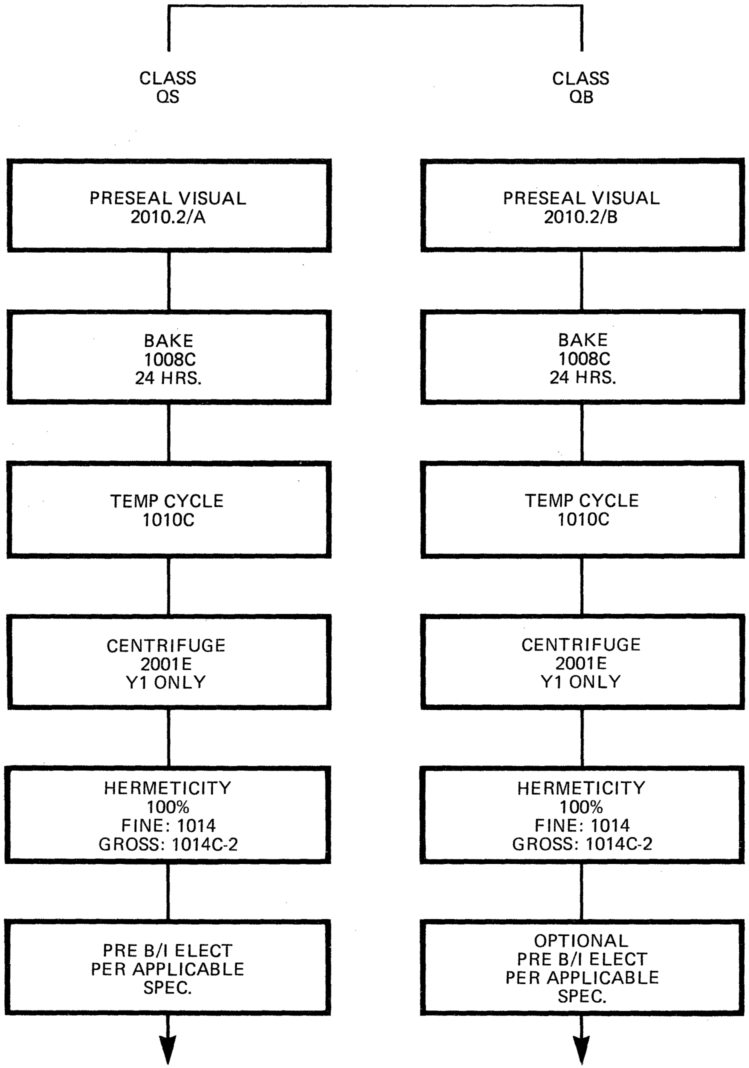
Letter Options: These options apply once per Purchase Order or line item and are considered Test Charges:

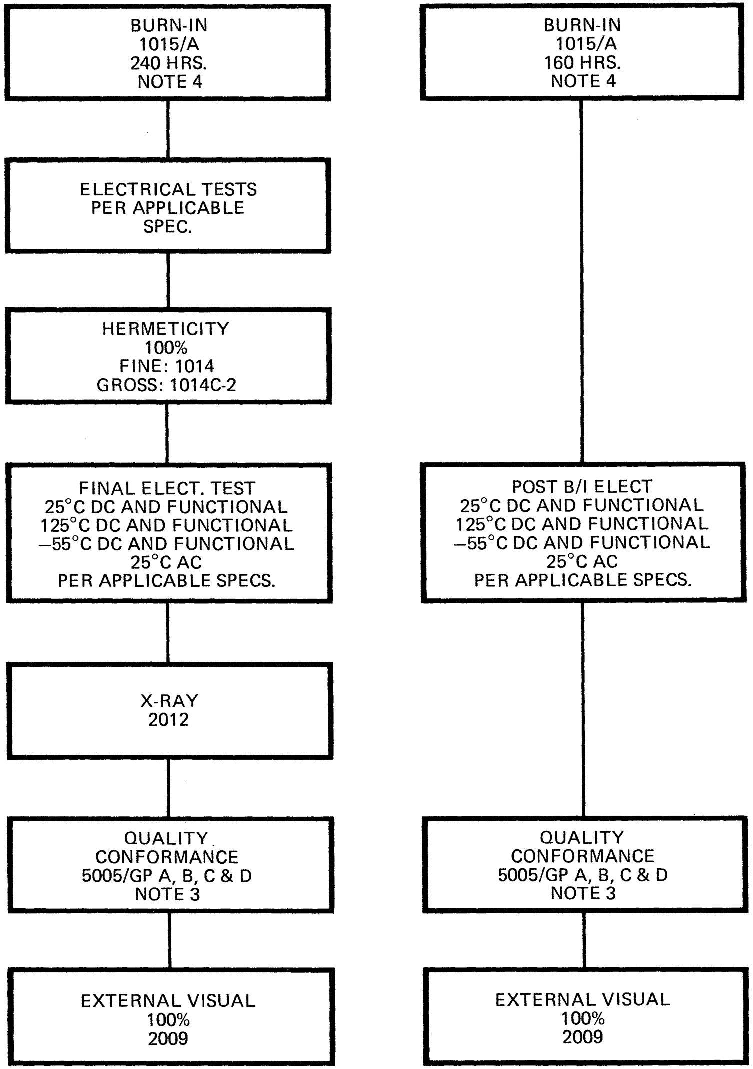
OPTION A	Group C testing shall be performed on customer's parts.
OPTION B	Group D testing shall be performed on customer's parts.
OPTION C	Generic data to be supplied from the latest completed lot.
OPTION D	Unique 38510 program plan, pertinent to the device family being purchased, shall be supplied.

PROCESS SCREENING REQUIREMENTS

MIL-STD-883 TEST METHODS	DESCRIPTION
Preseal Visual MTD. 2010.2	Cond. A – Class QA Cond. B – Other Classes
Bond Strength:	Bond strength is monitored on a sample basis three times per shift per mach.
Seal:	Devices are hermetically sealed for compliance to MIL-STD-883 requirements
High Temperature Storage:	Cond. C Tstg = 150°C/24 hrs
Temperature Cycle MTD 1010:	Cond. C –65°/150°C 10 cycles
Constant Acceleration MTD 2001:	Cond. E 30000 Gs Y_1 only
Hermetic Seal MTD 1014:	Cond. B Fine-Radiflo 5×10^{-8}cc/sec Cond. C2 Gross-FC78 with pressure 10^{-5}cc/sec
Pre Burn-In Electrical	Per detailed drawing to remove rejects prior to submission to burn-in screen
Burn-in Screen MTD 1015:	Cond. A – Static burn-in inputs alternately HIGH and LOW.
Post Burn-in Electrical (5004.1):	Per detailed drawing to cull out devices which failed as a result of burn-in.
Radiography MTD 2012:	Two views
Quality Conformance Inspection MTD 5005	Group A: Electrical Characteristics Group B: Physical Dimensions, marking permanence, bond strength, solderability Group C: Die Related Tests Group D: Packaged Related Tests
External Visual MTD 2009:	3X, 20X magnification: Verify dimensions, configuration, lead structure, marking and workmanship

UNIQUE 38510
NOTE 2



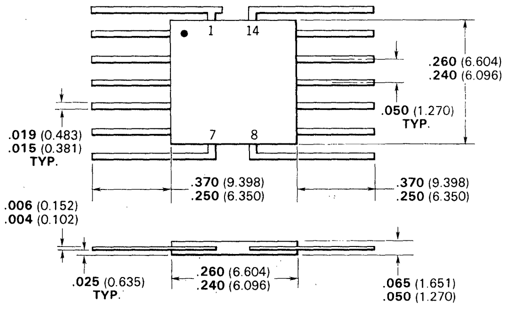


1. Unique 38510 is written around the MIL-M-38510 requirements with a few modifications to Method 5005 in that 100% dc testing at the temperature extremes and 100% ac testing at 25°C is not done and Unique 38510 QS has some burn-in logistics differences.
2. Qualification testing per groups B, C and D on a customer's parts require additional lot charges and an added minimum of two months to the schedules deliveries.
3. Any burn-in condition other than MTD 1015 Condition A is at customer request only.

PACKAGE OUTLINES

In Accordance with JEDEC TO-86 Outline 14-Pin Cerpak

3I



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

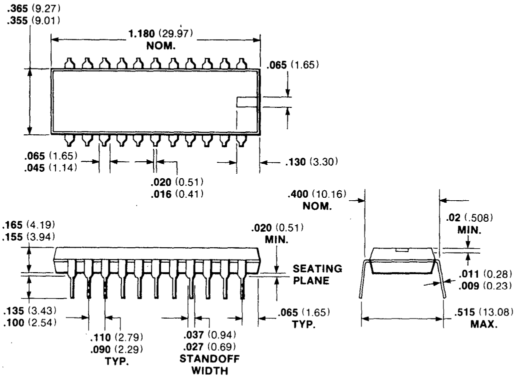
Pins are alloy 42

Package weight is 0.26 gram

Pin 1 orientation may be either tab or dot

22-Pin MSI Plastic Dual In-Line

4K



NOTES:

Pins are tin-plated 42 alloy

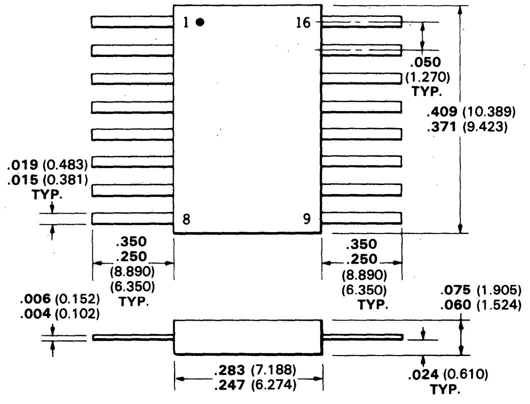
Package material is plastic

Pins are intended for insertion in hole rows on 400 (10.16) centers.

They are purposely shipped with "positive" misalignment to facilitate insertion.

16-Pin Cerpak

4L



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

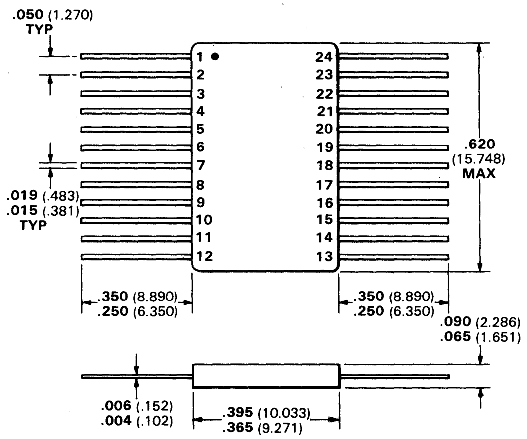
Pins are alloy 42

Package weight is 0.4 gram

Hermetically sealed beryllia package

24-Pin BeO Cerpak

4M



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are alloy 42

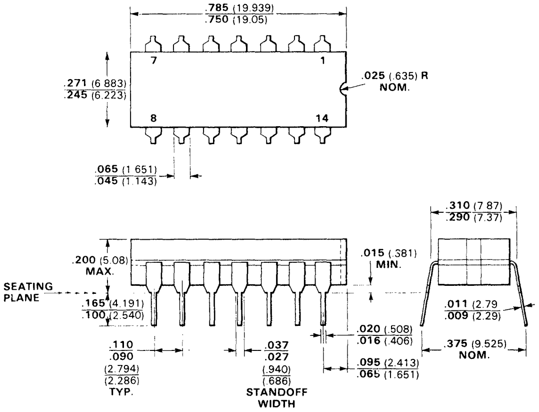
Package weight is 0.8 gram

Hermetically sealed beryllia package

PACKAGE OUTLINES

in accordance with JEDEC (TO-116) outline 14-Pin Ceramic Dual In-Line

6A



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .300" (7.620) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

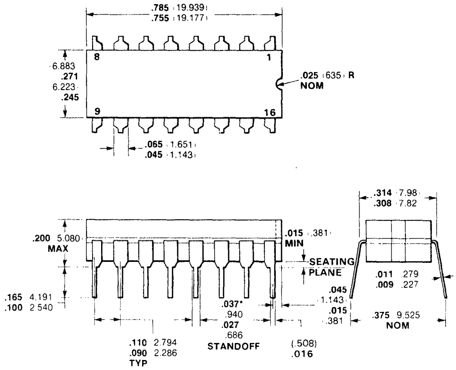
Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin

Pins are alloy 42

Package weight is 2.0 grams

16-Pin Ceramic Dual In-Line

6B



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .300" (7.620) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

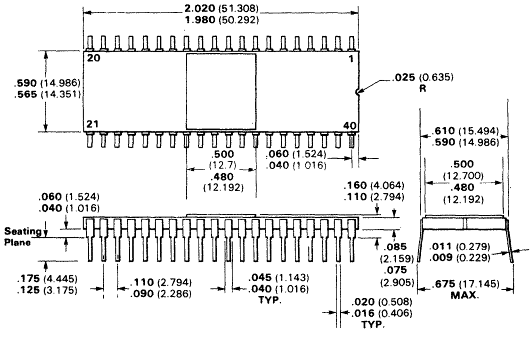
Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin

Pins are alloy 42

Package weight is 2.0 grams

*The .037/.027 (.940/.686) dimension does not apply to the corner pins

40-Pin Dual In-Line Side Brazed, Large Cavity



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pin material nickel gold-plated kovar

Cap is kovar

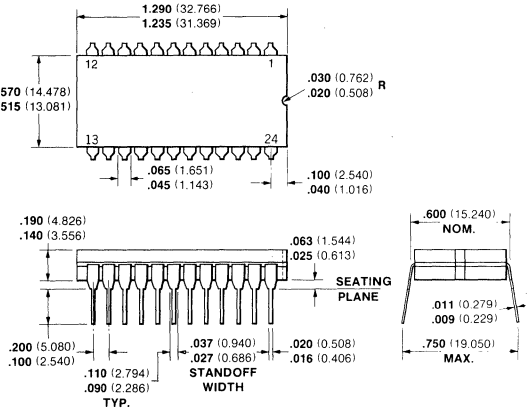
Base is ceramic

Package weight is 6.5 grams

PACKAGE OUTLINES

24-Pin Ceramic Dual In-Line

6N



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .600" (15.24) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

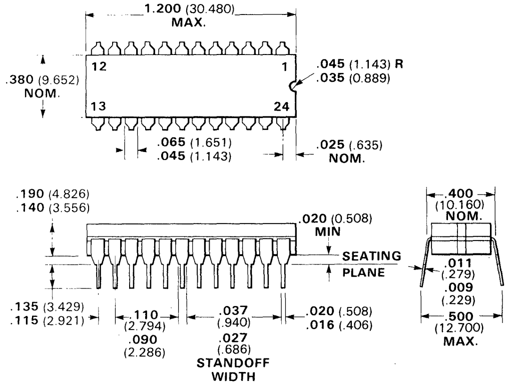
Pins are alloy 42

Package weight is 6.5 grams

Package material is alumina

24-Pin Ceramic Dual In-Line

6Q



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .400" (10.16) centers

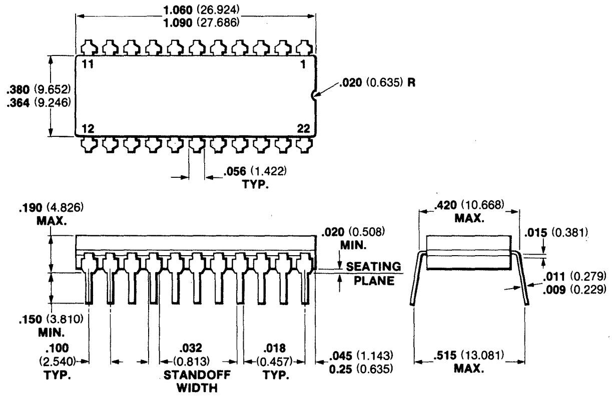
They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin

Pins are alloy 42

22-Pin Ceramic Dual In-Line

6V



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are tin-plated 42 alloy

Package material is alumina

Pins are intended for insertion in hole rows on .400 (10.160) centers

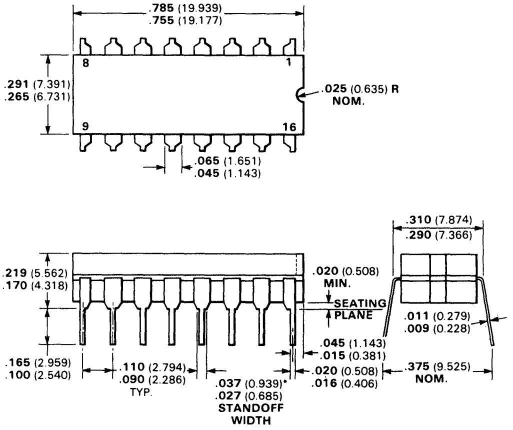
They are purposely shipped with "positive misalignment to facilitate insertion.

Package weight is 6.0 grams

PACKAGE OUTLINES

16-Pin Dual In-Line

7B



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .300" (7.620) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin

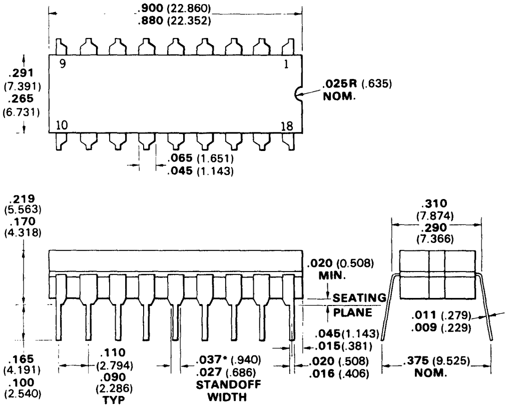
Pins are alloy 42

Package weight is 2.2 grams

*The .037/.027 (.940/.686) dimension does not apply to the corner pins

18-Pin Ceramic Dual In-Line

7D



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .300" (7.620) centers

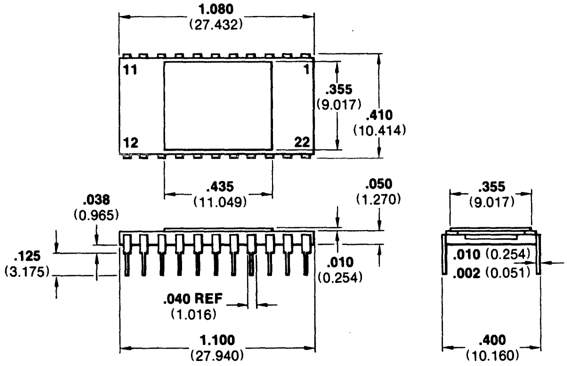
They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin

Pins are alloy 42

22-Pin Dual In-Line (Metal Cap)

7I



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insersion in hole rows on .400" (10.16) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020" (0.51) diameter pin

Pins are gold-plated Kovar

Cap is Kovar

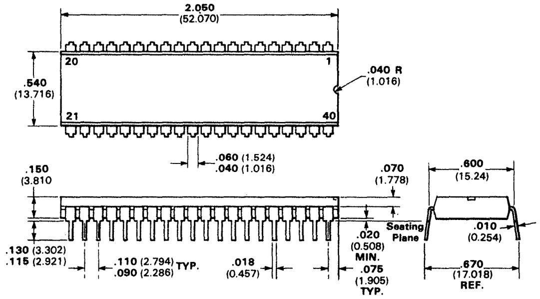
Base is ceramic

Package weight is 4 grams

PACKAGE OUTLINES

40-Pin Plastic Dip (Production Mold)

8P



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are alloy 42

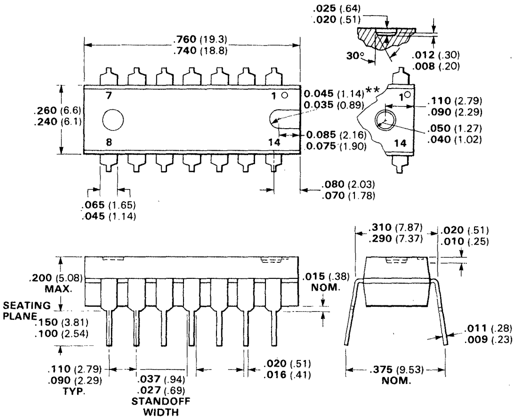
Package material is plastic

Pins are intended for insertion in hole rows on .600" (15.24) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

14-Pin Plastic Dual In-Line

9A



NOTES:

All dimensions in inches (bold) and millimeters (parantheses)

Pins are intended for insertion in hole rows on .300" (7.620) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin

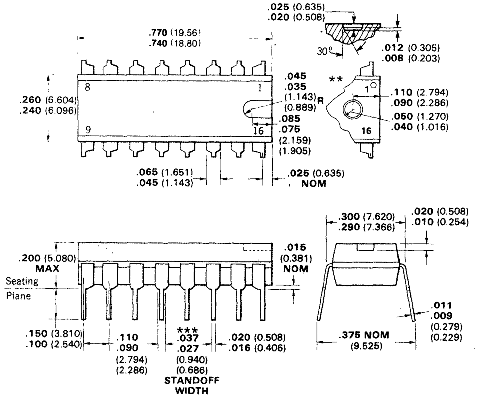
Pins are alloy 42

Package weight is 0.9 gram

Package material is silicone

16-Pin Plastic Dual In-Line

9B



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are alloy 42

Pins are intended for insertion in hole rows on .300" (7.620) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

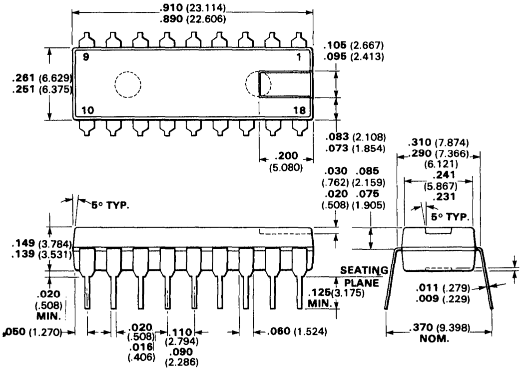
Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin

***The .037/.027 (.940/.686) dimension does not apply to the corner pins

Package weight is 0.9 gram

18-Pin Plastic Dual In-Line

9M



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .300" (7.620) centers

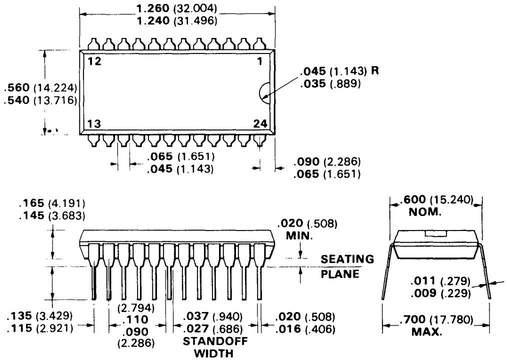
They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin

Pins are alloy 42

24-Pin Plastic Dual In-Line

9N



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .600" (15.24) centers

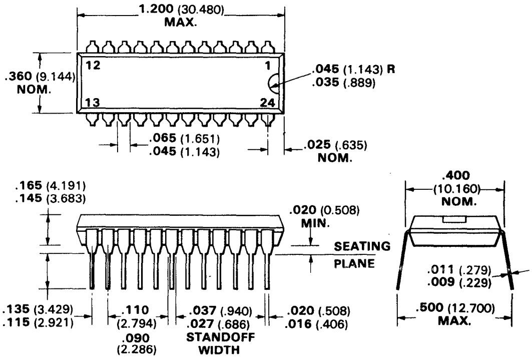
They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin

Pins are alloy 42

24-Pin Plastic Dual In-Line

9U



NOTES:

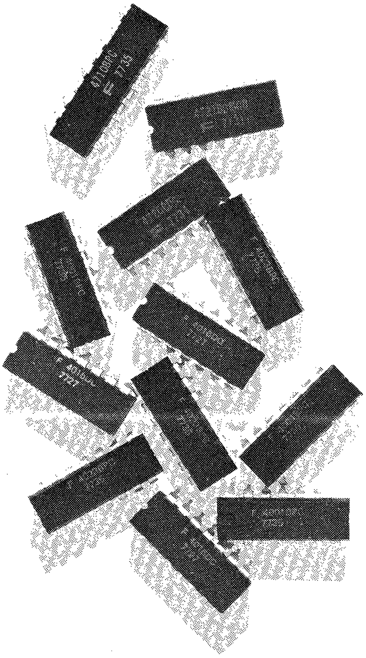
All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .400" (10.16) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin

Pins are alloy 42



Fairchild Semiconductor Franchised Distributors United States and Canada

Alabama
Hallmark Electronics
4900 Bradford Drive
Huntsville, Alabama 35807
Tel: 205-837-8700 TWX: 810-726-2187

Hamilton/Avnet Electronics
4692 Commercial Drive
Huntsville, Alabama 35805
Tel: 205-837-7210
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

Arizona
Hamilton/Avnet Electronics
505 S. Madison Drive
Tempe, Arizona 85281
Tel: 602-275-7851 TWX: 910-951-1535

Kierulff Electronics
4134 East Wood Street
Phoenix, Arizona 85040
Tel: 602-243-4101

Wyle Distribution Group
8155 North 24th Ave.
Phoenix, Arizona 85021
Tel: 602-249-2232 TWX: 910-951-4282

California
Avnet Electronics
350 McCormick Avenue
Costa Mesa, California 92626
Tel: 714-754-6111 (Orange County)
213-558-2345 (Los Angeles)
TWX: 910-595-1928

Bell Industries
Electronic Distributor Division
1161 N. Fair Oaks Avenue
Sunnyvale, California 94086
Tel: 408-734-8570 TWX: 910-339-9378

Wyle Distribution Group
3000 Bowers Avenue
Santa Clara, California 95051
Tel: 408-727-2500 TWX: 910-338-0541

Hamilton Electro Sales
3170 Pullman Avenue
Costa Mesa, California 92636
Tel: 714-979-6864

Hamilton Electro Sales
10912 W. Washington Blvd.
Culver City, California 90230
Tel: 213-558-2121 TWX: 910-340-6364

Hamilton/Avnet Electronics
1175 Bordeaux Drive
Sunnyvale, California 94086
Tel: 408-743-3355 TWX: 910-379-6486

Hamilton/Avnet Electronics
4545 Viewridge Avenue
San Diego, California 92123
Tel: 714-571-7527
Telex: HAMAVELEC SDG 69-5415

Anthem Electronics
1020 Stewart Drive
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Sunnyvale, California 94086
Tel: 408-738-1111

Anthem Electronics, Inc.
4040 Sorrento Valley Blvd.
San Diego, California 92121
Tel: 714-279-5200

Anthem Electronics, Inc.
2661 Dow Avenue
Tustin, California 92680
Tel: 714-730-8000

Wyle Electronics
124 Maryland Street
El Segundo, California 90245
Tel: 213-322-8100 TWX: 910-348-7111

Wyle Distributor Group
17872 Cowan Avenue
Irvine, California 92714
Tel: 714-641-1600
Telex: 610-595-1572

**Sertech Laboratories
2120 Main Street, Suite 190
Huntington Beach, California 92647
Tel: 714-960-1403

Wyle Distribution Group
9525 Chesapeake
San Diego, California 92123
Tel: 714-565-9171 TWX: 910-335-1590

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Bell Industries
8155 West 48th Avenue
Wheatridge, Colorado 80033
Tel: 303-424-1985 TWX: 910-938-0393

Arrow Electronics
2121 South Hudson
Denver, Colorado 80222
Tel: 303-758-2100

Wyle Distribution Group
6777 E. 50th Avenue
Commerce City, Colorado 80022
Tel: 303-287-9611 TWX: 910-936-0770

Hamilton/Avnet Electronics
8765 E. Orchard Rd., Suite 708
Englewood, Colorado 80111
Tel: 303-740-1000 TWX: 910-935-0787

Connecticut
Arrow Electronics, Inc.
12 Beaumont Road
Wallingford, Connecticut 06492
Tel: 203-265-7741 TWX: 203-265-7741

Hamilton/Avnet Electronics
Commerce Drive, Commerce Park
Danbury, Connecticut 06810
Tel: 203-797-2800
TWX: None — use 710-897-1405
(Regional Hq. in Mt. Laurel, N.J.)

Harvey Electronics
112 Main Street
Norwalk, Connecticut 06851
Tel: 203-853-1515

Schweber Electronics
Finance Drive
Commerce Industrial Park
Danbury, Connecticut 06810
Tel: 203-792-3500

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Arrow Electronics
1001 Northwest 62nd Street
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Ft. Lauderdale, Florida 33309
Tel: 305-776-7790

Arrow Electronics
115 Palm Bay Road N.W.
Suite 10 Bldg. #200
Palm Bay, Florida 32905
Tel: 305-725-1408

Hallmark Electronics
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Tel: 305-971-9280 TWX: 510-956-3092

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Ft. Lauderdale, Florida 33309
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3197 Tech Drive, North
St. Petersburg, Florida 33702
Tel: 813-576-3930

Schweber Electronics
2830 North 28th Terrace
Hollywood, Florida 33020
Tel: 305-927-0511 TWX: 510-954-0304

Georgia
Arrow Electronics
2979 Pacific Drive
Norcross, Georgia 30071
Tel: 404-449-8252
Telex: 810-766-0439

Hamilton/Avnet Electronics
6700 Interstate 85 Access Road, Suite 1E
Norcross, Georgia 30071
Tel: 404-448-0800
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

Illinois
Hallmark Electronics, Inc.
1177 Industrial Drive
Bensenville, Illinois 60106
Tel: 312-860-3800

Hamilton/Avnet Electronics
3901 N. 25th Avenue
Schiller Park, Illinois 60176
Tel: 312-678-6310 TWX: 910-227-0060

Kierulff Electronics
1536 Landmeier Road
Elk Grove Village, Illinois 60007
Tel: 312-640-0200 TWX: 910-227-3166

Schweber Electronics, Inc.
1275 Brummel Avenue
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Chicago, Illinois 60666

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195 Spangler Avenue
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Elmhurst, Illinois 60126
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Hallmark Electronics, Inc.
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Shawnee Mission, Kansas 66214
Tel: 913-888-4746

Hamilton/Avnet Electronics
9219 Guivira Road
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Tel: 913-888-8900
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

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Tel: 504-887-7610
Telex: STERLE LEC MRIE 58-328

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6655 Amberton Drive
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Hamilton/Avnet Electronics
(mailing address)
Friendship International Airport
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Baltimore, Maryland 21240

(shipping address)
7235 Standard Drive
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Tel: 313-525-8100

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Tel: 313-971-8220

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7449 Cahill Road
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Earth City, Missouri 63045
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Tel 609-424-0880

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10 Industrial Road
Fairfield, New Jersey 07006
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774 Pfeiffer Blvd.
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Tel: 215-627-1920

Wilshire Electronics
1111 Paulison Avenue
Clifton, N.J. 07015
Tel: 201-365-2600 TWX: 710-989-7052

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Bell Industries
11728 Linn Avenue N.E.
Albuquerque, New Mexico 87123
Tel: 505-292-2700 TWX: 910-989-0625

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Albuquerque, New Mexico 87119
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Arrow Electronics
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20 Oser Avenue
Hauppauge, New York 11787
Tel: 516-231-1000

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40-17 Oser Avenue
Hauppauge, New York 11787
Tel: 516-231-6722

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TWX: 710-545-0230

Components Plus, Inc.
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Hauppauge, L.I., New York 11787
Tel: 516-231-9200 TWX: 510-227-9869

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Tel: 315-437-2642 TWX: 710-541-0959

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5 Hub Drive
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Tel: 607-748-8211

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3939 Ann Arbor
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The Lyons Corporation
6151 Wilson Mills Road, Suite 101
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Tel: 216-461-8288
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Technical Marketing
9717 E. 42nd Street, Suite 221
Tulsa, Oklahoma 74145
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